INTRODUCTION

TOSHIBA HS-C² MOS FAMILY (TC74HC SERIES)

During the past few years, the integration scale of MOS LSIs has made a rapid progress owing to the advance of the micro-lithograph technology. Along with this progress, the heat radiation of MOS LSIs has become a big problem in the same way the bipolar world has been struggling for many years. At present, it is well known that only CMOS technology will solve this problem, and CMOS technology has been adopted increasingly in the field of various LSIs for major example high-performance microprocessors and large capacity memories.

However, there was no general purpose logic IC interfacing these high-performance LSIs except LSTTLs which will satisfy simply the speed requirement.

Therefore, in many cases the excellent features of CMOS LSIs could not be fully utilized in the application systems.

The TC74HC series IC is the CMOS logic IC in a new generation which achieves the high-speed operation thirty times as much as that of conventional B series CMOS IC while maintaining the low power dissipation of conventional CMOS. This high-performance was accomplished utilizing as much advanced micro-lithograph technology as that of the high-performance CMOS LSIs.

These logic ICs will bring a large improvement into the limited performance of conventional systems in every respect of characteristics such as power dissipation, noise margin, margin for operating voltage and operating temperature, etc.

Since the individual ICs are pin-to-pin compatible with LSTTL or conventional B series CMOS, no logical redesign may be required at the time of adopting TC74HC series ICs into the existing systems.

This data book provides technical information on TOSHIBA's TC74HC series high-speed C² MOS devices. The contents described in this data book are subject to change without notice due to standardization of the specification in JEDEC, etc.

Note: Toshiba does not assume any responsibility for use of any circuity described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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TC74HCT640P/F	OCTAL BUS TRANSCEIVER (3-STATE/INV.)	20	432
TC74HC643P/F	OCTAL BUS TRANSCEIVER (3-STATE)	20	427
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TC74HC697P	U/D 4-BIT BINARY CTR./REGISTER (3-STATE)	20	692
TC74HC698P *	U/D DECADE COUNTER/REGISTER (3-STATE)	20	–
TC74HC699P *	U/D 4-BIT BINARY CTR./REGISTER (3-STATE)	20	–
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Type Number	Function	Number of Pins	Page
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TC74HC4022P/F	OCTAL COUNTER/DIVIDER	16	717
TC74HC4024P/F	7-STAGE BINARY COUNTER	14	723
TC74HC4028P/F	BCD-TO-DECIMAL DECODER	16	728
TC74HC4040P/F	12-STAGE BINARY COUNTER	16	733
TC74HC4049P/F	HEX BUFFER (INV.)	16	738
TC74HC4050P/F	HEX BUFFER	16	738
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TC74HC4052P *	DUAL 4-CHANNEL ANALOG MULTIPLEXER	16	—
TC74HC4053P *	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	16	—
TC74HC4060P/F	14-STAGE BINARY COUNTER/OSCILLATOR	16	742
TC74HC4066P/F	QUAD BILATERAL SWITCH	14	748
TC74HC4072P/F	DUAL 4-INPUT OR GATE	14	753
TC74HC4075P/F	TRIPLE 3-INPUT OR GATE	14	757
TC74HC4078P/F	8-INPUT OR/NOR GATE	14	761
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Note: 1. All DIP 24 pin products service as an enclosure of the narrow type (300mil)
2. * denotes the products under development

2. HIGH SPEED CMOS SELECTION GUIDE

FUNCTION			TYPE NUMBER
GATE	NAND NOR AND OR INVERTER		74HC00, 74HC03, 74HC10, 74HC20, 74HC30, 74HC133 74HC02, 74HC27, 74HC4002, 74HC4078 74HC08, 74HC11, 74HC21 74HC32, 74HC4075, 74HC4072, 74HC4078 74HCU04, 74HC04, 74HCT04
	SCHMITT TRIGGER		74HC14, 74HC132
	MULTIFUNCTION		74HC51, 74HC86, 74HC386, 74HC7266
BUFFER			74HC4049, 74HC4050, 74HCT7007
	3-STATE		74HC125, 74HC126, 74HC240, 74HCT240, 74HC241, 74HCT241, 74HC244, 74HCT244, 74HC365, 74HC366, 74HC367, 74HC368, 74HC540, 74HCT540, 74HC541, 74HCT541
	BIDIRECTIONAL		74HC242, 74HC243, 74HC245, 74HCT245, 74HC620 74HC623, 74HC640, 74HCT640, 74HC643, 74HCT643
FLIP-FLOP	J-K, FLIP-FLOP		74HC73, 74HC76, 74HC107, 74HC109, 74HC112, 74HC113
	D FLIP-FLOP		74HC74, 74HC174, 74HC175, 74HC273, 74HC377
		3-STATE	74HC374, 74HCT374, 74HC534, 74HC564, 74HCT564, 74HC574, 74HCT574, 74HC646, 74HCT646, 74HC648, 74HCT648, 74HC651, 74HCT651, 74HC652, 74HCT652
LATCH			74HC75, 74HC77, 74HC259, 74HC279, 74HC375
		3-STATE	74HC373, 74HCT373, 74HC533, 74HC563, 74HCT563, 74HC573, 74HCT573
MULTIVIBRATOR			74HC123, 74HC221, 74HC423, 74HC4538
DECODER			74HC42, 74HC131, 74HC137, 74HCT137, 74HC138, 74HCT138, 74HC139, 74HC154, 74HC155, 74HC237, 74HC238, 74HC4028, 74HC4514, 74HC4515
		7-SEGMENT	74HC4511, 74HC4543
ENCODER			74HC147, 74HC148
REGISTER			74HC164, 74HC165, 74HC166, 74HC173, 74HC194, 74HC195, 74HC299, 74HC323, 74HC595, 74HC597, 74HC670, 74HC4094
COUNTER		BINARY	74HC161, 74HC163, 74HC191, 74HC193, 74HC393, 74HC590, 74HC592, 74HC593, 74HC691, 74HC693, 74HC697, 74HC699, 74HC4520
		DECADE	74HC160, 74HC162, 74HC190, 74HC192, 74HC390, 74HC690, 74HC692, 74HC696, 74HC698, 74HC4518
		DIVIDER	74HC4017, 74HC4020, 74HC4022, 74HC4024, 74HC4040, 74HC4060, 74HC40102, 74HC40103, 74HC7292, 74HC7294
MULTI-PLEXER		ANALOG	74HC4051, 74HC4052, 74HC4053, 74HC4066
		DIGITAL	74HC151, 74HC153, 74HC157, 74HC158, 74HC251, 74HC253, 74HC257, 74HC258, 74HC298, 74HC354, 74HC356
OTHERS	COMPARATOR		74HC85, 74HC688
	ADDER		74HC283
	ALU		74HC181, 74HC182
	PARITY TREE		74HC280

GATE

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 00	QUAD 2-INPUT NAND GATE	LS00	4011, 7400	14
74HC 03	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	LS03	*40107,*5029	14
74HC 10	TRIPLE 3-INPUT NAND GATE	LS10	4023	14
74HC 20	DUAL 4-INPUT NAND GATE	LS20	4012	14
74HC 30	8-INPUT NAND GATE	LS30	4068	14
74HC 133	13-INPUT NAND GATE	LS133		16
74HC 02	QUAD 2-INPUT NOR GATE	LS02	4001	14
74HC 27	TRIPLE 3-INPUT NOR GATE	LS27	4025,*4000	14
74HC4002	DUAL 4-INPUT NOR GATE	*LS25	4002	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 08	QUAD 2-INPUT AND GATE	LS08	4081	14
74HC 11	TRIPLE 3-INPUT AND GATE	LS11	4073	14
74HC 21	DUAL 4-INPUT AND GATE	LS21	4082	14
74HC 32	QUAD 2-INPUT OR GATE	LS32	4071	14
74HC4075	TRIPLE 3-INPUT OR GATE		4075	14
74HC4072	DUAL 4-INPUT OR GATE		4072	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 04	HEX INVERTER	LS04	*4069U	14
74HC T04	HEX INVERTER	LS04	*4069U	14
74HC U04	HEX INVERTER (SINGLE STAGE)	*LS04	4069U,7404U	14
74HC 51	DUAL 2W-2I AND/OR INVERT GATE	LS51	*4085	14
74HC 86	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC7266	QUAD EXCLUSIVE NOR GATE	*LS266	4077	14
74HC 386	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC 14	HEX SCHMITT INVERTER	LS14	4584	14
74HC 132	QUAD 2-INPUT SCHMITT NAND	LS132	4093	14

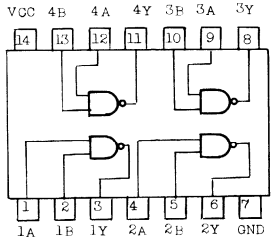
* Suggested alternative

GATE

QUAD 2-INPUT NAND GATE

00

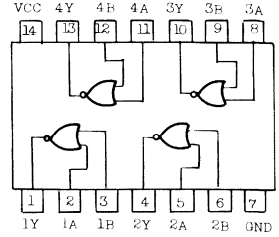
Positive logic: $Y = \overline{AB}$



QUAD 2-INPUT NOR GATE

02

Positive logic: $Y = \overline{A+B}$

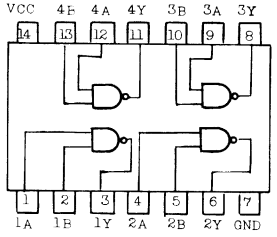


GATE (Continued)

QUAD 2-INPUT NAND GATE WITH OPEN DRAIN OUTPUT

03

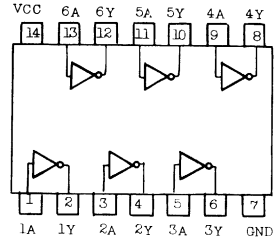
Positive logic: $Y = \overline{AB}$



HEX INVERTER

04
T04
U04

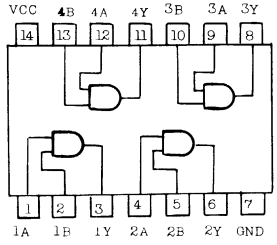
Positive logic: $Y = \overline{A}$



QUAD 2-INPUT AND GATE

08

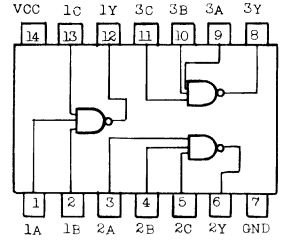
Positive logic: $Y = AB$



TRIPLE 3-INPUT NAND GATE

10

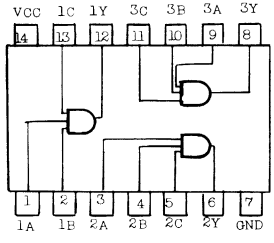
Positive logic: $Y = \overline{ABC}$



TRIPLE 3-INPUT AND GATE

11

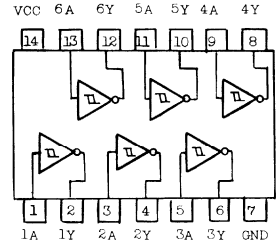
Positive logic: $Y = ABC$



HEX SCHMITT INVERTER

14

Positive logic: $Y = \overline{A}$

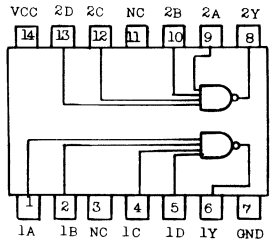


GATE (Continued)

DUAL 4-INPUT NAND GATE

20

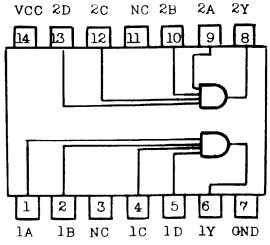
Positive logic: $Y = \overline{ABCD}$



DUAL 4-INPUT AND GATE

21

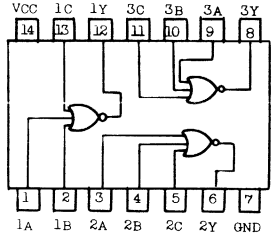
Positive logic: $Y = ABCD$



TRIPLE 3-INPUT NOR GATE

27

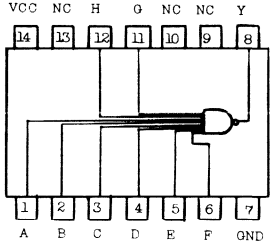
Positive logic: $Y = \overline{A+B+C}$



8-INPUT NAND GATE

30

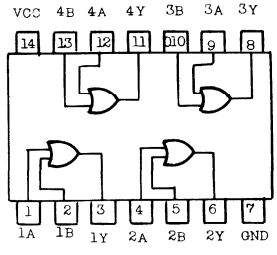
Positive logic: $Y = \overline{ABCDEFGH}$



QUAD 2-INPUT OR GATE

32

Positive logic: $Y = A+B$

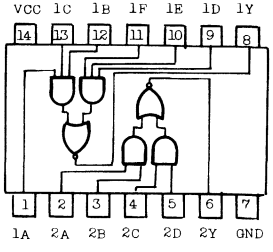


DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

51

Positive logic: $1Y=\overline{1A \cdot 1B \cdot 1C+1D \cdot 1E \cdot 1F}$

$2Y=\overline{2A \cdot 2B+2C \cdot 2D}$

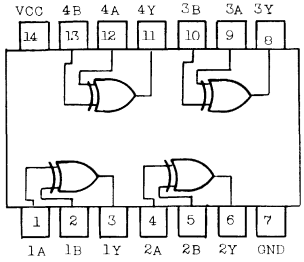


GATE (Continued)

QUAD 2-INPUT EXCLUSIVE-OR GATE

86

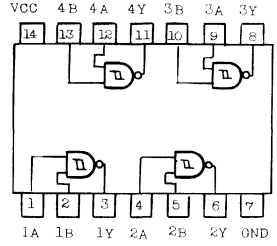
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



QUAD 2-INPUT SCHMITT NAND GATE

132

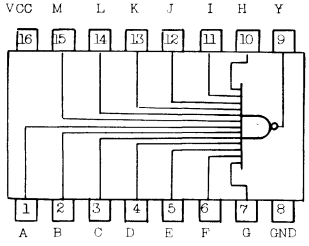
Positive logic: $Y=\overline{AB}$



13-INPUT NAND GATE

133

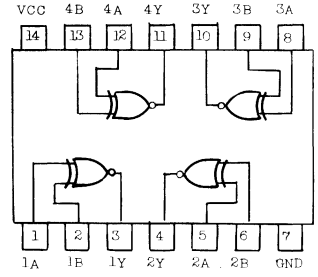
Positive logic: $Y=\overline{ABCDEFGHIJKLM}$



QUAD 2-INPUT EXCLUSIVE-NOR GATE

7266

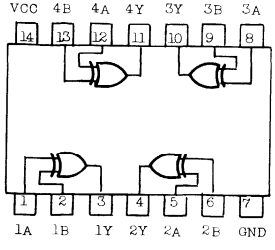
Positive logic: $Y=\overline{A\oplus B}=AB+\overline{A}\overline{B}$



QUAD 2-INPUT EXCLUSIVE-OR GATE

386

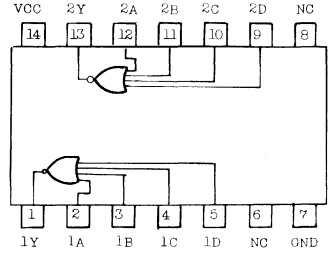
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



DUAL 4-INPUT NOR GATE

4002

Positive logic: $Y=\overline{A+B+C+D}$

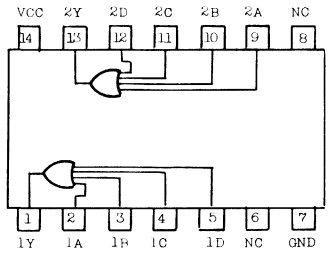


GATE (Continued)

DUAL 4-INPUT OR GATE

4072

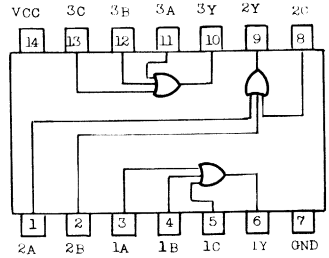
Positive logic: Y=A+B+C+D



TRIPLE 3-INPUT OR GATE

4075

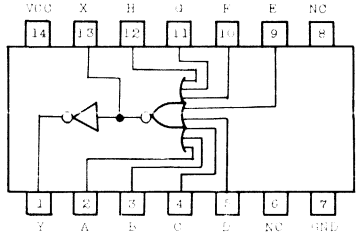
Positive logic: Y=A+B+C



8-INPUT NOR GATE

4078

Positive logic: Y=A+B+C+D+E+F+G+H



BUFFER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HCT7007	HEX BUFFER	* LS07		14
74HC4049	HEX BUFFER (INVERTING)		4049	16
74HC4050	HEX BUFFER		4050	16
74HC 125	QUAD BUS BUFFER	LS125	5024	14
74HC 126	QUAD BUS BUFFER	LS126	5025	14
74HC 240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HCT240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HC 241	OCTAL BUS BUFFER	LS241		20
74HCT241	OCTAL BUS BUFFER	LS241		20
74HC 244	OCTAL BUS BUFFER	LS244		20
74HCT244	OCTAL BUS BUFFER	LS244		20
74HC 365	HEX BUS BUFFER	LS365A		16
74HC 366	HEX BUS BUFFER (INVERTING)	LS366A		16
74HC 367	HEX BUS BUFFER	LS367A	5012	16
74HC 368	HEX BUS BUFFER (INVERTING)	LS368A		16
74HC 540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HCT540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HC 541	OCTAL BUS BUFFER	LS541		20
74HCT541	OCTAL BUS BUFFER	LS541		20
74HC 242	QUAD BUS TRANSCEIVER (INVERTING)	LS242		14
74HC 243	QUAD BUS TRANSCEIVER	LS243		14
74HC 245	OCTAL BUS TRANSCEIVER	LS245		20
74HCT245	OCTAL BUS TRANSCEIVER	LS245		20
74HC 620	OCTAL BUS TRANSCEIVER (INVERTING)	LS620		20
74HC 623	OCTAL BUS TRANSCEIVER	LS623		20
74HC 640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HCT640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HC 643	OCTAL BUS TRANSCEIVER	LS643		20
74HCT643	OCTAL BUS TRANSCEIVER	LS643		20

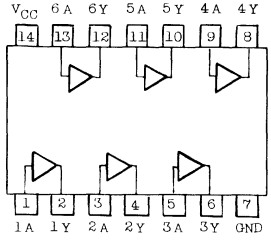
* Suggested alternative

BUFFER

HEX BUFFER

T7007

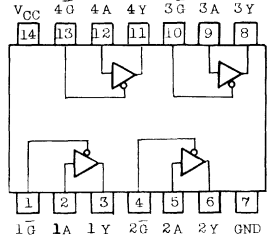
Positive logic: Y = A



QUAD BUS BUFFER

125

Positive logic: Y = A

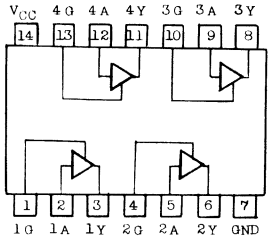


BUFFER (Continued)

QUAD BUS BUFFER

126

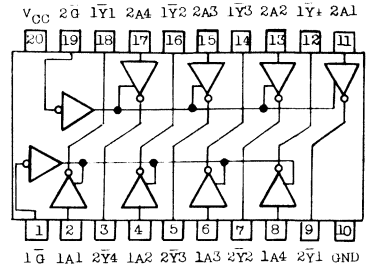
Positive logic: Y = A



OCTAL BUS BUFFER (INVERTING)

240

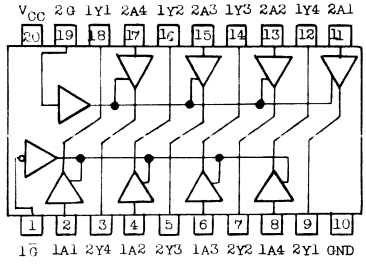
T240



OCTAL BUS BUFFER

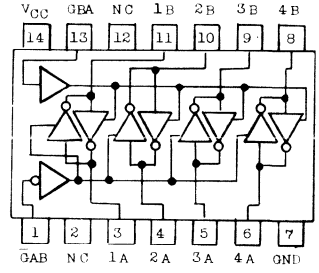
241

T241



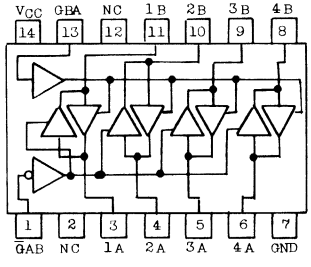
QUAD BUS TRANSCEIVER (INVERTING)

242



QUAD BUS TRANSCEIVER

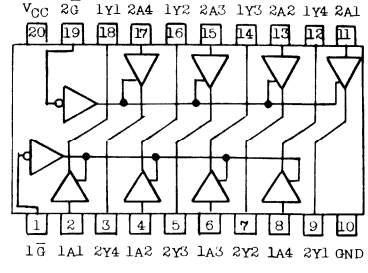
243



OCTAL BUS BUFFER

244

T244

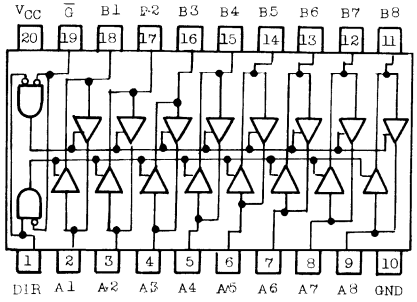


BUFFER (Continued)

OCTAL BUS TRANSCEIVER

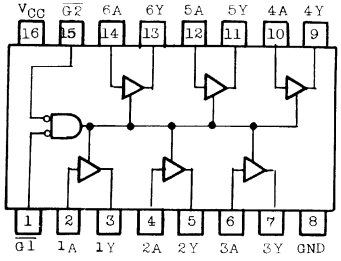
245

T245



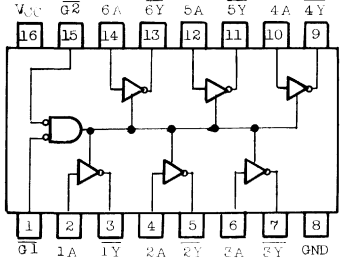
HEX BUS BUFFER

365



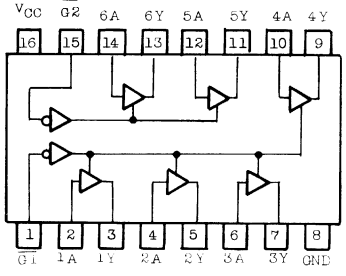
HEX BUS BUFFER (INVERTING)

366



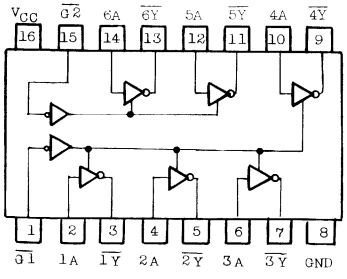
HEX BUS BUFFER

367



HEX BUS BUFFER (INVERTING)

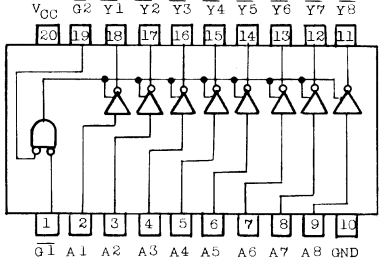
368



OCTAL BUS BUFFER (INVERTING)

540

T540

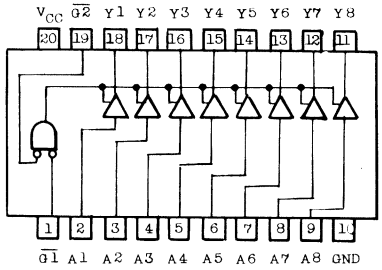


BUFFER (Continued)

OCTAL BUS BUFFER

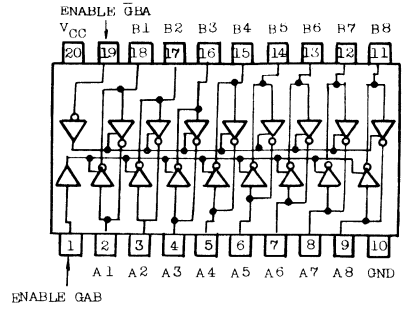
541

T541



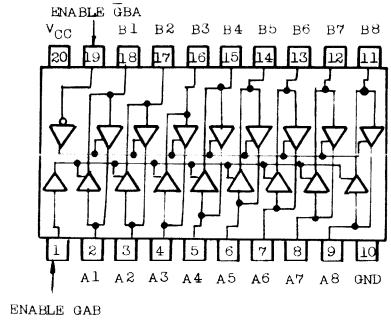
OCTAL BUS TRANSCEIVER (INVERTING)

620



OCTAL BUS TRANSCEIVER

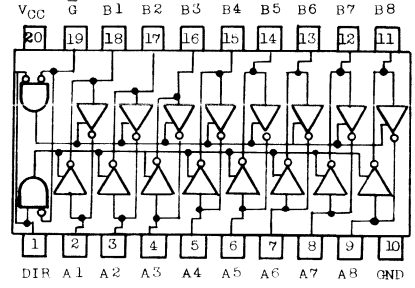
623



OCTAL BUS TRANSCEIVER (INVERTING)

640

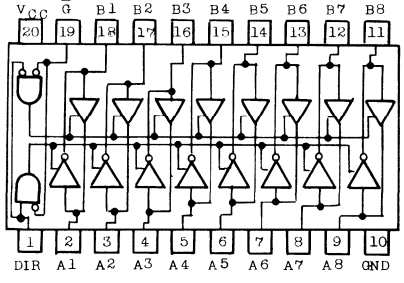
T640



OCTAL BUS TRANSCEIVER

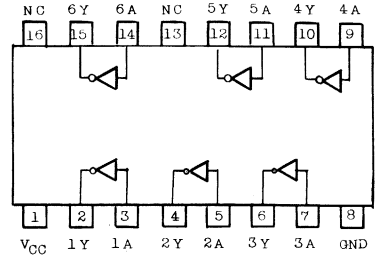
643

T643



HEX BUFFER/CONVERTER (INVERTING)

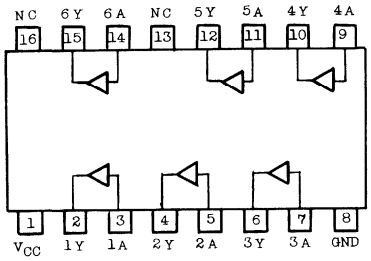
4049



BUFFER (Continued)

HEX BUFFER/CONVERTER

4050



FLIP–FLOP

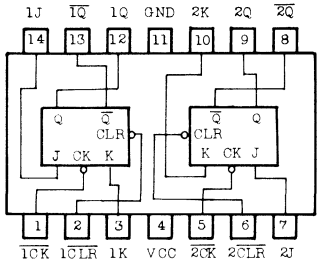
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 73	DUAL J-K FLIP-FLOP WITH CLEAR	LS73A,LS107A		14
74HC 76	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 107	DUAL J-K FLIP-FLOP WITH CLEAR	LS107A,LS73A		14
74HC 109	DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR	LS109A		16
74HC 112	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 113	DUAL J-K FLIP-FLOP WITH PRESET	LS113A		14
74HC 74	DUAL D FLIP-FLOP WITH PRESET AND CLEAR	LS74A	4013	14
74HC 174	HEX D FLIP-FLOP WITH CLEAR	LS174	40174	16
74HC 175	QUAD D FLIP-FLOP WITH CLEAR	LS175	40175	16
74HC 273	OCTAL D FLIP-FLOP WITH CLEAR	LS273		20
74HC 377	OCTAL D-TYPE FLIP-FLOP			20
74HC 374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 534	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS534		20
74HC 564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HCT564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HC 574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HCT646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HC 648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HCT648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HC 651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HCT651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HC 652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24
74HCT652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24

* Suggested alternative

FLIP-FLOP

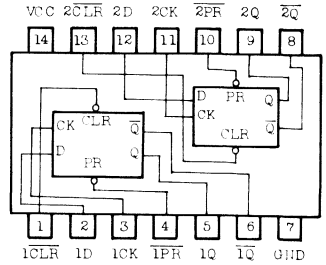
DUAL J-K FLIP-FLOP WITH CLEAR

73



DUAL D FLIP-FLOP WITH PRESET AND CLEAR

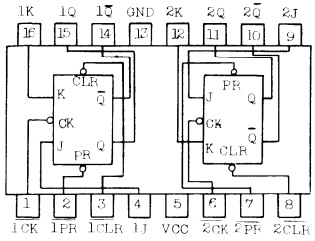
74



FLIP-FLOP (Continued)

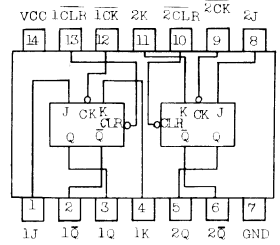
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

76



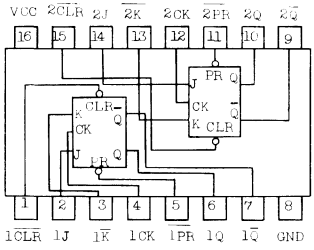
DUAL J-K FLIP-FLOP WITH CLEAR

107



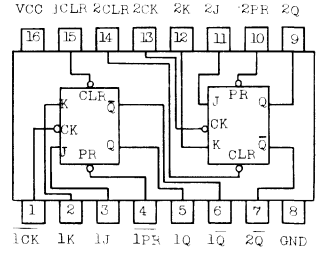
DUAL J-K̄ FLIP-FLOP WITH PRESET AND CLEAR

109



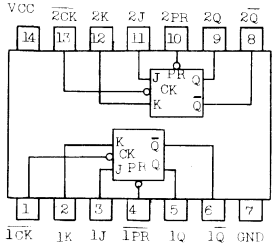
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

112



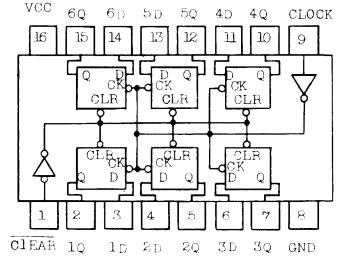
DUAL J-K FLIP-FLOP WITH PRESET

113



HEX D FLIP-FLOP WITH CLEAR

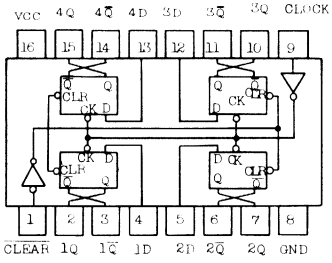
174



FLIP-FLOP (Continued)

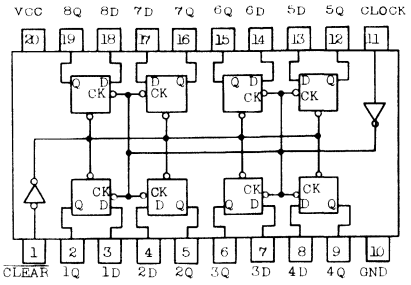
QUAD D FLIP-FLOP WITH CLEAR

175



OCTAL D FLIP-FLOP WITH CLEAR

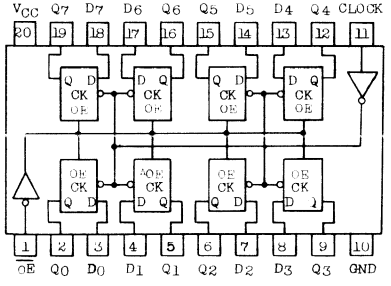
273



OCTAL D FLIP-FLOP (3-STATE)

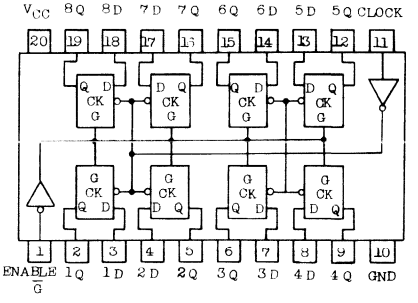
374

T374



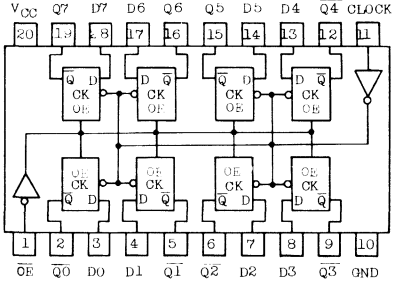
OCTAL D FLIP-FLOP

377



OCTAL D FLIP-FLOP (3-STATE/INV.)

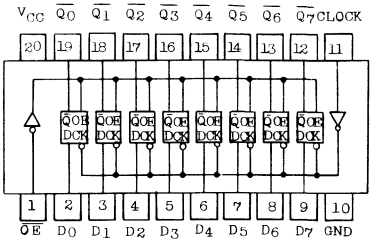
534



OCTAL D FLIP-FLOP (3-STATE/INV.)

564

T564

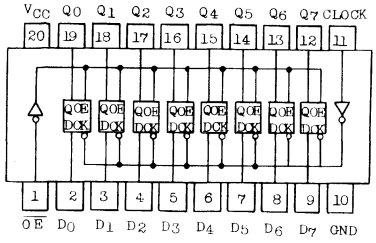


FLIP-FLOP (Continued)

OCTAL D FLIP-FLOP (3-STATE)

574

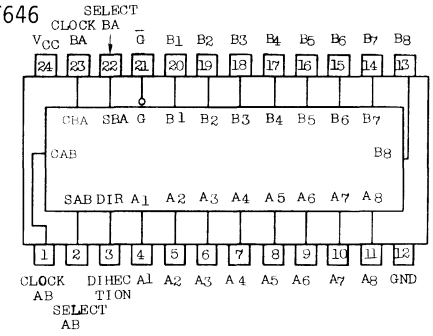
T574



OCTAL BUS TRANSCEIVER REGISTER (3-STATE)

646

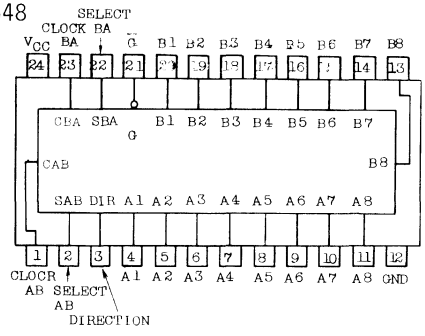
T646



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

648

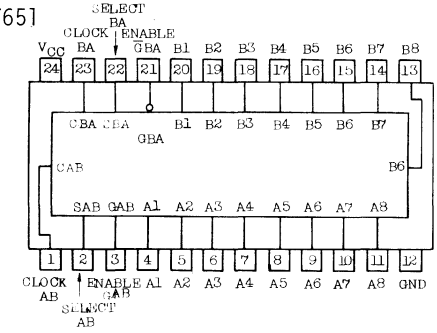
T648



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

651

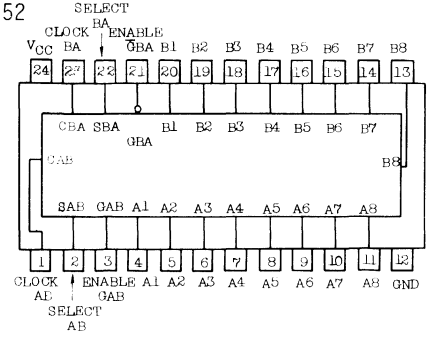
T651



OCTAL BUS TRANSCEIVERS REGISTER (3-STATE)

652

T652



MULTIVIBRATOR

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 123	DUAL MONOSTABLE MULTIVIBRATOR	LS123	*4538,*4528	16
74HC 221	DUAL MONOSTABLE MULTIVIBRATOR	LS221	*4538,*4528	16
74HC 423	DUAL MONOSTABLE MULTIVIBRATOR	LS423	*4538,*4528	16
74HC4538	DUAL MONOSTABLE MULTIVIBRATOR	*LS423	4538, 4528	16

* Suggested alternative

MULTIVIBRATOR

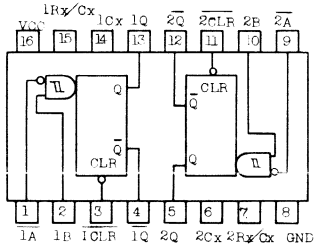
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

123

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎
↓	L	H	⎍	⎎

X : DON'T CARE



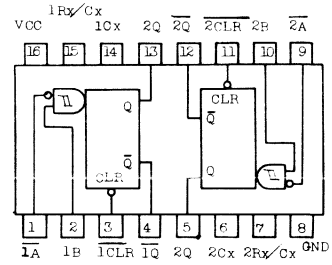
DUAL MONOSTABLE MULTIVIBRATOR

221

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎
↓	L	H	⎍	⎎

X : DON'T CARE



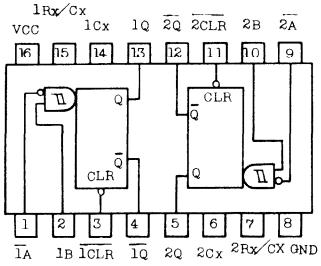
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

423

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎

X : DON'T CARE



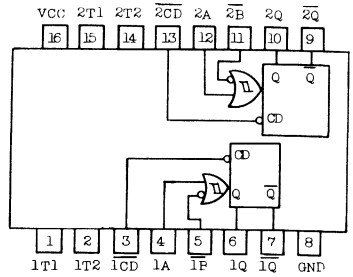
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

4538

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CD}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎

X : DON'T CARE



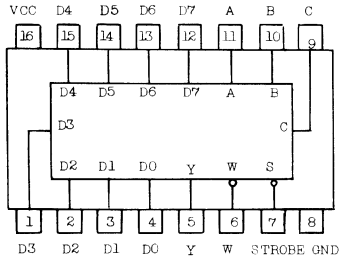
MULTIPLEXER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC4051	8-CHANNEL ANALOG MULTIPLEXER		4051	16
74HC4052	DUAL 4-CHANNEL ANALOG MULTIPLEXER		4052	16
74HC4053	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER		4053	16
74HC4066	QUAD BILATERAL SWITCH		4016,4066	14
74HC 151	8-CHANNEL MULTIPLEXER	LS151	*4512	16
74HC 153	DUAL 4-CHANNEL MULTIPLEXER	LS153	4539	16
74HC 157	QUAD 2-CHANNEL MULTIPLEXER	LS157		16
74HC 158	QUAD 2-CHANNEL MULTIPLEXER (INVERTING)	LS158		16
74HC 251	8-CHANNEL MULTIPLEXER (3-STATE)	LS251	*4512	16
74HC 253	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	LS253	*4539	16
74HC 257	QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	LS257		16
74HC 258	QUAD 2-CHANNEL MULTIPLEXER (3-STATE INVERTING)	LS258		16
74HC 298	QUAD 2-CHANNEL MULTIPLEXER/REGISTER	LS298		16
74HC 354	8-CHANNEL MULTIPLEXER/REGISTER	LS354	*4512	20
74HC 356	8-CHANNEL MULTIPLEXER/REGISTER	LS356	*4512	20

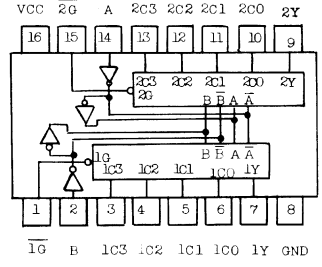
* Suggested alternative

MULTIPLEXER

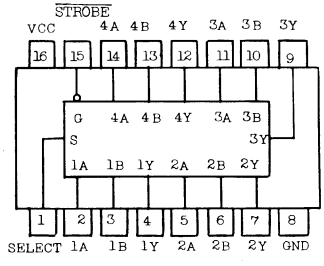
8-CHANNEL MULTIPLEXER
151



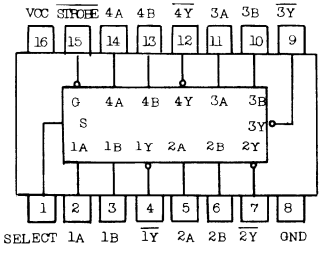
DUAL 4-CHANNEL MULTIPLEXER
153



QUAD 2-CHANNEL MULTIPLEXER
157 NONINVERTED DATA OUTPUTS



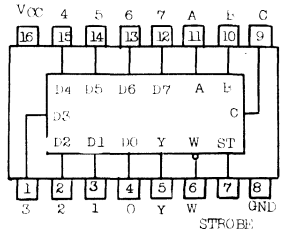
QUAD 2-CHANNEL MULTIPLEXER
158 INVERTED DATA OUTPUTS



MULTIPLEXER (Continued)

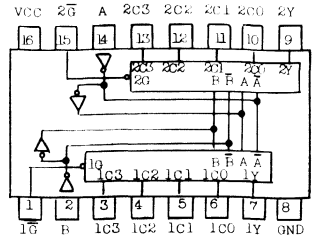
8-CHANNEL MULTIPLEXER (3-STATE)

251



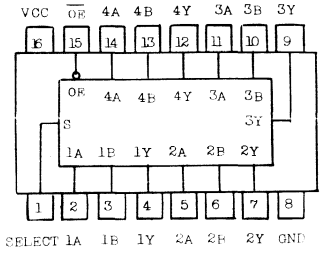
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)

253



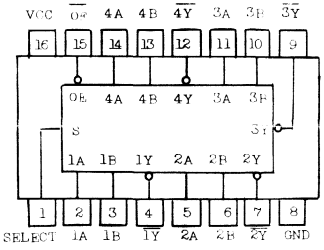
QUAD 2-CHANNEL MULTIPLEXER (3-STATE)

257 NONINVERTED DATA OUTPUTS



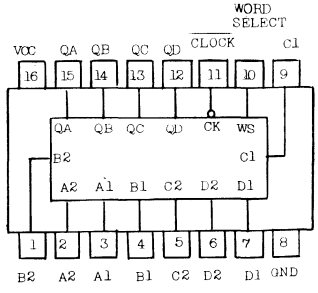
QUAD 2-CNANNEL MULTIPLEXER (3-STATE)

258 INVERTED DATA OUTPUTS



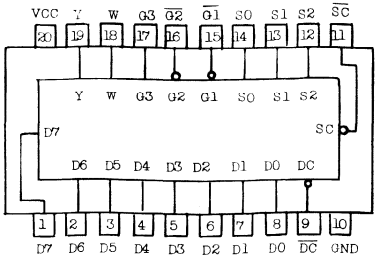
QUAD 2-CHANNEL MULTIPLEXERS WITH OUTPUT REGISTER

298



8-CHANNEL MULTIPLEXER WITH LATCH (3-STATE)

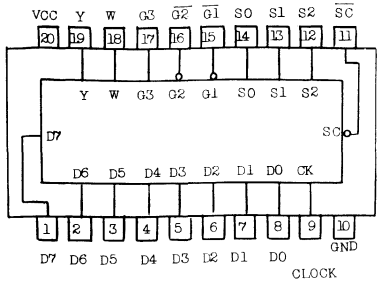
354



MULTIPLEXER (Continued)

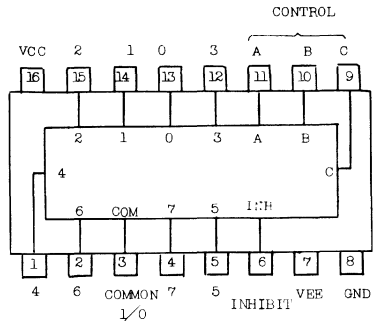
8-CHANNEL MULTIPLEXER WITH FLIP-FLOP (3-STATE)

356



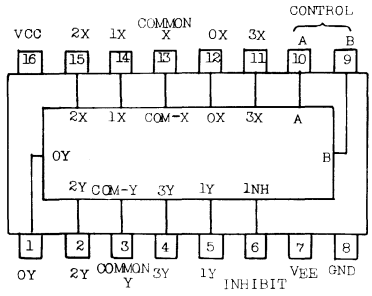
8-CHANNEL ANALOG MULTIPLEXER

4051



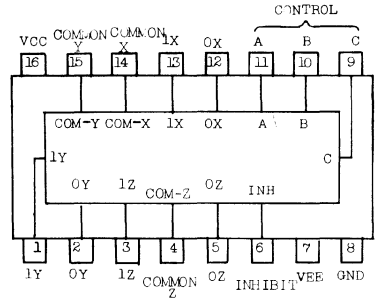
DUAL 4-CHANNEL ANALOG MULTIPLEXER

4052



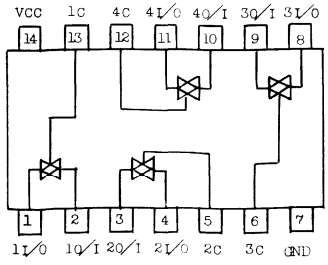
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER

4053



QUAD BILATERAL SWITCH

4066



COUNTER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 161	SYNC. BINARY COUNTER WITH ASYNC. CLEAR	LS161A	40161	16
74HC 163	SYNC. BINARY COUNTER WITH SYNC. CLEAR	LS163A	40163	16
74HC 191	4-BIT BINARY UP/DOWN COUNTER	LS191	*4516	16
74HC 193	SYNC. UP/DOWN BINARY COUNTER	LS193	40193	16
74HC 393	DUAL BINARY COUNTER	LS393	*4520	14
74HC 590	8-BIT BINARY COUNTER/REGISTER (3-STATE)	LS590		16
74HC 592	8-BIT REGISTER/BINARY COUNTER	LS592		16
74HC 593	8-BIT REGISTER/BINARY COUNTER (3-STATE)	LS593		20
74HC 691	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS691		20
74HC 693	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS693		20
74HC 697	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS697		20
74HC 699	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS699		20
74HC4520	DUAL 4-BIT BINARY COUNTER		4520	16
74HC 160	SYNC. DECADE COUNTER WITH ASYNC. CLEAR	LS160A	40160	16
74HC 162	SYNC. DECADE COUNTER WITH SYNC. CLEAR	LS162A	40162	16
74HC 190	BCD UP/DOWN COUNTER	LS190	*4510	16
74HC 192	SYNC. UP/DOWN DECADE COUNTER	LS192	40192	16
74HC 390	DUAL DECADE COUNTER	LS390		16
74HC 690	DECADE COUNTER REGISTER (3-STATE)	LS690		20
74HC 692	DECADE COUNTER REGISTER (3-STATE)	LS692		20
74HC 696	U/D DECADE COUNTER/REGISTER (3-STATE)	LS696		20
74HC 698	U/D DECADE COUNTER/REGISTER (3-STATE)	LS698		20
74HC4518	DUAL DECADE COUNTER		4518	16
74HC4017	DECADE COUNTER/DIVIDER		4017	16
74HC4020	14-STAGE BINARY COUNTER		4020	16
74HC4022	OCTAL COUNTER/DIVIDER		4022	16
74HC4024	7-STAGE BINARY COUNTER		4024	14
74HC4040	12-STAGE BINARY COUNTER		4040	16
74HC4060	14-STAGE BINARY COUNTER/OSCILLATOR			16
74HC40102	DUAL BCD PROGRAMMABLE DOWN COUNTER		40102	16
74HC40103	8-BIT BINARY PROGRAMMABLE DOWN COUNTER		40103	16
74HC7292	PROGRAMMABLE DIVIDER/TIMER	*LS292		16
74HC7294	PROGRAMMABLE DIVIDER/TIMER	*LS294		16

* Suggested alternative

COUNTER

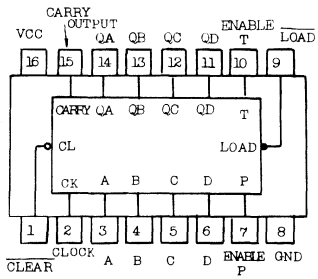
PRESETTABLE 4-BIT COUNTER

160 DECADE, ASYNCHRONOUS CLEAR

161 BINARY, ASYNCHRONOUS CLEAR

162 DECADE, SYNCHRONOUS CLEAR

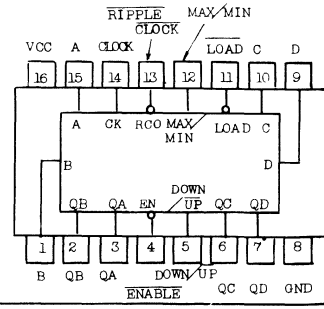
163 BINARY, SYNCHRONOUS CLEAR



SYN. 4-BIT UP/DOWN COUNTER

190 BCD

191 BINARY

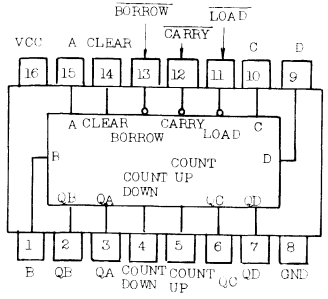


COUNTER (Continued)

SYNC. 4-BIT UP/DOWN COUNTER

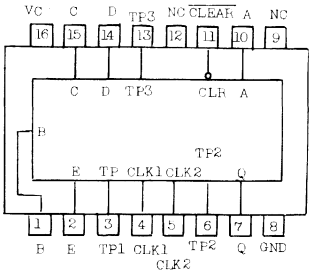
192 BCD

193 BINARY



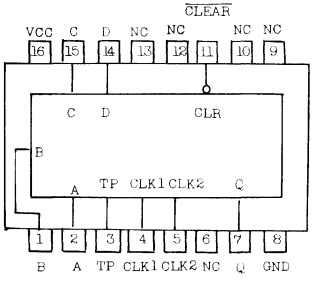
PROGRAMMABLE DIVIDER/TIMER

7292 FROM 2^2 to 2^{31}



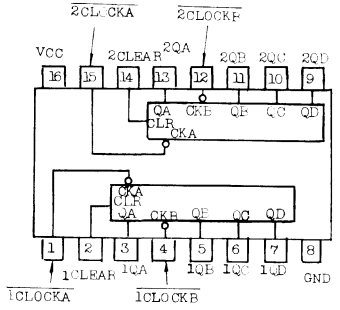
PROGRAMMALBE DIVIDER/TIMER

7294 FROM 2^2 to 2^{15}



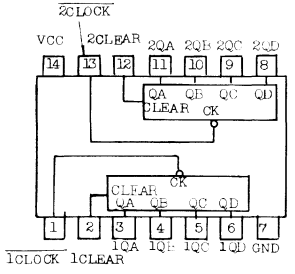
DUAL DECADE COUNTER

390 (BI-QUINARY OR BCD)



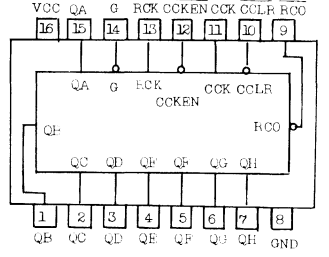
DUAL 4-BIT BINARY COUNTER

393



8-BIT BINARY COUNTER WITH OUTPUT REGISTER (3-STATE)

590



COUNTER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 161	SYNC. BINARY COUNTER WITH ASYNC. CLEAR	LS161A	40161	16
74HC 163	SYNC. BINARY COUNTER WITH SYNC. CLEAR	LS163A	40163	16
74HC 191	4-BIT BINARY UP/DOWN COUNTER	LS191	*4516	16
74HC 193	SYNC. UP/DOWN BINARY COUNTER	LS193	40193	16
74HC 393	DUAL BINARY COUNTER	LS393	*4520	14
74HC 590	8-BIT BINARY COUNTER/REGISTER (3-STATE)	LS590		16
74HC 592	8-BIT REGISTER/BINARY COUNTER	LS592		16
74HC 593	8-BIT REGISTER/BINARY COUNTER (3-STATE)	LS593		20
74HC 691	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS691		20
74HC 693	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS693		20
74HC 697	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS697		20
74HC 699	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS699		20
74HC4520	DUAL 4-BIT BINARY COUNTER		4520	16
74HC 160	SYNC. DECADE COUNTER WITH ASYNC. CLEAR	LS160A	40160	16
74HC 162	SYNC. DECADE COUNTER WITH SYNC. CLEAR	LS162A	40162	16
74HC 190	BCD UP/DOWN COUNTER	LS190	*4510	16
74HC 192	SYNC. UP/DOWN DECADE COUNTER	LS192	40192	16
74HC 390	DUAL DECADE COUNTER	LS390		16
74HC 690	DECADE COUNTER REGISTER (3-STATE)	LS690		20
74HC 692	DECADE COUNTER REGISTER (3-STATE)	LS692		20
74HC 696	U/D DECADE COUNTER/REGISTER (3-STATE)	LS696		20
74HC 698	U/D DECADE COUNTER/REGISTER (3-STATE)	LS698		20
74HC4518	DUAL DECADE COUNTER		4518	16
74HC4017	DECADE COUNTER/DIVIDER		4017	16
74HC4020	14-STAGE BINARY COUNTER		4020	16
74HC4022	OCTAL COUNTER/DIVIDER		4022	16
74HC4024	7-STAGE BINARY COUNTER		4024	14
74HC4040	12-STAGE BINARY COUNTER		4040	16
74HC4060	14-STAGE BINARY COUNTER/OSCILLATOR			16
74HC40102	DUAL BCD PROGRAMMABLE DOWN COUNTER		40102	16
74HC40103	8-BIT BINARY PROGRAMMABLE DOWN COUNTER		40103	16
74HC7292	PROGRAMMABLE DIVIDER/TIMER	*LS292		16
74HC7294	PROGRAMMABLE DIVIDER/TIMER	*LS294		16

* Suggested alternative

COUNTER

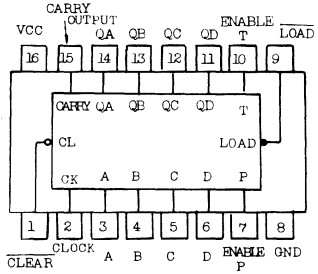
PRESETTABLE 4-BIT COUNTER

160 DECADE, ASYNCHRONOUS CLEAR

161 BINARY, ASYNCHRONOUS CLEAR

162 DECADE, SYNCHRONOUS CLEAR

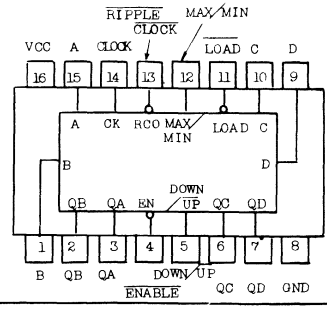
163 BINARY, SYNCHRONOUS CLEAR



SYN. 4-BIT UP/DOWN COUNTER

190 BCD

191 BINARY

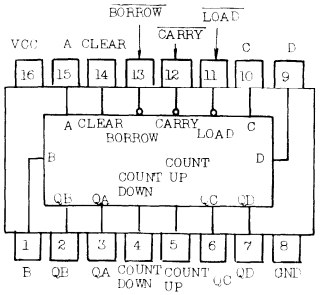


COUNTER (Continued)

SYNC. 4-BIT UP/DOWN COUNTER

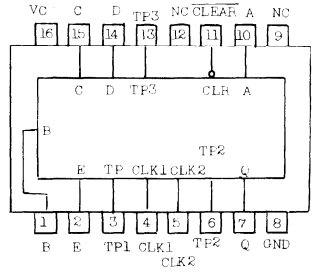
192 BCD

193 BINARY



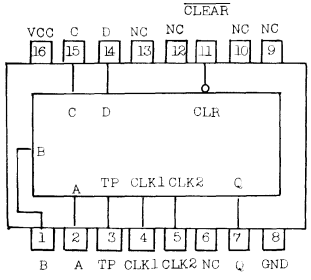
PROGRAMMABLE DIVIDER/TIMER

7292 FROM 2^2 to 2^{31}



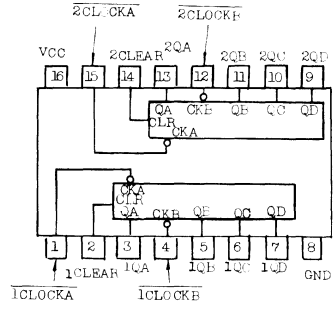
PROGRAMMALBE DIVIDER/TIMER

7294 FROM 2^2 to 2^{15}



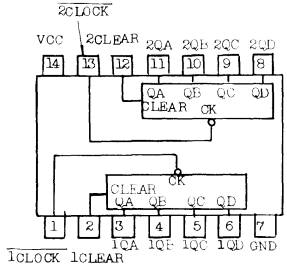
DUAL DECADE COUNTER

390 (BI-QUINARY OR BCD)



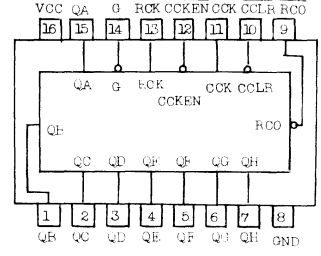
DUAL 4-BIT BINARY COUNTER

393



8-BIT BINARY COUNTER WITH OUTPUT REGISTER (3-STATE)

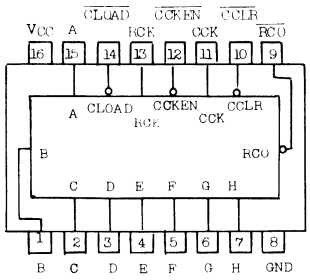
590



COUNTER (Continued)

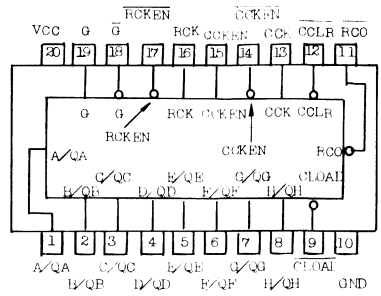
8-BIT BINARY COUNTER WITH INPUT REGISTER

592



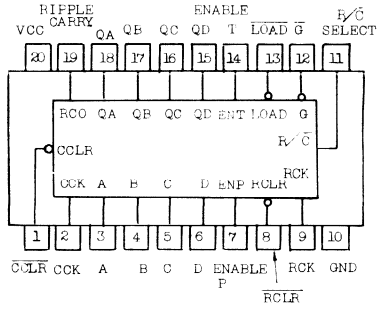
8-BIT BINARY COUNTER WITH INPUT REGISTER (MULTIPLEXED 3-STATE OUTPUTS)

593



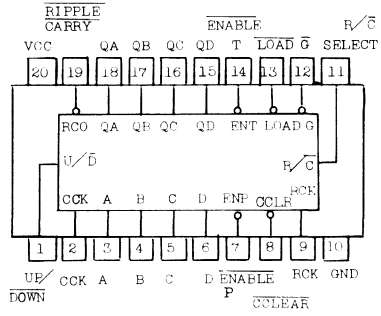
SYNCHRONOUS COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUT

690 DECADE, DIRECT CLEAR
691 BINARY, DIRECT CLEAR
692 DECADE, SYNCHRONOUS CLEAR
693 BINARY, SYNCHRONOUS CLEAR



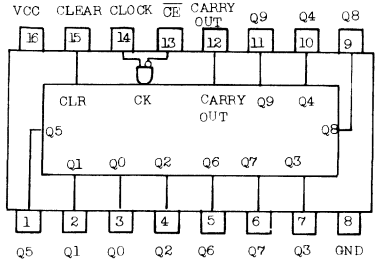
SYNCHRONOUS UP/DOWN COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUTS

696 DECADE, DIRECT CLEAR
697 BINARY, DIRECT CLEAR
698 DECADE, SYNCHRONOUS CLEAR
699 BINARY, SYNCHRONOUS CLEAR



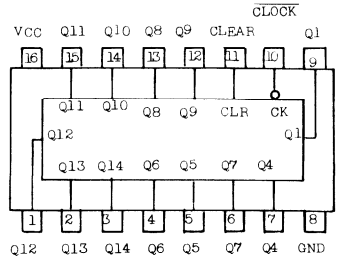
DECADE COUNTER/DIVIDER

4017



14-STAGE BINARY COUNTER

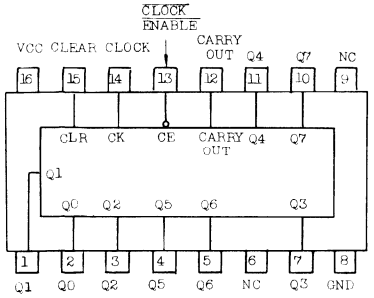
4020



COUNTER (Continued)

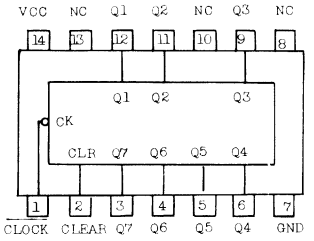
OCTAL COUNTER/DIVIDER

4022



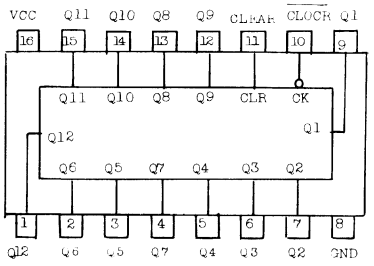
7-STAGE BINARY COUNTER

4024



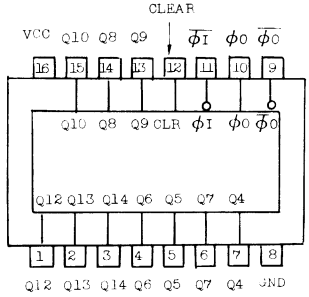
12-STAGE BINARY COUNTER

4040



14-STAGE BINARY COUNTER/OSCILLATOR

4060

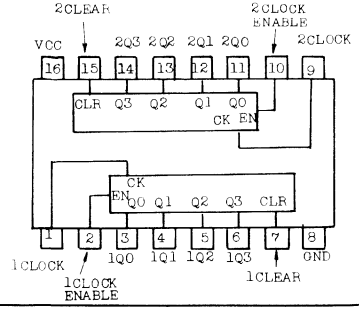


DUAL DECADE COUNTER

4518

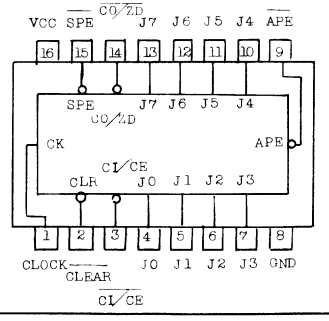
DUAL BINARY COUNTER

4520



PROGRAMMABLE DOWN COUNTER

40102 DUAL BCD
40103 8-BIT BINARY



ENCODER

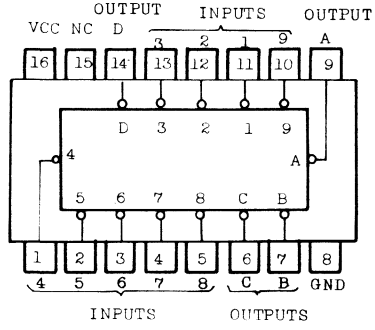
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 147	10-TO-4 LINE PRIORITY ENCODER	LS147		16
74HC 148	8-TO-3 LINE PRIORITY ENCODER	LS148	*4532	16

* SUGGESTED ALTERNATIVE

ENCODER

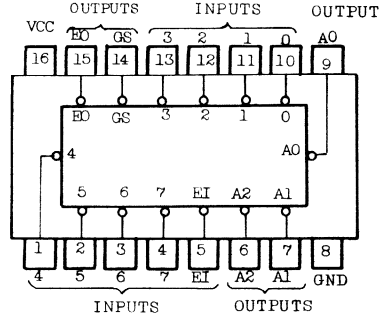
10-TO-4 LINE PRIORITY ENCODER

147



8-TO-3 LINE PRIORITY ENCODER

148



DECODER

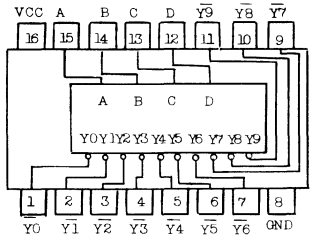
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 42	BCD TO DECIMAL DECODER	LS42	*4028	16
74HC 131	3-TO-8 LINE DECODER/LATCH	LS131		16
74HC 137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HCT137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HC 138	3-TO-8 LINE DECODER	LS138		16
74HCT138	3-TO-8 LINE DECODER	LS138		16
74HC 139	DUAL 2-TO-4 LINE DECODER	LS139	4556,*4555	16
74HC 154	4-TO-16 LINE DECODER	LS154	*4515	24
74HC 155	DUAL 2-TO-4 LINE DECODER	LS155	*4556,*4555	16
74HC 237	3-TO-8 LINE DECODER/LATCH			16
74HC 238	3-TO-8 LINE DECODER			16
74HC4028	BCD-TO DECIMAL DECODER		4028	16
74HC4514	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4514	24
74HC4515	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4515	24
74HC4511	BCD TO 7 SEGMENT L/D/D (LED)	*LS47,*LS48,*LS49	4511	16
74HC4543	BCD TO 7 SEGMENT L/D/D (LCD)	*LS47,*LS48,*LS49	4543	16

* Suggested alternative

DECODER

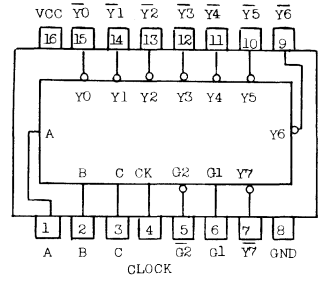
BCD TO DECIMAL DECODER

42



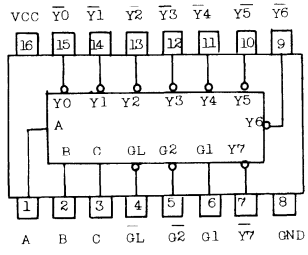
3-TO-8 LINE DECODER/LATCH

131



3-TO-8 LINE DECODER/LATCH

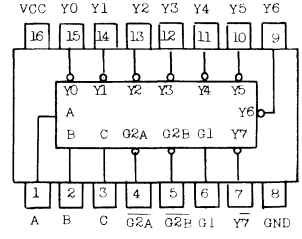
137



3-TO-8 LINE DECODER

138

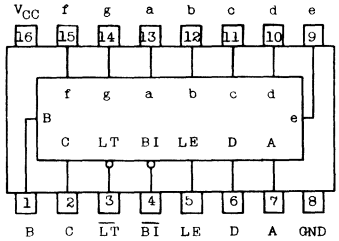
T138



DECODER (Continued)

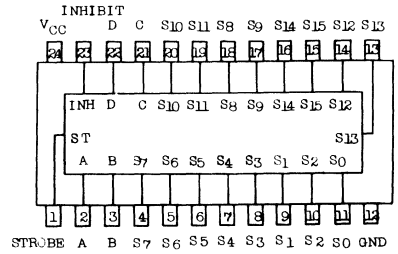
BCD TO 7 SEGMENT LATCH/DECODER/DRIVER

4511



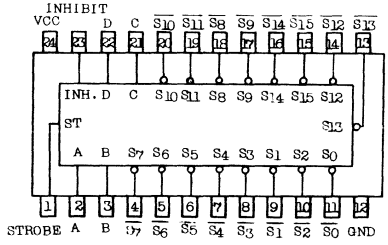
4-TO-16 LINE DECODER/LATCH

4514



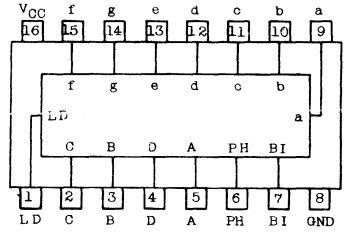
4-TO-16 LINE DECODER/LATCH

4515



BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

4543



ALU

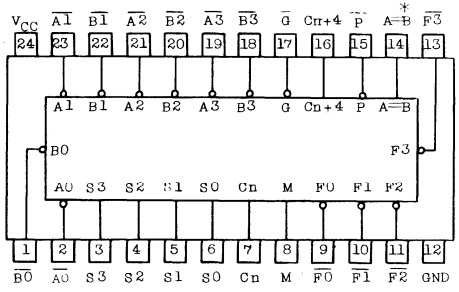
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 181	ARITHMETIC LOGIC UNIT	LS181		24
74HC 182	LOOK AHEAD CARRY LOGIC	LS182		16

ALU

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

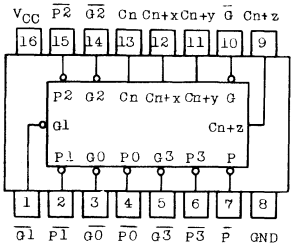
181

* : OPEN DRAIN OUTPUT



LOCK AHEAD CARRY GENERATOR

182



PARITY TREE

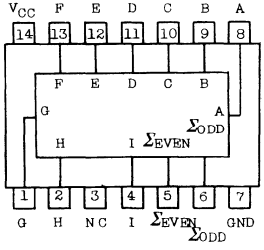
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC280	9-BIT PARITY GENERATOR/CHECKER	LS280	*4531	14

* Suggested alternative

PARITY TREE

9-BIT ODD/EVEN PARITY GENERATOR/ CHECKER

280



LATCH

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 75	4-BIT D-TYPE LATCH	LS75	*4042	16
74HC 77	4-BIT D-TYPE LATCH	LS77	*4042	14
74HC 259	8-BIT ADDRESSABLE LATCH	LS259	*4099	16
74HC 279	QUAD $\overline{S}$-$\overline{R}$ LATCH	LS279	*4043,*4044	16
74HC 375	QUAD D-TYPE LATCH	LS375		16
74HC 373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HC 533	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS533		20
74HC 563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HCT563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HC 573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20

* Suggested alternative

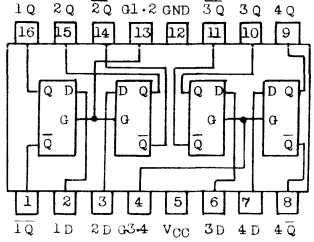
LATCH

4-BIT LATCH
75

FUNCTION TABLE

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE

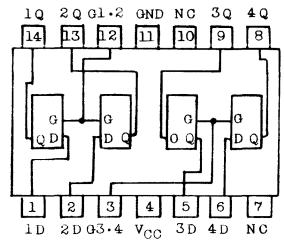


4-BIT LATCH
77

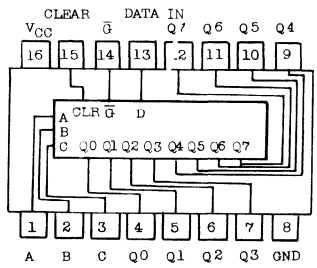
FUNCTION TABLE

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE



8-BIT ADDRESSABLE LATCH
259

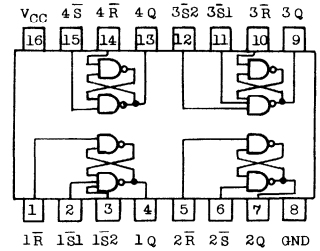


QUAD $\overline{S}$-$\overline{R}$ LATCH
279

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{S}$*	$\overline{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

* FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:
H=BOTH $\overline{S}$ INPUTS HIGH
L=ONE OF BOTH INPUTS LOW

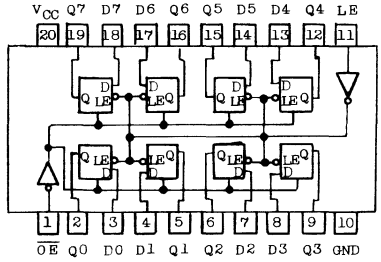


LATCH (Continued)

OCTAL LATCH (3-STATE)

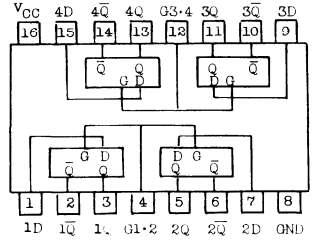
373 NONINVERTED DATA OUTPUTS

T373



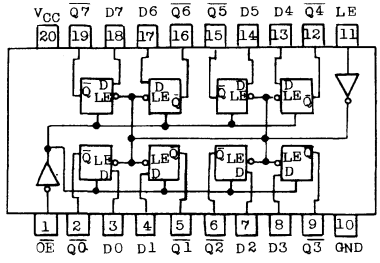
QUAD LATCH

375



OCTAL LATCH (3-STATE)

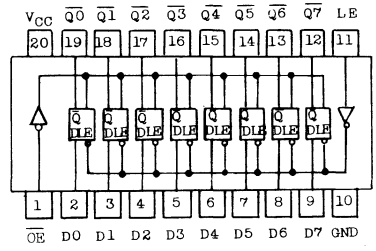
533 INVERTED DATA OUTPUTS



OCTAL LATCH (3-STATE)

563 INVERTED DATA OUTPUTS

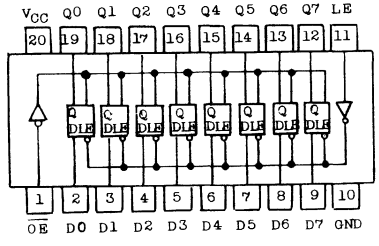
T563



OCTAL LATCH (3-STATE)

573 NONINVERTED DATA OUTPUTS

T573



REGISTER

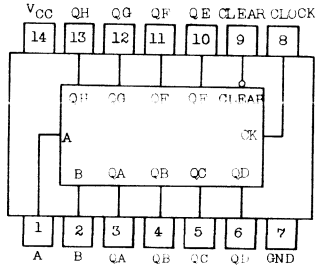
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 164	8-BIT SIPO SHIFT REGISTER	LS164	*4034	14
74HC 165	8-BIT PISO SHIFT REGISTER	LS165	*4014,*4021	16
74HC 166	8-BIT PISO SHIFT REGISTER	LS166	*4014,*4021	16
74HC 173	QUAD D-TYPE REGISTER (3-STATE)	LS173	4076	16
74HC 194	4-BIT PIPO SHIFT REGISTER	LS194A	40194,*40104	16
74HC 195	4-BIT PIPO SHIFT REGISTER	LS195A	*4035	16
74HC 299	8-BIT PIPO SHIFT REGISTER	LS299	*4034	20
74HC 323	8-BIT PIPO SHIFT REGISTER	LS323	*4034	20
74HC 595	8-BIT SHIFT REGISTER/LATCH (3-STATE)	LS595		16
74HC 597	8-BIT LATCH/SHIFT REGISTER	LS597		16
74HC 670	4 WORD × 4-BIT REGISTER FILE(3-STATE)	LS670		16
74HC4094	8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)		4094	16

* Suggested alternative

REGISTER

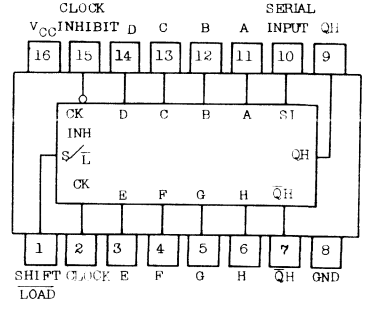
8-BIT SERIAL-IN/PARALLEL OUT SHIFT REGISTER

164



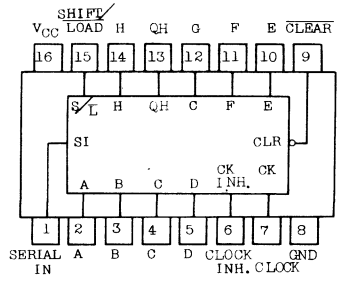
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

165



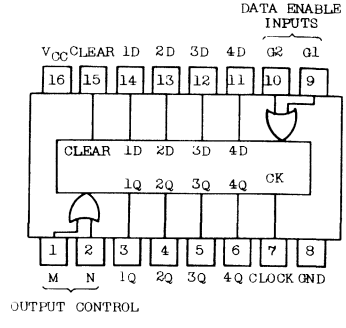
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

166



QUAD D FLIP-FLOP (3-STATE)

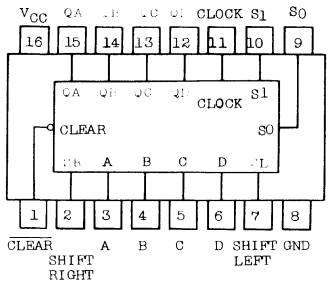
173



REGISTER (Continued)

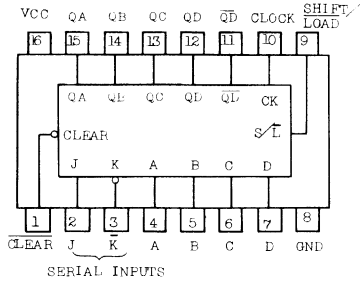
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

194



4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

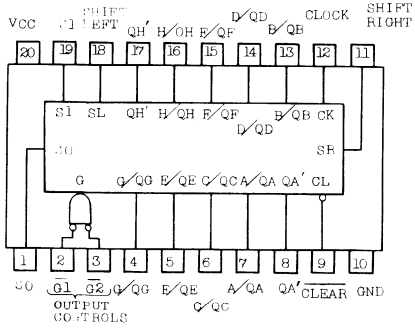
195



8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER (3-STATE)

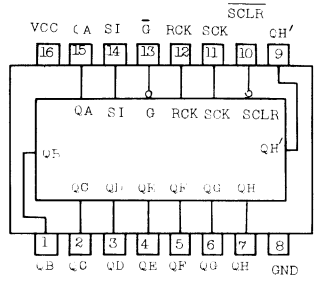
299 DIRECT CLEAR

323 SYNCHRONOUS CLEAR



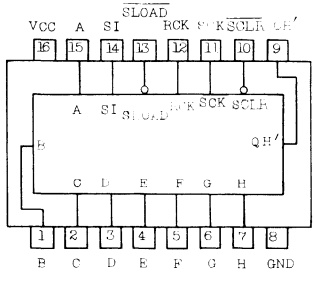
8-BIT SHIFT REGISTER/LATCH (3-STATE)

595



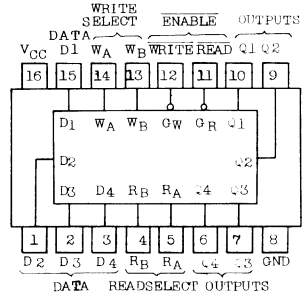
8-BIT LATCH/SHIFT REGISTER

597



4 WORD x 4 BIT REGISTER FILE(3-STATE)

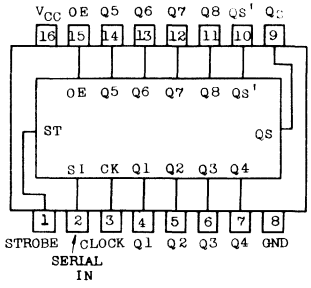
670



REGISTER (Continued)

8-BIT SERIAL IN/PARALLEL-OUT SHIFT REGISTER/LATCH (3-STATE)

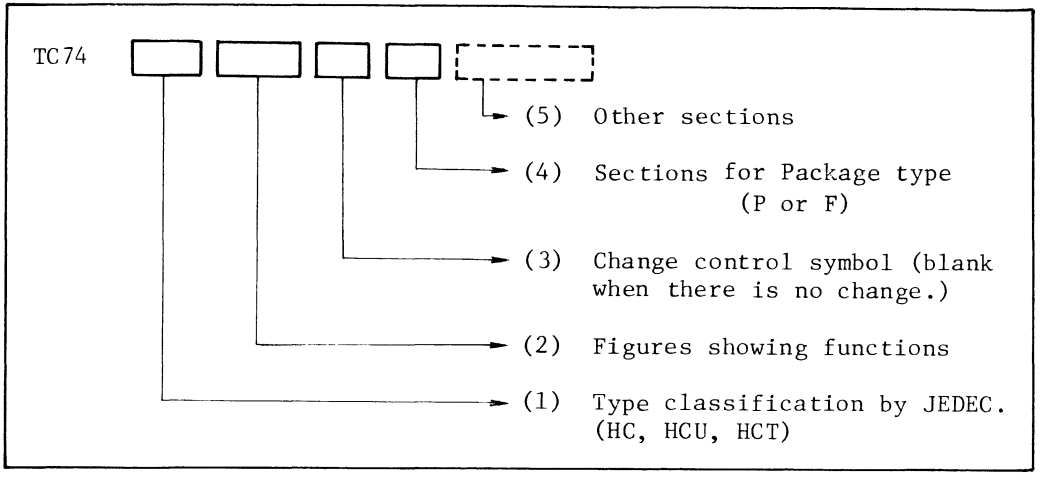
4094



3. OUTLINE OF PRODUCTS

3.1 Naming Method of TC74HC Series

TC74HC Series was named by the standard naming method of JEDEC.
Its formal type number is as shown below.



(Example) TC74HCT240F

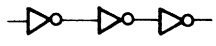
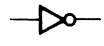
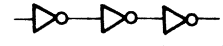
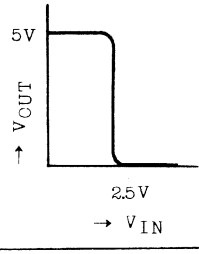
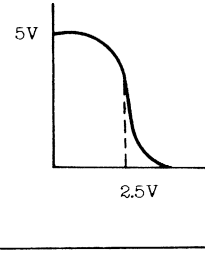
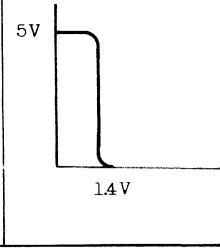
High speed C^2MOS IC which is pin and functionally compatible with the bipolar 74LS240 device.
Input is designed with TTL level, and direct driving from LSTTL is possible.
Package type is plastic Mini Flat Package.

(1) HC, HCU, HCT

In the high speed CMOS, HC series, there are HCU type and HCT type beside the fundamental HC type. These sections were decided by JEDEC in order to prevent the difference in electrical performance produced by input level and existence of buffer even in the case of CMOS of same function.

Type	Internal stage	Input threshold voltage
HC	Two stages and above	CMOS level
HCU	One stage	CMOS level
HCT	Two stages and above	TTL level

Taking inverter as an example, we can show the difference of these types as follows.

	TC74HC04	TC74HCU04	TC74HCT04
Logic Diagram			
Input-Output Voltage transfer characteristics			

(2) Classification of functions

Functions are expressed by English numerals of two to five figures. In the case of TC74HC Series, there are provided the product having same pin connection and function with LSTTL, and the product having same pin connection and function with 4000B/4500B series of standard CMOS.

00 ∿ 999 ..... Product of same pin connection and same function with 74LS series.

(Example) 74LS240 ↔ 74HC240

4000∿40199 .... Product of same pin connection and same
4500∿4599 function with standard CMOS 4000B/4500B series.

(Example) 40102B ↔ 74HC40102

7000 7999 ..... Function proper to 74HC series. However, some function approaches LSTTL.

(Example) Same function with 74HC7266 ↔ 74LS266.
However, output is of normal buffer structure.
(not open drain structure.)

(3) Change control symbol

This symbol is given to clarify the revision of product when improvement which will remarkably change the characteristics of product is made. Normally, it is blank, but if there is a change, English characters are given successively from A.

(4) Partition for package designator

English characters showing type of package.

P ..... dual in line package (DIP) Plastic
F ..... mini flat package (MFP) Plastic

In TC74HC series, narrow 300 mill type 24 pin package was newly developed. By this development, in the case of "P" type, 14/16/20/24/pins are all unified into 300 mill width (7.62 mm width).

Also, in the case of mini flat "F" type, 14/16/20 pins are all unified into EIAJ 300 mill type package (TYPE II, Form A).

In the case of both DIP and MFP types, pin arrangement of same width and same pitch is adopted regardless of pin number, and so it is possible to arrange the parts systematically when designing the printed board, and automatic mounting can be easily made.

(5) Other partitions

In the case of mini flat IC Taping specification, the following indication is added to the parts name.

- TP1 or - TP2 (Difference in sticking direction)

3-2. Features

TC74HC Series has the following features in comparison with other standard Logic IC.

(1) High Speed operation : Same as LSTTL

(2) Low Power Dissipation: Same as standard CMOS series (μW)

(3) Output Drive Capability: Capable of directly driving 10 LSTTL loads (Standard output type).

Capable of directly driving 15 LSTTL loads (Buffer output type).

(4) High Noise Immunity : HC/HCU Type ... 45% V_{CC} (Typ.)
HCT Type ..... 25% V_{CC} (Typ.)

(5) Wide Operating Voltage Range :
HC/HCU Type ... 2 to 6V
HCT Type ..... 4.5 to 5.5V

(6) Wide Operating Temperature Range : -40 to +85°C

(7) Self-contained static electricity protective circuit:
±200V (min) (All inputs and Outputs)
by EIAJ method

(8) Ample Latch up Capacity: Total input ±70mA and above (Restricted by input protective resistance)
Total output ±300 mA and above.

(9) Based on the same pin connection and function with LSTTL.

(10) Wide Line up, and products amounting to 180 kinds.

Table 3-1 shows comparison of characteristics of various logic families.

Table 3-1 Performance Comparison of Each Logic Family

Parameter		HS-C^{2}MOS (TC74HC series)	LSTTL	HS-C^{2}MOS (TC40H series)	C^{2}MOS	Condition
Propagation delay time GATE(C_L=15pF)		8ns typ	9ns typ	15ns typ	125ns typ	V_{DD} = 5.0V
Maximum clock freqency J/KF·F(C_L=15pF)		60MHz typ	45MHz typ	20MHz typ	2MHz typ	Ta = 25°C
Quiescent Supply Current (GATE)		0.01μW typ	8mW typ	0.01μW typ	0.01μW typ	Total temperature voltage range
Input Voltage	VIH	3.5Vmin	2.0Vmin	4.0Vmin	3.5Vmin	V_{DD}=5.0V
	VIL	1.5Vmax	0.8Vmax	1.0Vmax	1.5Vmax	Total temperature range

Parameter		HS-C²MOS (TC74HC series)	LSTTL	HS-C²MOS (TC40H series)	C²MOS	Condition
Output Current	$\|I_{OH}\|$	4mA min*1	0.4mA min*2	0.36mA min*3	0.12mA min*3	*1 V_{CC}=4.5V *2 V_{CC}=4.75V *3 V_{CC}=5V Total temperature range
	I_{OL}	4mA min	4mA min	0.8mA min	0.36mA min	
Operating Voltage Range		2 ∿ 6V	4.75∿5.25V	2 ∿ 8V	3 ∿ 18V	
Operating Temperature Range		-40 ∿ 85°C	0 ∿ 70°C	-40 ∿ 85°C	-40∿85°C	

4. EXPLANATIONS OF RATINGS AND STANDARDS

4-1. Maximum Ratings

Regarding C MOS IC, the maximum Rating is regulated for each product.

In general, the maximum rating value should not be exceeded in order to guarantee the life and reliability of integrated circuit products. Here is adopted the notion of absolute maximum rating as the maximum rating.

Absolute Maximum Rating should not be exceeded even for a moment, and any one standard of ratings should not be exceeded.
When the unit is used in excess of the maximum rating, the characteristic will not recover sometimes, and in an extreme case, permanent breakage will be caused.

In designing the circuit, therefore, it is necessary to pay attention to the fluctuation of supply voltage, characteristics of connecting parts, ambient temperature, and surge of input and output siganl line, so that the maximum rating not be exceeded.

Table 4-1 indicates common maximum ratings of TC74HC series.

When the maximum rating of each unit and common rating differ, the former shall control. As for the meaning of each item, refer to Table 4-2.

Table 4-1 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25 (Standard) ±35 (Buffer)	mA
DC VCC/GND Current	I_{CC}	±50 (Standard) ±70 (Buffer)	mA
Power Dissipation	P_D	500 (DIP)* 180 (MFP)	mW
Storage Temperature	T_{STG}	-65 ∿ 150	°C
Lead Temperature (10sec)	T_L	300	°C

* 500mW in the range of Ta = 40°C ∿ 65°C. In the range of Ta = 65°C to 85°C, derating factor of -10mW/°C shall be applied until 300mW.

Table 4-2

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	Indicates the voltage range in which IC does not cause breakage, deterioration of characteristics and fall of reliability when voltage is impressed on V_{CC} terminal.
DC Inpunt Voltage DC Output Voltage	V_{IN} V_{OUT}	Indicates the voltage range in which IC does not cause breakage, deterioration of characteristics and fall of reliability when voltage is impressed on input and output terminals.
Input Diode Current Output Diode Current	I_{IK} I_{OK}	Indicates the current value at which IC does not cause breakage due to latch up when input current or output current is fed. * Practically, the design in which DC current flows is not recommendable. When flow of current cannot be prevented, adopt the current value lower than this.
DC Output Current V_{CC}/GND Current	I_{OUT} I_{CC}	Output current indicates the current value which can be fed for one output. As V_{CC}/GND current includes output current, in the case of IC having many output terminals, substantial output current is controlled by it.
Power Dissipation	P_D	Indicates consumption power not causing breakage of IC in the entire operating temperature range.

Parameter	Sumbol	Explanation
Storage Temperature	Tstg	Indicates the ambient temperature range not causing deterioration of characteristic and fall of reliability when left for a long time in the state not impressed with supply voltage.
Load Temperature Time	T_L	Indicates the conditions when soldering is carried out after IC is mounted on printed board.

4-2. Recommended Operating Conditions

This is the range in which the operation of 74HC series is guaranteed, and when this range is exceeded, the operation is not guaranteed even if it is within the maximum rating of 4-1. Common recommended operating condition of 74HC series is shown in Table 4-3. When recommended operating condition of each unit and common recommended operating condition differs, the former shall control. As for the meaning of each item, refer to Table 4-4.

Table 4-3 Common Recommended Operating Condition

(a) 74HC Type

Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0∿ 500 (V_{CC}=4.5V) 0∿ 400 (V_{CC}=6.0V)	ns

(b) 74HCT Type

Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltate	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Falling Time	t_r, tf	0 ∿ 500	ns

Table 4-4

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	Indicates supply voltage range guaranteeing normal theoretical operation of IC.
Input Voltage Output Voltage	V_{IN} V_{OUT}	Indicates voltage range guaranteeing normal theoretical operation and electric characteristic of IC.
Operating Temperature	Topr	Indicates operating temperature range guaranteeing normal theoretical operation and electric characteristic of IC.
Input Rise and Fall Time	tr, tf	Indicates rising and falling time range of input signal not causing malfunction due to oscillation of output.

4-3. DC characteristics

Table 4-5 shows DC characteristics of HC Type. As for the meaning of each item, refer to Table 4-7. Table 4-5 is a standard DC characteristics Table, and when it differs from individual characteristic, the latter shall control. DC characteristics is regulated by JEDEC (International standards). In TC74HC series, all units satisfy this international standard value, and some items guarantee the characteristics surpassing the international standards. Table 4-6 indicates characteristics Table standardized by JEDEC.

Table 4-5 TC74HC Series DC Characteristics Table

DC Electrical characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C			Ta=-40~85°C		Unit
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
**Low-level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
**High-level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA*	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA*	6.0	5.68	5.80	-	5.63	-	
** Low-level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA*	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA*	6.0	-	0.18	0.26	-	0.33	

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	Unit
3 State Output Off-state Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT}=VCC or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
**Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	-	-	1.0	-	10.0	
			FF	6.0	-	-	2.0	-	20.0	
			MSI	6.0	-	-	4.0	-	40.0	

Note) * Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}| = I_{OL}$ = 6mA, 7.8mA)

** Items guaranteeing the characteristics surpassing JEDEC standards.

Table 4-6 JEDEC Standard No.7

DC Electrical characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	Unit
High-level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2		-	4.2	-	
Low-level Input Voltage	V_{IL}			2.0	-	-	0.3	-	0.3	V
				4.5	-		0.9	-	0.9	
				6.0	-	-	1.2	-	1.2	
High-level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	-	-	1.9	-	V
				4.5	4.4	-	-	4.4	-	
				6.0	5.9	-	-	5.9	-	
			I_{OH}=-4mA*	4.5	3.98	-	-	3.84	-	
			IOH=-5.2mA*	6.0	5.48	-	-	5.34	-	

Parameter	Symbol	Test Condition		VCC	Ta = 25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	Unit
Low-level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	-	0.1	-	0.1	V
				4.5	-	-	0.1	-	0.1	
				6.0	-	-	0.1	-	0.1	
			I_{OL}=4mA*	4.5	-	-	0.33	-	0.37	
			I_{OL}=5.2mA*	6.0	-	-	0.33	-	0.37	
3-state Output Off-leak Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT}= V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	A
Input leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	-	-	2.0	-	20.0	
			FF	6.0	-	-	4.0	-	40.0	
			MSI	6.0	-	-	8.0	-	80.0	

Note) * Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}| = I_{OL}$ = 6mA, 7.8mA)

Table 4-7

Parameter	Symbol	Explanation
High level Input Voltage	V_{IH}	This is an input voltage capable of judging input of IC as "H" level, and the minimum value is guaranteed. Judgement in this case is made by confirming that it is above the prescribed V_{OH} when output voltage should be at "H" level, and below the prescribed V_{OL} when output voltage should be at "L" level.

Parameter	Symbol	Explanation
Low level Input Voltage	V_{IL}	This is an input voltage capable of judging input of IC as "L" level, and the maximum value is guaranteed. In this case, the judging method is same as V_{IH}.
High level Output Voltage	V_{OH}	This is an output voltage when each input terminal is connected to V_{IH} or V_{IL} so that the output level becomes "H". In this case, there is guaranteed the minimum value of output voltage obtainable when the specified output current (I_{OH}) is flown out.
Low level Output Voltage	V_{OL}	This is an output voltage when each input terminal is connected to V_{IH} or V_{IL} so that the output level becomes "L". In this case, there is guaranteed the minimum value of output voltage obtainable when the specified output current (I_{OL}) is flown in.
Input Current	I_{IN}	This is the current flowing in the input terminal when the voltage is impressed on the input terminal of IC. Normally, this current is so small that measurement is made with the maximum value of supply voltage.
3-state Output Off-leak Current	I_{OZ}	This is a leakage current flowing in the output terminal when the output has become high impedance, in the device having three state output terminal or open drain output terminal.

Parameter	Symbol	Explanation
Quiescent Supply Current	I_{CC}	This is a current flowing from V_{CC} terminal into IC when V_{CC} or GND level is held without changing IC input, and the maximum value under all theoretical conditions allowable for measured IC is guaranteed.

4-4. AC Characteristics

AC characteristics guarantees transient characteristic of produts. In general, impressed input waveform is so set as to have amplitude of V_{CC}-GND level and rising and fall time of 6ns. Table 4-8 shows the meaning of each item of AC characteristics, Fig. 4-1 indicates the output connection diagram of measuring time, and Fig. 4-2 illustrates the measured waveform.

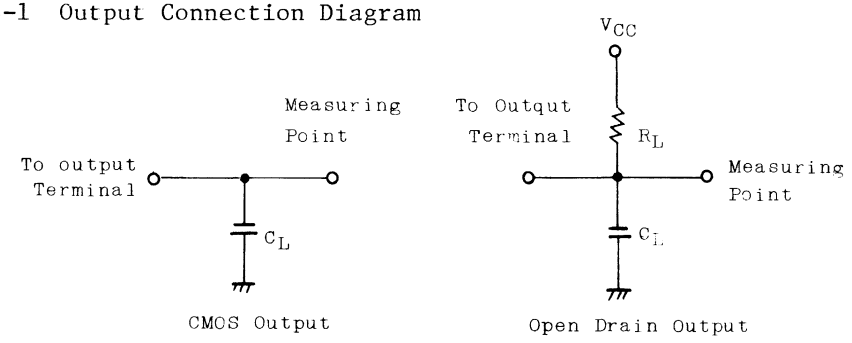
Table 4-8

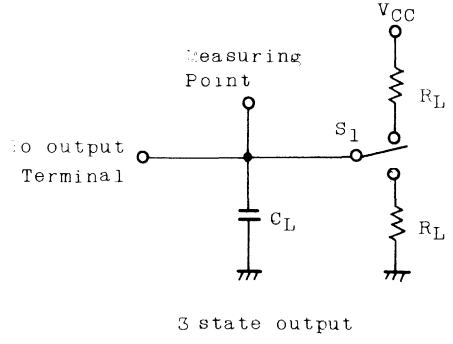
Parameter	Symbol	Explanation	Drawing No.	
			HC	HCT
Output Rising Time Output Falling Time	t_{TLH} t_{THL}	Indicates the time during which the output voltage (V_{OL}, V_{OH}) rises from 10% to 90%, and the time during which the output voltage falls down from 90% to 10%.	(1)-(i)	(2)-(i)

Parameter	Symbol	Explanation	Drawing No. HC	Drawing No. HCT
Propagation Delay Time	t_{pLH} t_{pHL}	Indicates the delay time, i.e., after input signal is given and until output response is made. t_{pLH} is the case in which the output changes from "L" level to "H" level, and t_{pHL} is the case in which the output changes from "H" level to "L"	(1)-(i)	(2)-(i)
Output disable Time	t_{pLZ} t_{pHZ}	Indicates the delay time, i.e., after a signal is given to the output control terminal and until 3 state output becomes high impedance state.	(1)-(iii)	(2)-(iii)
Output Enable Time	t_{pZL} t_{pZH}	Indicates the delay time, i.e., after a signal is given to the output control terminal and until 3 state output becomes "L" level or "H" level from the high impedance state.		
Minimum Set up Time	t_s	Regarding a certain data, indicates the time in which the data must be added and held before the input regarding that data (clock input, etc.) changes. For instance, when the data is read in at a rise of next clock pulse, it is necessary to add data before the rising of clock pulse, maximum value of t_s.	(1)-(ii)	(2)-(ii)
Minimum Hold Time	th	Regarding a certain data, indicates the time in which the data must be held even after the input regarding that data (clock input, etc.) has changed.		

Parameter	Symbol	Explanation	Drawing No.	
			HC	HCT
Minimum Removal Time	t_{rem}	Indicates the minimum time, i.e., after releasing of asynchronous input (clear, preset input, etc.) and until receiving of next operation input (clock, etc.)	(1)-(ii)	(2)-(ii)
Minimum Pulse Width	t_w	Indicates the minimum pulse width at which clock input, etc. is accepted as a normal signal.		
Max. Clock Frequency	f_{MAX}	Indicates a limit clock frequency at which IC carries out normal operaiton.		
Input Capacitance	C_{IN}	Indicates the capacity between input and GND.		

Fig.4-1 Output Connection Diagram



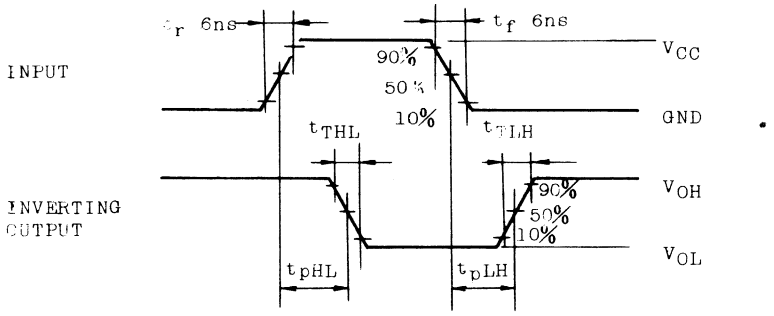


Note) C_L contains the capacity of probe, etc.

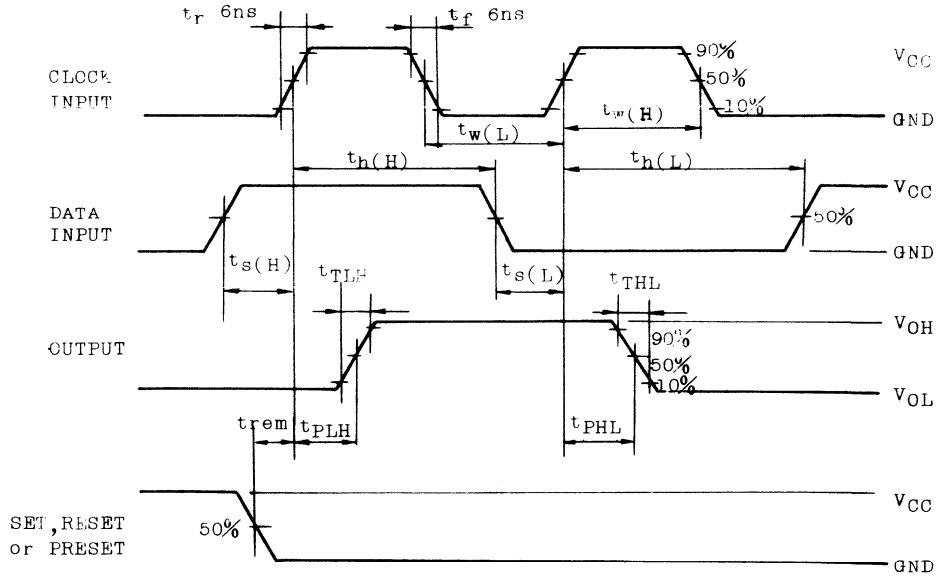
Fig. 4-2 Switching Characteristics Test Waveform

(1) HC Type

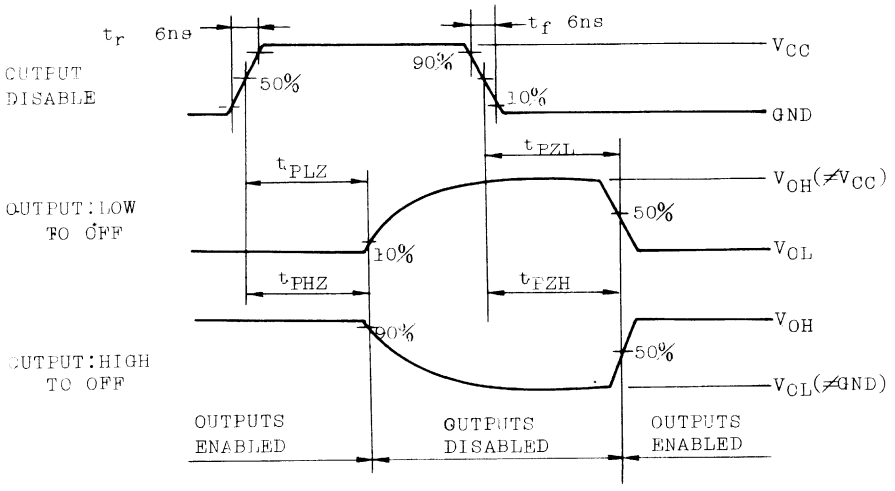
i) t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}



ii) t_w, t_s, t_h, t_{rem}

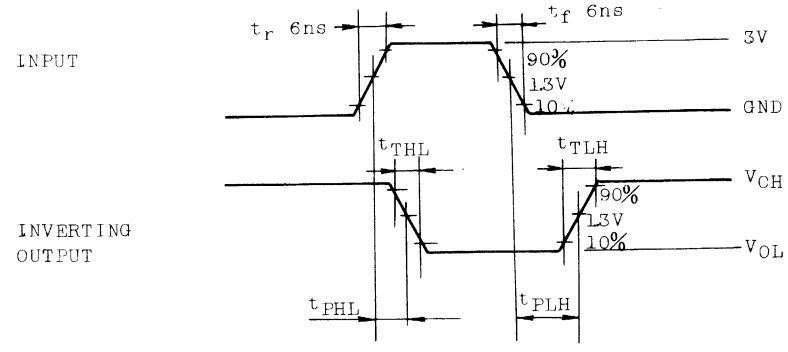


iii) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

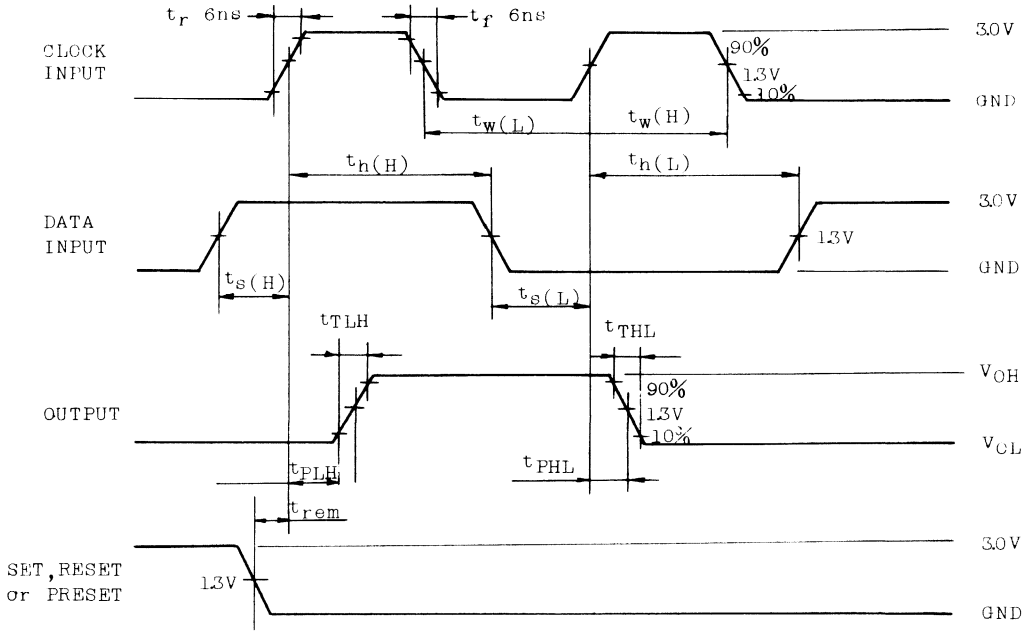


(2) HCT Type

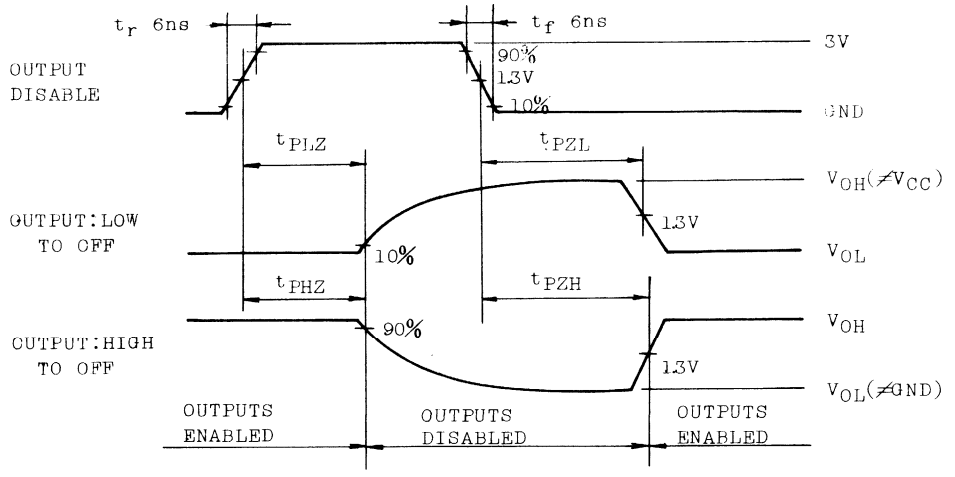
i) t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}



ii) t_w, t_{su}, t_h, t_{rem}



iii) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

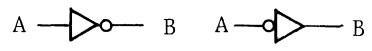
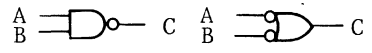
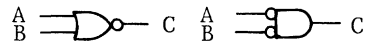
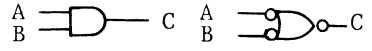
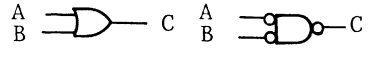
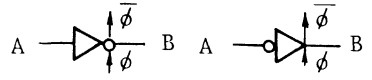
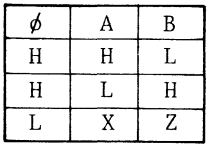
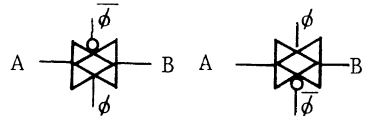
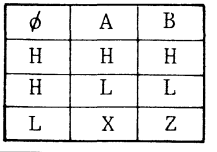
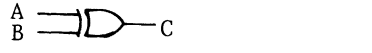


5. HOW TO READ LOGIC SYMBOL AND TRUTH TABLE

5-1. How to read Logic Symbol

Table 5-1 shows the basic logical block used in high-speed CMOS IC. The theoretical chart printed in individual technical data of each product is composed of the basic block shown in the table. This logical chart is based on MIL-STD-806B, and clocked inverter and transmission gate employ specific symbol.

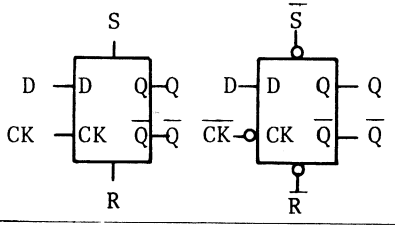
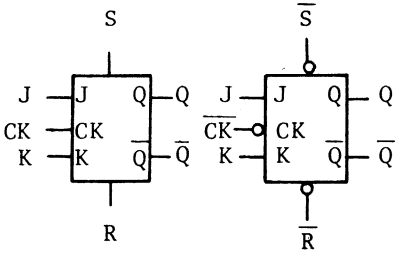
Table 5-1 Basic Logical Circuits

Circuit Function	Logic Symbol	Logical Equation or Truth Table
Inverter		$B = \overline{A}$
NAND Gate		$C = \overline{A \cdot B} = \overline{A} + \overline{B}$
NOR Gate		$C = \overline{A + B} = \overline{A} \cdot \overline{B}$
AND Gate		$C = A \cdot B = \overline{\overline{A} + \overline{B}}$
OR Gate		$C = A + B = \overline{\overline{A} \cdot \overline{B}}$
Clocked Inverter (Note 1)		 X: Don't Care Z: High Impedance
Transmission Gate (Note 2)		 X: Don't Care Z: High Impedance
EXCLUSIVE-OR Gate		$C = (A + B) \cdot (\overline{A} + \overline{B})$

ϕ	A	B
H	H	L
H	L	H
L	X	Z

ϕ	A	B
H	H	H
H	L	L
L	X	Z

Table 5-1 (Continued)

<table>
<tr><th>Circuit Function</th><th>Logic Symbol</th><th>Logical Equation or Truth Table</th></tr>
<tr><td>EXCLUSIVE-NOR Gate</td><td>  </td><td>$C = (A \cdot B) + (\overline{A} \cdot \overline{B})$</td></tr>
<tr><td>D-Type Flip Flop</td><td>  </td><td>
<table>
<tr><th>S</th><th>R</th><th>D</th><th>CK</th><th>Q</th></tr>
<tr><td>H</td><td>L</td><td>X</td><td>X</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>↑</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>↑</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>↓</td><td>QnΔ</td></tr>
</table>
X: Don't Care
Δ: No Change
</td></tr>
<tr><td>J/K Type Flip Flop</td><td>  </td><td>
<table>
<tr><th>S</th><th>R</th><th>J</th><th>K</th><th>CK</th><th>Q</th></tr>
<tr><td>H</td><td>L</td><td>X</td><td>X</td><td>X</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>X</td><td>X</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>↑</td><td>QnΔ</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>↑</td><td>L</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>↑</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>↑</td><td>$\overline{Qn}\nabla$</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>X</td><td>↓</td><td>QnΔ</td></tr>
</table>
X: Don't Care
Δ: No Change
∇: Toggle
</td></tr>
</table>

Note 1) Clocked Inverter

Clocked inverter has the circuit shown in Fig. 5-1. In this figure, Q1 and Q2 are P-channel MOS FET, and Q3 and Q4 are N-channel MOS FET, and four FET are all connected in series from V_{CC} to GND.

If ϕ signal is at "H" level, Q1 and Q4 turn on, and can be regarded as a mere inverter composed of Q2 and Q3.

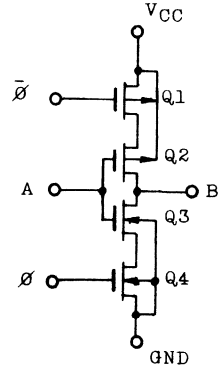


Fig. 5-1 Clocked Inverter

When ϕ signal is at "L" level, both Q_1 and Q_4 turn off, and irrespective of the condition of A input, the output B becomes high impedance condition cut off from both V_{CC} and GND. That is to say, clocked inverter can be applied as a switch to cut off input and output.

Note 2) Transmission Gate

Transmission gate has the circuit shown in Fig. 5-2. As shown in this figure, Q_1 is P channel MOS FET and Q_2 is N channel MOS FET, and these are connected in parallel. If ϕ signal is at "H" level, both Q_1 and Q_2 turn on, and a signal can be given from either direction. Further, if ϕ signal is at "L" level, both Q_1 and Q_2 turn off, and a signal cannot be passed.

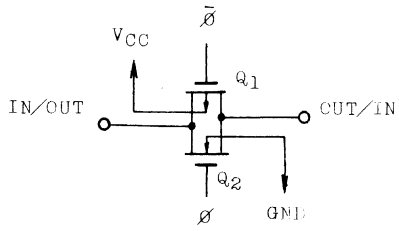


Fig. 5-2 Transmission Gate

5-2. How to Read Truth Table

Table 5-2 indicates the explanation of symbols described in Truth Table.

Table 5-2

Symbol	Explanation
H	High Level (Indicates stationary input or output level)
L	Low Level (Indicates stationary input or output level)
⌐	Indicates leading edge changing from "L" to "H".

Symbol	Explanation
↓	Indicates trailing edge changing from "H" to "L".
X	Don't care (Either "H" or "L")
Z	High impedance state
a....h	Input level of stationary state of each input of A to H.
Q_o	Level of Q just before the realization of input condition indicated in Truth Table.
Q_n	Level of Q just before inputting of active edge (↑ or ↓).
⊓	One "H" level pulse
⊔	One "L" level pulse

6. COMMON ELECTRICAL CHARACTERISTICS

6-1. Supply Current Characteristics

(1) Quiescent supply current

In the case of CMOS, under the condition in which input is fixed at "L" or "H" level, either N-channel FET or P-channel FET turns off. For this reason, the current following from V_{CC} to GND becomes only the reverse-direction saturated current of PN junction and the surface leakage current due to the stain of chip surface alone, and becomes the current of less than several nA at room temperature.

(2) Operating supply current

The operating supply current of high speed CMOS IC can be considered as the sum of the following "a" and "b":

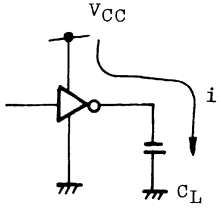
"a" The switching current to charge and discharge each capacity added to the gate output when the gate in the circuit including output buffer makes inversion.

"b" The through current flowing when P-channel FET and N-channel FET which constitute gate during inversion time turn on transiently at the same time.

When rise time and fall time of input signal are small (about 6 ns), through current of gate is usually negligibly small in comparison with switching current. For the reason, the operating supply current is governed by internal capacity of IC and charging and discharging current of load capacity. By obtaining the total sum (Power Dissipation Capacitance:CPD) of the capacity connected as a load to the gate operating in the circuit, the mean operating supply current can be decided as follows:

$$I_{DD}\ (opr.) = fin \cdot C_{pD} \cdot V_{CC} \quad \cdots\cdots\cdots \quad (6\text{-}1)$$

For the inversion of gate output from low level to high level, it is necessary that the electric charge corresponding to $C_L \cdot V_{CC}$ is supplied from V_{CC} line to load capacity C_L. Therefore, the value obtained by multiplying $C_L \cdot V_{CC}$ to the output inversion frequency (Frequency: f) within a certain period corresponds to the mean current to be supplied from V_{CC} line to IC during that period.



In the actual IC, operating gate exists in plural number, and their respective load capacity and inversion frequency are different. Therefore, operating supply current as IC is as follows:

$$I_{DD}\ (opr) = V_{CC} \cdot \sum_{1}^{n} fn \cdot C_{Ln}$$

As fn is certainly divisible by integer of input frequency (fin), the gate operating with fn/m frequency can be considered equivalently as the capacity of $\frac{C_{Ln}}{m}$.
Hence, the above equation can be developed as

$$I_{DD}\ (opr) = V_{CC} \cdot fin \cdot \sum_{1}^{n} \frac{C_{Ln}}{m} .$$

In equation (6-1), the final item is defined as CPD.

Here, C_{PD} and I_{CC} (opr) are obtained by taking TC74HC74P as an example. Connection diagram at the measurement time is shown in Fig. 6, and it is assumed that 265μA was obtained in the measured I_{CC} (opr). In this case, C_L = 0, and I_{CC} is negligible.

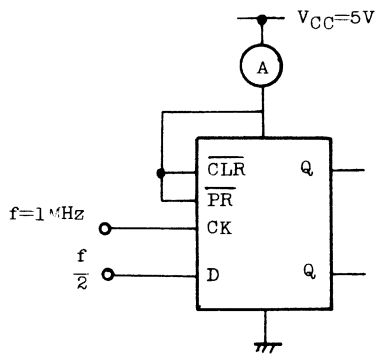


Fig. 6-1

Thus, from the above equation,

$$C_{PD} = \frac{I_{CC}\ (opr.)}{V_{CC} \cdot f_{IN}}$$

$$= \frac{265 \times 10^{-6}}{5 \cdot (1 \times 10^{6})}$$

$$= 53\ (pF)$$

Next, by V_{CC} = 5V, f_{IN} = 8MHz, C_{PD} = 53pF (using only one circuit), I_{CC} (opr) at the time of load capacity C_L = 50pF (Q output only) can be obtained as follows:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot fin + C_L \cdot V_{CC} \cdot f_{OUT}$$

$$= (53 \times 10^{-12}) \cdot 5 \cdot (8 \times 10^{6}) + (50 \times 10^{-12}) \cdot 5 \cdot (4 \times 10^{6})$$

$$= 3.12 \text{ (mA)}$$

As C_{PD} under standard operating condition is described in a separate data sheet, operating supply current can be calculated for each unit separately.

However, in the specific application such as crystal oscillation, it becomes supply current characteristics controlled by through current, and the calculation result by C_{PD} cannot be used.

6-2. Output current characteristics

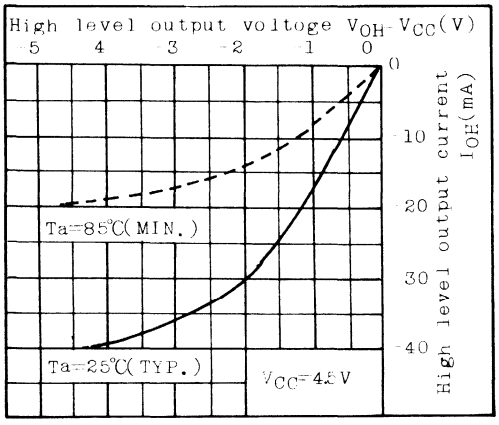
The output current characteristics of TC74HC series can be devided into standard type and buffer type.

IC of standard type is capable of directly driving 10 LSTTL, and guarantees $V_{DD}-V_{OH} \leqq 0.37V$, $V_{OL} \leqq 0.33V$ in the entire temperature range. Also, in buffer type, it is possible to directly drive 15 LSTTL under the same conditions.

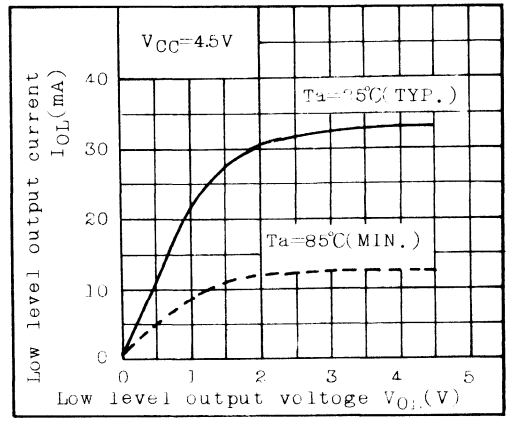
Fig. 6-2 shows the standard output current characteristics of each type when used at the supply voltage of 4.5V.

Fig. 6-2 Standard Output Current Characteristics

High level output current characteristics

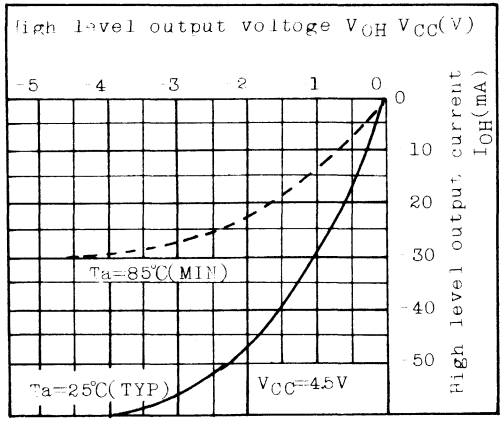


Low level output current characteristics

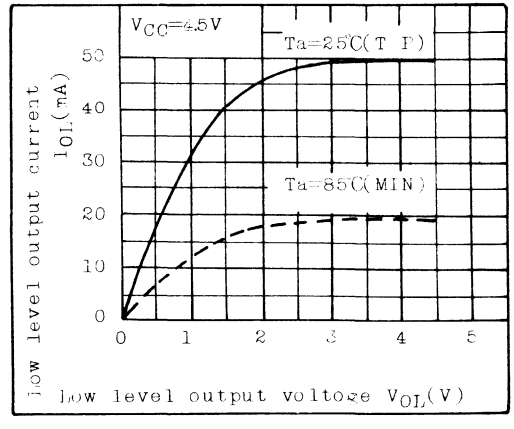


(i) Standard Type

High level output current characteristics



Low level output current characteristics



(ii) Buffer Type

(Note) Solid line shows standard characteristics chart. In the actual case, there is a variation depending upon the samples, and so, adopt the broken line and separate standard values when making design.

When the structure of device is decided, the current flowing in MOS FET is determined by gate voltage V_{GS} and voltage V_{DS} between source and drain.

In the actual IC, the gate voltage of output step MOS FET becomes nearly V_{CC} or GND level. Therefore, if $|V_{GS}| = V_{CC}$ is considered, the following equation is realized in non-saturation zone:

$$I_{DS} = K \left[2 V_{DS} (V_{GS} - V_T) - V_{DS}2\right]$$

If V_{DS} is made constant, I_{DS} is proportional to $V_{CC}-V_T$. In the saturation zone,

$$I_{DS} = K (V_{GS} - V_T)^2$$

Thus, it is proportional to $(V_{CC} - V_T)^2$ not by V_{DS}. Here, V_T is the threshold voltage proper to MOS FET, and is set at a value of about 0.7V in TC74HC series.

Fig. 6-3 shows supply voltage - output current characteristics of standard type output. This figure indicates standard value. Note that the variation of output current at the time of low supply voltage becomes large in comparison with that at the time of 4.5V.

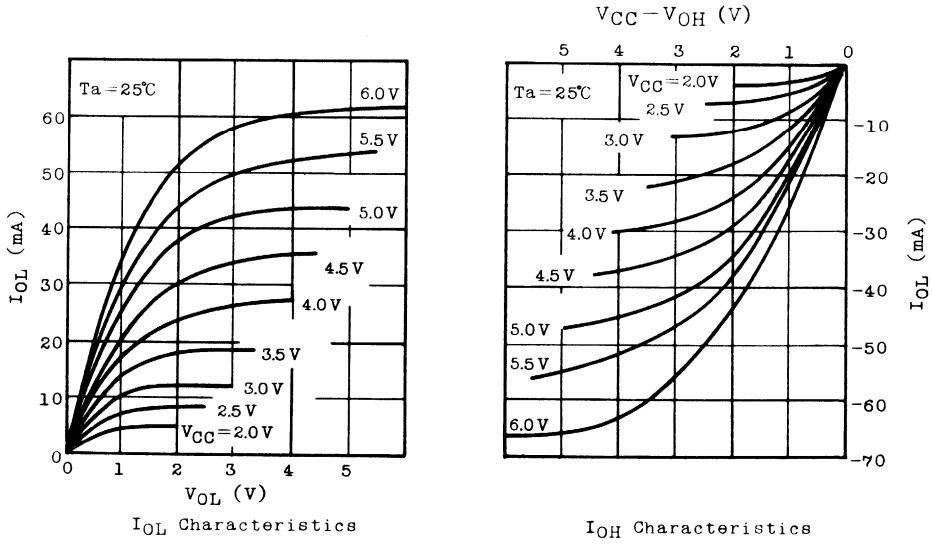


Fig. 6-3 Standard Output Current Characteristics

6-3. AC Electrical Characteristics

(1) Supply voltage dependence

Transient characteristics of IC such as propagation delay time and maximum operating frequency are determined by delay time of inner gate or rise time and fall time of output buffer.

Internal delay is considered to be chiefly due to integral effect of on resistance of MOS FET and load capacity, but as the internal capacity does not remarkably depend upon supply voltage, the drain current characteristic of MOS FET determines the dependability of AC electric characteristics on supply voltage.

Fig. 6-4 shows the dependability on supply voltage of propagation delay time in a representative gate IC.

In JEDEC, the coefficient of dependability on supply voltage is decided as follows as the standard. In the worst case, adopt the broken line indicated in Fig. 6-4 which was made on the basis of JEDEC standard.

Table 6-1 Calculation Method of AC Standard Value (excepting f_{MAX})

V_{CC}	Ta = 25°C	Ta = -40 ∿ 85°C
2.0	5.00X	5.00Y
4.5	X	Y = 1.25X
6.0	0.85X	0.85Y

Table 6-2 Calculation Method of f_{MAX} Standard Value

V_{CC}	Ta = 25°C	Ta = -40 ∿ 85°C
2.0	0.20X	0.20Y
4.5	X	Y = 0.80X
6.0	1.18X	1.18Y

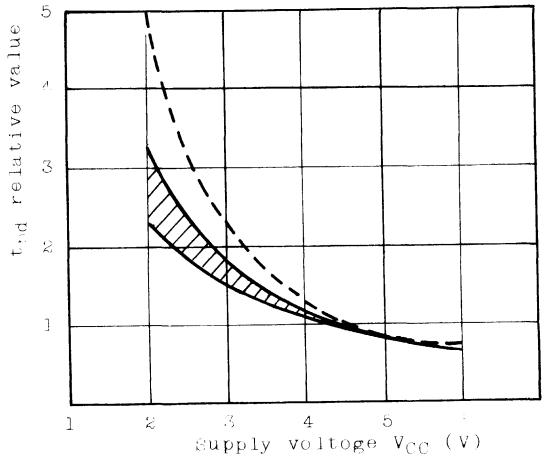


Fig. 6-4 Dependability on Supply Voltage of Propagation Delay Time (Gate IC)

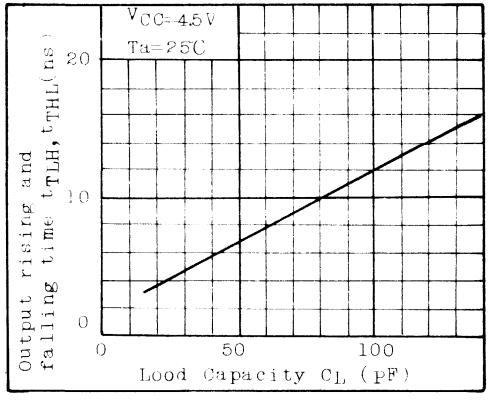
(2) Load capacitance dependence

In TC74HC series, output current has been widely improved in comparison with the conventional 4000B/4500B series, and capacity load can be driven at high speed.

However, as output impedance is decided when supply voltage is determined, rise time and fall time of output waveform, or propagation delay time will increase in proportion to an increase of load capacitance.

Fig. 6-5 indicates the load capacitance dependence of output rise time and fall time at supply voltage of 4.5V, while Fig. 6-6 shows the load capacitance dependence of propagation delay time.

Standard Type



Buffer Type

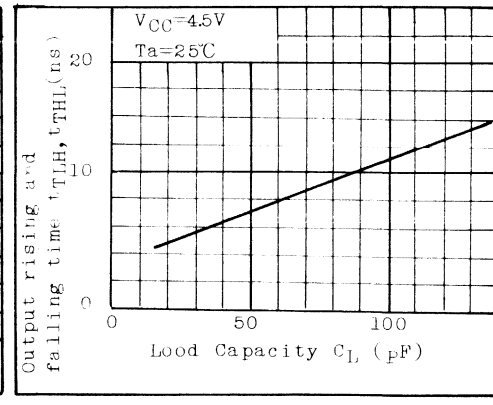


Fig. 6-5 Load Capacitance Dependence of t_{TLH}, t_{THL}

(standard characteristics)

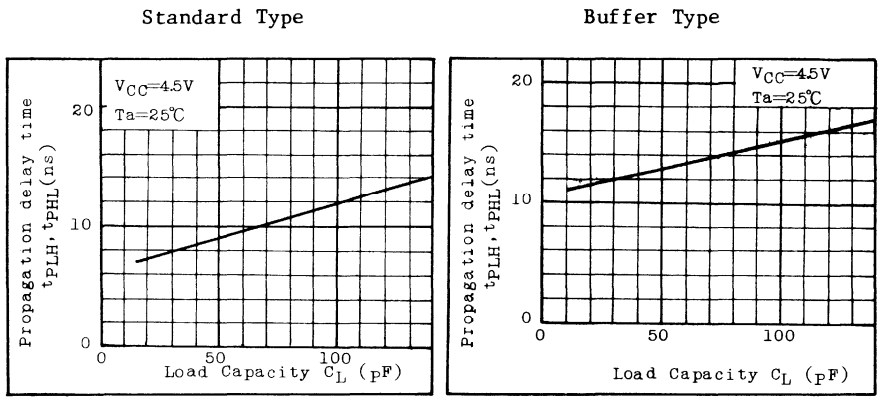


Fig. 6-6 Load Capacitance Dependence of t_{pLH}, t_{pHL} (standard characteristics)

In TC74HC series, AC characteristics of 50pF during load capacitance is guaranteed. Therefore, propagation delay time during load capacitance other than the above is obtained by the following equation.

(Example) High level propagation delay time in the case of load capacitance of XpF.

$$t_{PLH}(X) = A\ (X - 50) + t_{PLH}\ (50)$$

A: High level propagation delay time increase rate per unit load capacitance (ns/pF)

Table 6-3 Load Capacitance Dependence of AC Electrical Characteristics (ns/pF)

		Standard Output		Buffer Output	
	V_{CC}	Typical value (Ta = 25°C)	Limit value (Ta = 85°C)	Typical value (Ta = 25°C)	Limit value (Ta = 85°C)
t_{TLH}, t_{THL}	2.0	0.33	0.83	0.22	0.55
	4.5	0.12	0.24	0.08	0.16
	6.0	0.09	0.16	0.06	0.11
t_{PLH}, t_{PHL}	2.0	0.17	0.43	0.13	0.33
	4.5	0.06	0.12	0.05	0.10
	6.0	0.043	0.77	0.038	0.068

Table 6-3 indicates increase rate per unit capacity of AC electrical characteristics having load capacitance dependence.

In the case of heavy capacitance load, it is necessary to make calculation by using the limit value in this table.

6-4. Temperature Parameters of Various Characteristics

In TC74HC series, an operation in a wide temperature range of such as -40 to 85°C is guaranteed. This chapter shows how the switching time and output current are influenced by temperature.

(1) Temperature Characteristics of Output Current

Fig. 6-7 indicates temperature dependence of output current. In this figure, solid line shows the temperature dependence in standard sample. Therefore, at the time of designing, use the broken line indicated as the worst case.

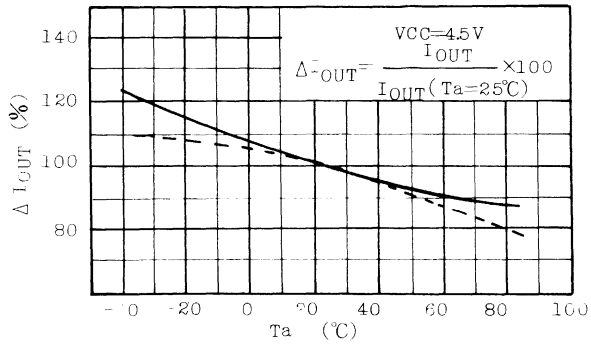


Fig. 6-7

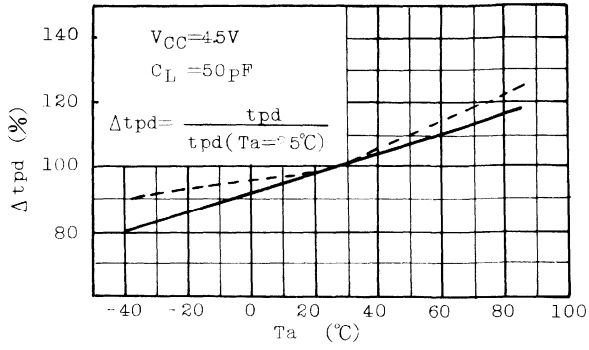


Fig. 6-8

(2) Tmeperature Characteristics of Propagation Delay Time

Fig. 6-8 shows temperature dependence of propagation delay time. Solid line in this figure indicates standard temperature dependence at Gate IC. At the time of designing, therefore, use the broken line indicated as the worst case.

7. PRECAUTIONS IN HANDLING

7-1. Electric Static Discharge

CMOS IC has very thin gate insulation oxide film. When high voltage is applied to this gate electrode (input of CMOS IC), oxide film directly under the gate causes dielectric breakdown sometimes. In TC74HC series, as shown in Fig. 7-1, resistnace and diode are added to all input terminals in order to protect CMOS gate from such high voltage. However, protective circuit may not necessarily be effective against accidental high voltage, care must be fully taken in handling it.

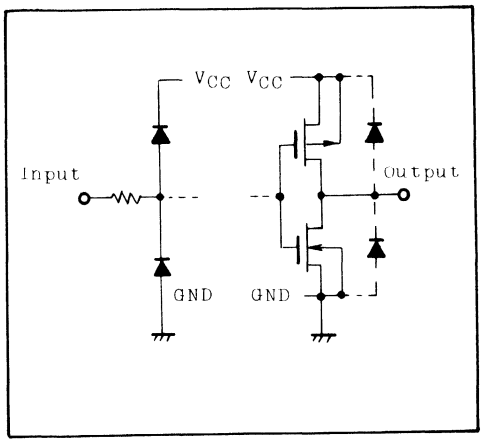


Fig. 7-1 Input Protective Circuit, Output Equivalent Circuit

Futher, as parastic diode is formed between each terminals as indicated in Fig. 7-1, thermal breakage and latch up due to excessive current may sometimes be caused when the voltage exceeding the ratings is applied between each terminals. Therefore, care must fully be taken at the time of assembling and adjustment.

Note) As input protective resistance, poly silicon resistance of 200 to 400Ω is used.

(1) Electrostatic Discharge Test Method

Fig. 7-2 shows electrostatic discahrge test method. In Fig. 7-2, test is conducted with C = 200pF, R = 0Ω. Table 7-1 shows the results of electrostatic discharge test applied to a representative type of TC74HC series.

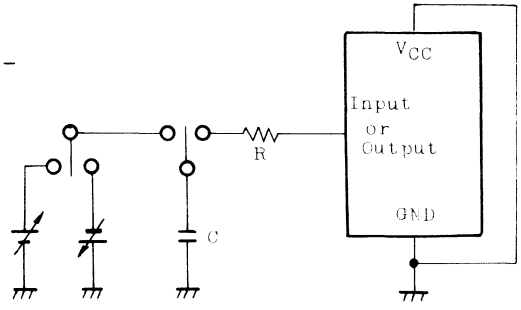


Fig. 7-2 Test Circuit

In the test of the above method standardized by EIAJ, it is acknowledged that ±200V will practically withstand an ordinary service condition. As shown by Table 7-1 Toshiba's TC74HC series has ample capacitance.

Name	Input		Output	
	Impression of + voltage	Impression of - voltage	Impression of + voltage	Impression of - voltage
TC74HC 00P	300V	-300V	Above 1000V	Above -1000V
TC74HC 04P	400V	-350V	Above 1000V	Above -1000V
TC74HC 74P	300V	-300V	Above 1000V	Above -1000V
TC74HC138P	450V	-350V	Above 1000V	Above -1000V
TC74HC240P	350V	-350V	Above 1000V	Above -1000V
TC74HC373P	350V	-350V	Above 1000V	Above -1000V

C = 200pF, R = 0Ω, Impression frequency three times

Table 7-1 Test Result

7-2. Precautions in Handling

(1) Transportation and Storage

As input and output terminals of unmounted CMOS IC are in the state of high impedance, they are apt to receive induction from the surrounding charged body, space electric field, and human body. For this reason, it is necessary in transporting and storing them to use dielectric mat, metal case or aluminum foil box, so that each terminal of IC may become at same potential.

As TC74HC series is inserted in a magazine given no-charging treatment at the time of shipment, do not take it out from the magazine unnecessarily. Especially, avoid to use plastic or vinyl container which is apt to charge static electricity.

(2) Assembling

When installing CMOS IC on the printed board, it is necessary to protect the electric equipment, working stand and operators from static electricity by making grounding. It is advisable to ground the working stand by spreading metal plate or aluminum foil on the surface. Grounding of operators should be made through the resistance of about 1 MΩ so as to prevent an electric shock. It is convenient to make grounding through metallic ring or metallic watch band. Also, it is advisable not to wear working clothes make of chemical fiber. Further, it is necessary to periodically check electric equipment to insure absence of electric leakage.

When shaping the lead wire during the packaging of IC, it is advisable to use pincet or similar jig, so that stress may not be given to the root.

When storing or transporting the completely assembled printed board, short circuit the terminals of printed board or cover the entire board with aluminum foil, so that input terminal of IC may be opened.

(3) Soldering, washing

When making soldering by using soldering iron and tank, carry out the work at the temperature of 260°C or below within 10 seconds. It is confirmed that the reliability of TC74HC series is never affected when subjected to a temperature stress to the stopper of lead at 260°C for 10 seconds.
Use a soldering iron having no leak at its end. It is recommended to use A class iron having insulation resistance exceeding 10 MΩ.

When using soldering tank, it is necessary to make grounding so as to prevent the potential of soldering tank from becoming unstable.

After soldering IC on the printed board, cleaning is made to remove flux, etc. For this cleaning is used flux removing abluent or cleaning method utilizing ultrasonic wave. Care must be fully taken for the selection of this solvent so at to prevent the effect given to the package and mark of CMOS IC. In general, it is advisable to use Freon series.

In the case of ultrasonic cleaning, it is necessary to prevent the stress due to resonance from being imposed on IC or printed board. For this purpose, it is needed to consider such washing method that the main body becomes a shade against a vibrator, and also a cleaning time of less than 30 seconds.

(4) Adjustment, Test

When making adjustment and test after the completion of printed circuit board, it is necessary to check absence of soldering bridge or crack on the printed board before switching on supply power. As CMOS system requires only small supply current, it is well to apply current limitation when making test by using marketed constant voltage power source.

When mounting and dismounting printed circuit board on and from the socket, never fail to cut off power supply beforehand.

When surveying each part of printed board with probe during the test, care must be fully taken to prevent contact of tip of probe with other signal or power line. When surveying place is previously determined, it is advisable to erect a special test pin.

When test is conducted under high temperature and low temperature, it is necessary to take grounding of constant temperature oven, and the inside set must be on or in the inductive material.

This item excepting one part, is also applicable when CMOS IC single unit is tested.

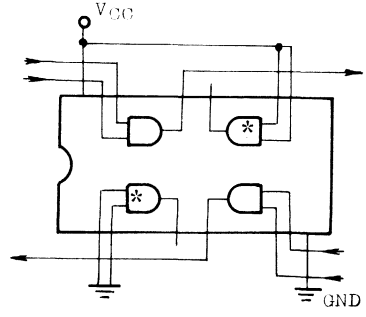
8. PRECAUTIONS IN DESIGNING CIRCUITS

8-1 Input Processing

(1) Processing of unnecessary gate

Input of CMOS IC has so high impedance that logical level becomes underfined under open condition. In this case, if input is at intermediate level, the transistors of both P-channel and N-channel become continuity state, and unnecessary supply current flows.

Therefore, as shown in Fig. 8-1, be sure to connect unnecessary input line to V_{CC}, GND or other input and output whose logical level is decided.



(* Unnecessary gate)

Fig. 8-1 Treatment of Input

In the case of CMOS, if soldered part has bad contact, mul-function of system or increase of supply current will be caused. Therefore, care must be taken at the time of wiring.

(2) Input processing of printed circuit board

When input terminal of printed circuit board is connected directly to CMOS input, CMOS input is brought to electrically floated condition as in the case of IC single unit when transported or stored as a single unit of printed board. It is advisable, therefore, to connect previously to V_{CC} or GND through resistance in the printed circuit board, as indicated in Fig. 8-2.

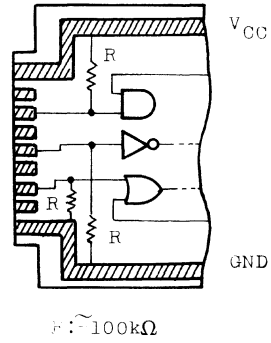


Fig. 8-2 Input processing of printed circuit board

8-2 Design of Power Source

In general, CMOS requires small consumption current in comparison with other bipolar digital IC, and therefore it needs only small capacity power supply. However, from its operational requirement, CMOS consumes power in spike state, and therefore it is necessary to keep high frequency impedance of power source at low level.

It is adviasable to make wiring of power source (V_{CC}) line and GND line thick and short, and to insert, as high frequency fliter, once 0.01 μF to 0.1 μF capacitor between V_{CC} and GND for each IC.

Also, it is recommended to insert a condenser of about 10μF to 100μF between power supply entrance and GND as low frequency filter. As mean supply current considerably differs depending upon operating frequency of system, existence of condenser load, rising and falling of input signal and supply voltage, attention must be specially given in the case of simple power source by Zener diode, or battery driving. When there is overshooting or undershooting during transient time of supply power, use filter etc, so that the maximum rating may not be exceeded.

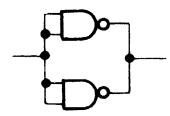


Fig. 8-3 Example of increase in driving capacity

8-3 On Output Short-circuit

In TC74HC series, buffer is added to the output, and both flow-out (I_{OH}) and flow-in (I_{OL}) current driving are possible. For this reason, excessive current flows in C MOS output when "H" level output line is shorted with GND line or "L" level output line is shorted with V_{CC} line. Particularly, when the supply voltage is high, allowable loss of package is exceeded by this current, and therefore care must be taken not to cause output short circuit.

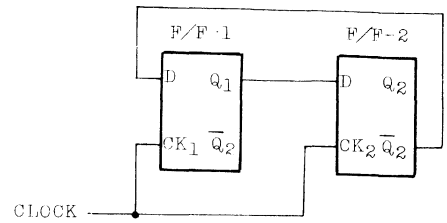
It is of course impossible to directly connect ordinary outputs together, but in the case of IC which has 3 state output, wired OR is permitted provided that more than two outputs do not become enable simultaneously.

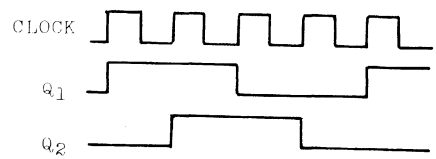
Further, in order to improve driving capacity, it is possible to connect the gates in the same package as shown in Fig. 8-3.

8-4 Effect of Input of Slow Rise Time and Fall Time

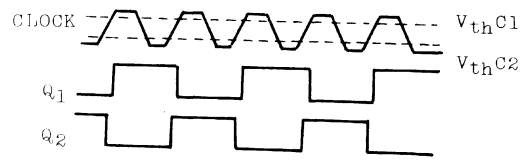
When the waveform of slow rise time or fall time is impressed to CMOS input, it sometimes happens that output tends to oscillation around V_{TH} (threshold voltage of circuit) of input waveform in the case of gate IC. This is because CMOS gate becomes linear amplifier equivalently in the vicinity of V_{TH}, and minute power source ripple and noise component are amplified in the output and appear.

For the purpose of preventing the above, it is necessary to insert high frequency filter condenser between V_{CC} and GND of oscillating IC, or to use Schmitt trigger IC.
In the case of TC74HC series, excepting HCU type, Schmitt trigger IC, input rising and falling time is regulated as shown in Table 8-1 in the recommended operating conditions. Please follow this condition.

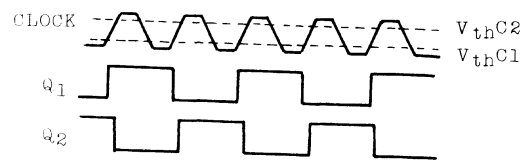




(a) Normal operating waveform



(b) Malfunction waveform from at the time of $V_{thC1} > V_{thC2}$



(c) Malfunction waveform from at the time of $V_{thC1} < V_{thC2}$

Fig. 8-4 Example of Malfunction

Fig. 8-4 shows an example of malfunction when shift counter is constituted by using type D flip-flop of another package. In this case, malfunction is considered to be caused by the difference of circuit threshold level of respective D type flip flop.

Now, let circuit threshold level of F/F-1 be $V_{th}C1$, and that of F/F-2 be $V_{th}C2$. Then, as shown in Fig. 8-4, time difference Δt is formed while the rising waveform of clock pulse cuts the respective circuit threshold voltage, and thus malfunction takes place.
The following condition is required for insuring normal operation:

$$\Delta t < tpd\ (CK - Q) + t_{set-up}$$

In this case, there is a possibility of malfunction even though input signal is within the standard value of Table 8-1. Therefore, care must be specially taken for sequence circuit clock input.

Table 8-1 Standard Value of Input Rising and Falling Time

Item	Symbol	Limit	Unit
Input Rising and Falling Time	tr, tf	0 ∿ 1000 (V_{CC} = 2.0V) 0 ∿ 500 (V_{CC} = 4.5V) 0 ∿ 400 (V_{CC} = 6.0V)	ns

8-5 Precautions for Wiring

(1) Output waveform distortion

As output impedance of TC74HC series is considerably low in comparison with the conventional standard CMOS IC, distortion is sometimes caused in the output waveform depending upon L component of wiring, when the wiring connected to output end is long or when capacitance is connected between signal line and V_{CC} or between signal line and GND. Therefore, when designing the printed board, take care not to make signal wiring length too long. In the case of both side printed board, it is ideal to limit signal wire length to 30cm or less. Especially, in the clock signal line, distortion of waveform causes malfunction.

(2) Precautions for arrangement

Output of TC74HC series has quick rising and falling time, and makes full swing at V_{CC}-GND, and so it becomes a noise source of other signal. Therefore, it is desirous to locate it separately from a part which is sensitive to a noise of analog circuit. Also, care must be taken for the reduction of load number and curtailment of wiring length.

(3) Termination

From its physical and electrical factors, TC74HC series is apt to cause overshooting and undershooting, and this leads to malfunction of circuit or breakdown of passive IC. These troubles can be prevented to some extent by terminating the end of signal line. Fig. 8-5 indicates examples of general termination.

(a) Termination by CR (b) Termination by Diode

Fig. 8-5 Examples of Termination

8-6 Interface

(1) Input and output interface

When making some processing with CMOS system, most systems make exchange of signals with external circuit or mechanism. These input and output signal lines are naturally made long in many cases, and have distributed inductance or reactance. Therefore, if directly connected with CMOS, they will give rise to various troubles.

Conceivable serious troubles may be the malfunction due to induced noise, and the destruction of input/output element due to surge. To cope with these problems, reduction of signal line impedance (driving impedance) or insertion of noise eliminating circuit on the receiving side is applied for the former, while surge protective measures are taken for the latter.

Fig. 8-6 illustrates an example of making noise · surge protection on the input side.

(a) and (b) of this figure show an example of absorbing noise by integrating input waveform by RC. (c) and (d) indicate an example of protecting CMOS from input surge.

Fig. 8-7 gives an example of output interface. These are only one example, but in any case, some protection should be given to an interface involving long signal line.

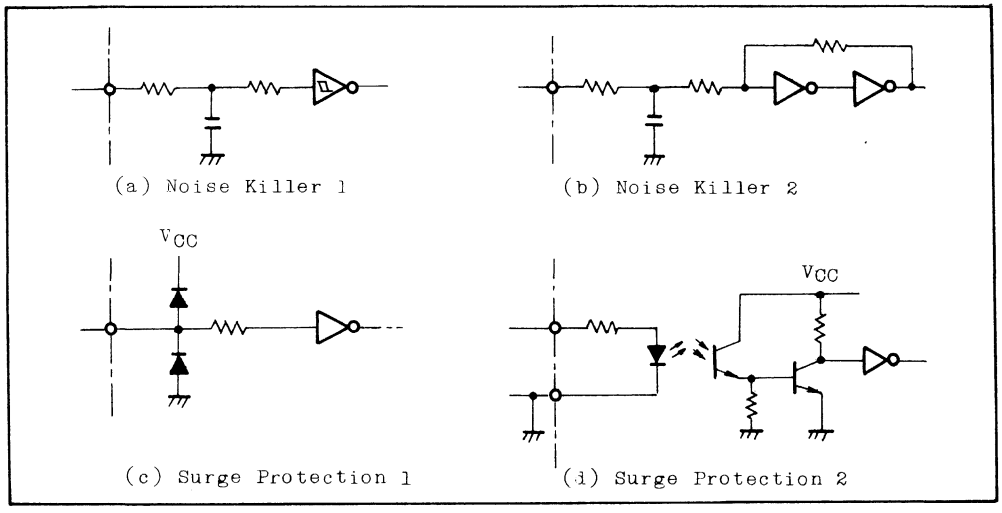


Fig. 8-6 C MOS Input Protective Circuit

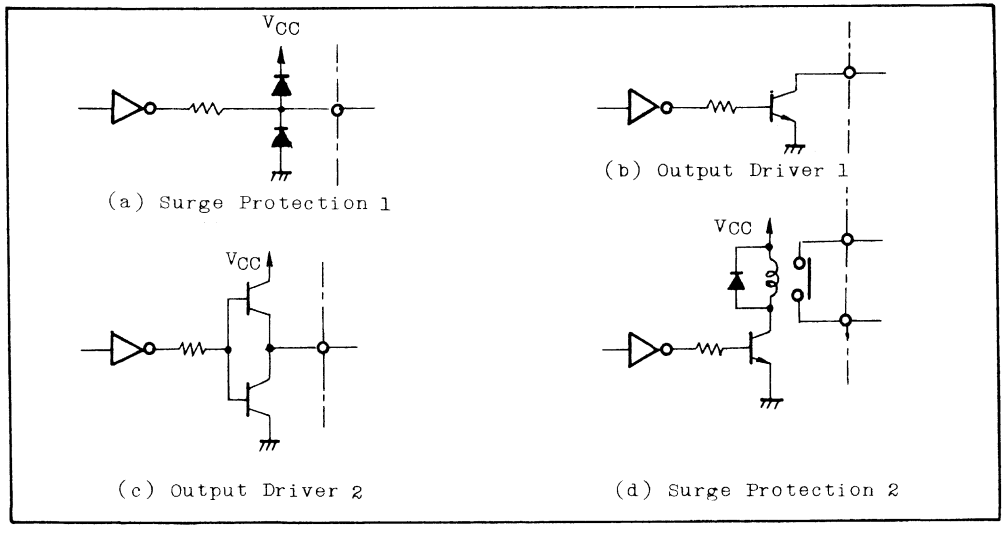


Fig. 8-7 Output Protection/Driving Circuit

(2) Interface of C MOS IC

In the case of mutual interface between CMOS IC, input impedance of CMOS has so large value that limitation of fan out may not be so large. However, there is actually need to consider fall of propagation time due to adding effect of load capacity and an increase of power consumption.

As input capacity of CMOS is about 5 pF per input, if 10 fan outs are taken for example, load capacity of 50pF is given by it, and further, line capacity on the printed board must also be taken into account. This shows that the processing speed of system is controlled not only by circuit constituting method but also by fan out.

When constituting a system with CMOS IC, it is recommended to examine fan out by taking these points into cosideration.

(3) Interface between different CMOS families

The problem to be considered between different CMOS families is difference of supply voltages between families. When different C MOS families are used with the same power source, it is all right to pay attention to the hazard due to the propagation delay time difference, but in the case of different power source, the voltage level converting circuit is needed.

Fig. 8-8 shows an interface method from the standard C MOS oprating at 6V∿15V to 74HC. The most popular method is to use C MOS (4049B/4050B) which has level shift function as shown in this figure.

4049B/4050B has diode of GND side diode only, and is so constructed that current does not flow in the power source (V_{CC}) of 5V system even though voltage of 15V is impressed.

On the otherhand, an interface from 74HC to standard C MOS can be realized by using TC5020BP of level shift use IC, as indicated in Fig. 8-9(a). Further, it is also possible to use discrete transistor as shown in Fig. 8-9(b). The circuit employing discrete transistor can of course be used for power inversion.

(4) Interface with TTL

When driving TTL with TC74HC series, input and output voltage level can be connected in that state without trouble. Fan out is decided by output current of CMOS IC and input current of TTL. Its example is shown in Fig. 8-10.

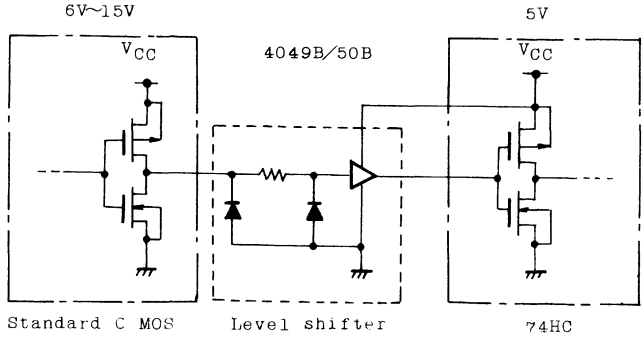
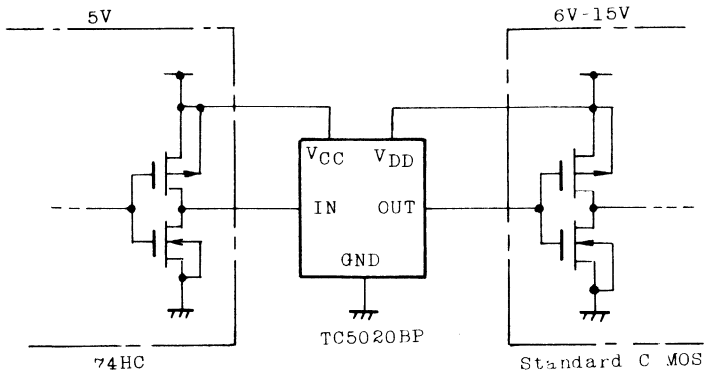
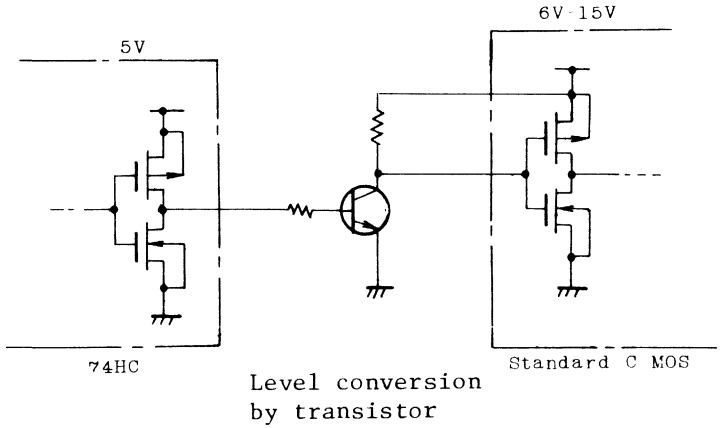


Fig. 8-8 Standard C MOS → 74HC Interface

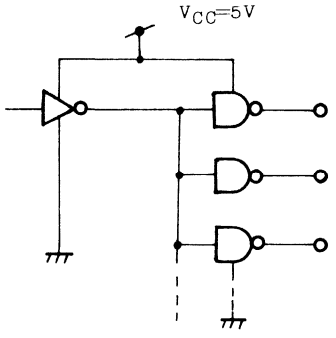


(a) Example of using level shifter IC.



(b) Example of using transistor

Fig. 8-9 74HC → Standard C MOS



Fan Out Number

	Standard Type	Buffer Type
TTL	2	3
S TTL	2	3
LS TTL	10	15
ALS TTL	20	30

Fig. 8-10 TC74HC → TTL Interface

In this way, TC74HC series is capable of directly driving various TTL devices.

On the other hand, when driving TC74HC series from TTL, it is necessary to convert output voltage level of TTL to input level of 74HC. Normally, in this case TC74HCT series which has same input level with LS TTL are used. Input current of TC74HCT series is very small like that of TC74HC series, and therefore no burden is imposed on the driving side 74LS, and the speed also does not fall so much. Therefore it can be said to be an effective method. Another method is to use pull up resistance as shown in Fig. 8-11.

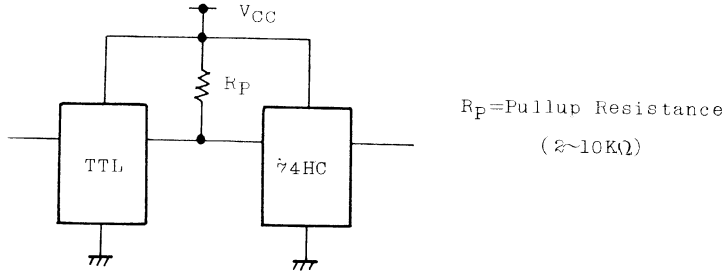


Fig. 8-11 TTL → TC74HC Interface

(5) Interface with CPU

At present, as the peripheral supporting logic of microprocessor of many NMOS and CMOS, 74LS series is used universally. As TC74HC series has the same speed with 74LS, it can naturally be used as microporcessor peripheral logic.

As for an interface between C MOS CPU and 74HC series, there is no problem because both are CMOS. At present, however, priority of NMOS CPU is higher, and interface of NMOS to CMOS must be taken into consideration.

Output of most NMOS CPU deflects up to near V_{CC}, but as shown in Fig. 8-12, as outputs of both driving MOS and load MOS are constituted with enhancement type, no deflection takes place until V_{CC}. For this reason, in order to certainly carry out the signal transfer from NMOS CPU to 74HC, it is easy to use 74HCT series which has an input of TTL level. When connecting 74HC series, pull up resistance is used as indicated in Fig. 8-12.

Next, driving of NMOS CPU from 74HC series can be connected without difficulty. This is because, normally input of NMOS is of high impedance like C MOS, and DC fan out need not be taken into consideration.

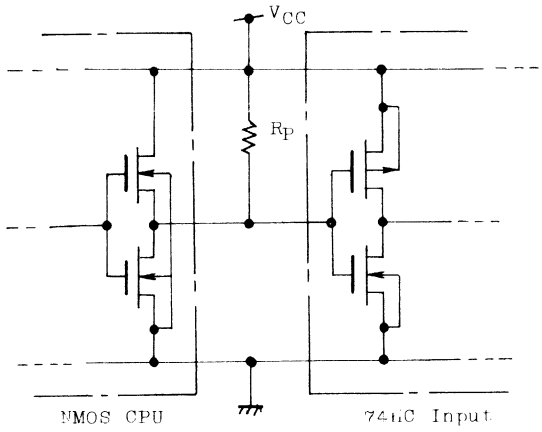


Fig. 8-12 NMOS CPU Interface

8-7 Latch-up

Latch up is a phenomenon peculiar to CMOS, and is also called SCR (Silicon Controlled Rectifier) Phenomenon. During the normal operation time, if excessive voltage and current caused by big noise or accidental surge are applied on the input and output terminal, or supply source amplitude is suddenly fluctuated, abnormal current flows between V_{CC} and GND, and this abnormal current continues to flow even though the disturbance signal is cut off, and finally puncture is caused. Latch-up is a name given to such phenomenon.

Once the latch-up takes place, the former condition is not restored unless the power supply is cut off or voltage is lowered, and an overcurrent continues to flow between V_{CC} and GND. It this status is left alone, destruction of element such as melting of wiring will take place.

(1) Cause of latch-up

Fig. 8-13 shows an equivalent circuit due to parasitic element. NPN transistor Q_2 is formed in P-well of NMOS side while PNP transistor Q_1 is formed in N-substrate of PMOS side, and parasitic resistance exists between terminals. As is clear from the current path through the medium of parasitic element indicates in this figure, these parasitic elements constitute Thyristor.

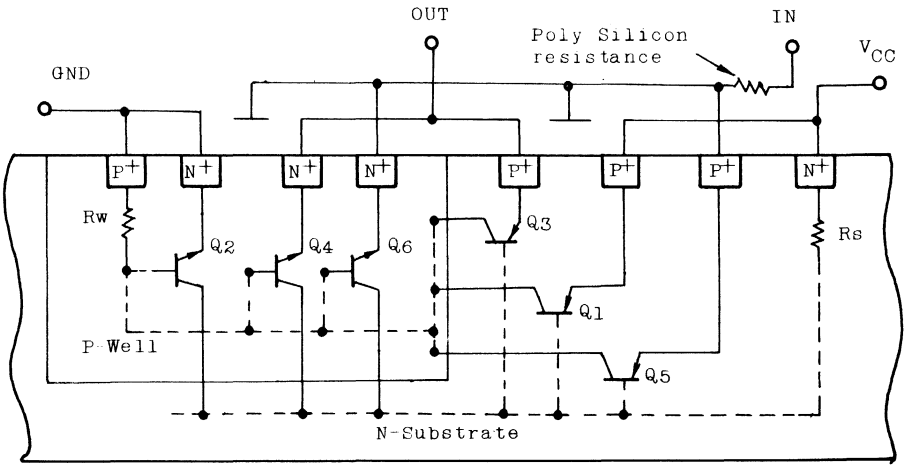


Fig. 8-13 Internal Equivalent Circuit of CMOS IC

For example, if current flows into the N-substrate from external causes, voltage drop takes place in resistance Rs of the N-substrate, and this causes to turn on parasistic transistor Q_1, and current flows towards GND from Vcc through the medium of resistance Rw of P-Well. When current flows in Rw, voltage drop takes place at both ends of Rw, Q2 turns on, and further, supply current flows through Rs. As a result, the voltage drop at both ends of Rs furthers increase, Q_1 and Q_2 are left in the turn-on state, and the supply current further increases.

In this way, if the voltage drop takes place in resistance Rw of P-Well and in resistance Rs of N-substrate, latch-up occurs, and therefore, the following causes are considered.

① To make input voltage higher than $V_{CC} + V_F$
(Q5 of Fig. 8-13 turns on)

② To make input voltage lower than GND - V_F
(Q5 of Fig. 8-13 turns on)

③ To make output voltage higher than $V_{CC} + V_F$
(Q5 of Fig. 8-13 turns on)

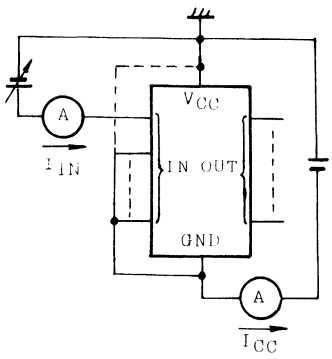
④ To make output voltage lower than GND - V_F)

⑤ To raise supply voltage V_{CC} above the rated value and to cause breakdown. (To directly flow current in Rw or Rs)

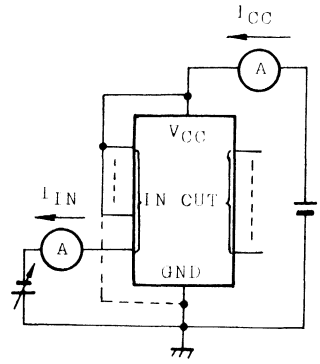
Here, V_F is the forward voltage between base and emitter of parasitic bipolar transistor Q_3 - Q_4.

(2) Latch up strength measurement

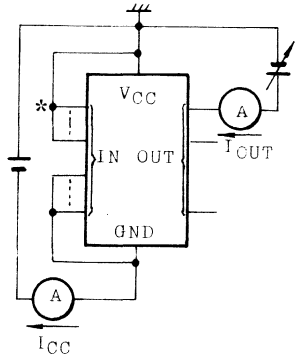
Fig. 8-14 illustrates measurement example of latch up strength. As indicated in Fig. 8-14, latch-up is induced by flowing current into input terminal (⊕ injection) or flowing current out of output terminal (⊖ Injection), and the current value at that time is measured. Table 8-2 shows the results of Latch-up Strength Test of representative types of TC74HC series. As indicated here, TC74HC series have ample margin such as input of above ± 70mA and output of above ± 300mA against the maximum rating of ± 20mA.



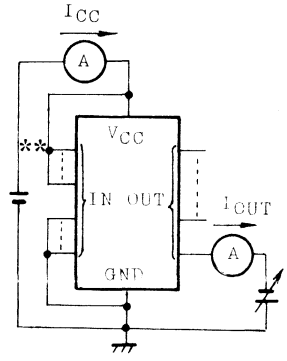
(a) Measuring circuit of ⊕ Injection strength of Input Terminal



(b) Measuring circuit of ⊖ Injection strength of Input Terminal



(c) Measuring circuit of ⊕ Injection strength of Output Terminal



(d) Measuring circuit of ⊖ Injection strength of Output Terminal

* : Input condition to make measured terminal "H" level.

** : Input condition to make measured terminal "L" level.

Fig. 8-14 Latch-up Strength Measuring Circuit by Current Feeding System

Table 8-2

Unit : mA

Type	Class	Input ⊕	Input ⊖	Output ⊕	Output ⊖
74HC02	NOR-GATE	Above 70	Above 70	Above 300	Above 300
U04	INVERTER	Above 70	Above 70	Above 300	Above 300
74	D-F/F	Above 70	Above 70	Above 300	Above 300
138	LINE DECODER	Above 70	Above 70	Above 300	Above 300
375	D-Latch	Above 70	Above 70	Above 300	Above 300

(Note 1) As for this input exceeding ±70mA and the output exceeding ±300mA, no measurement is made as there is a possibility of breakdown of element.

(3) Countermeasures

As ample margin is provided for latch-up as explained in (2), there is no problem in using the unit within the standards. However, for the interface part having the possibility of receiving excessive surge, it is recommended to add the protective circuit as indicated in Fig. 8-15.

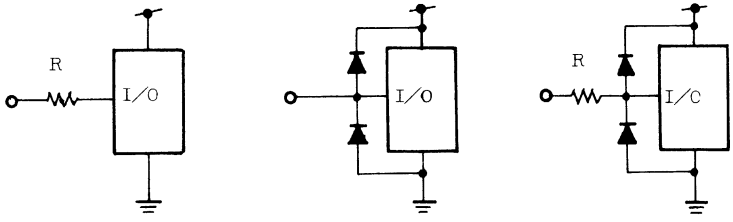


Fig. 8-15 Example of Latch-up Preventive Method

9. MINI FLAT PACKAGE (MFP) C MOS

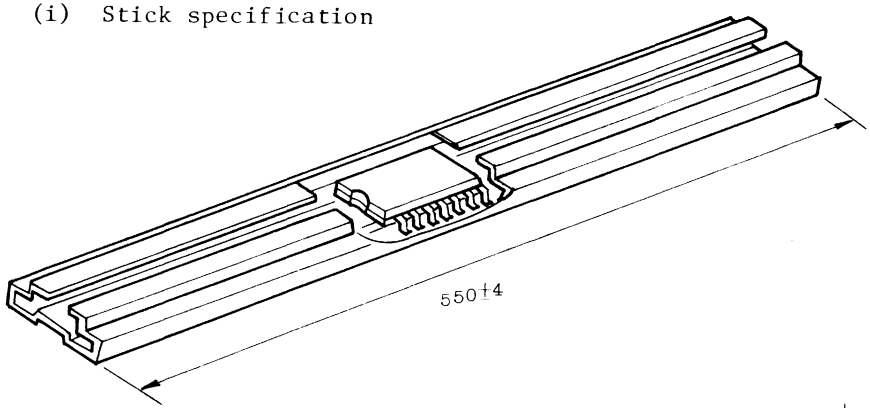
With the tendency of electronic apparatus towards light weight, thim thickeness, short size, small volume and low power consumption, the semiconductor, integrated circuit and various component parts mounted on them have also been requested to be made smaller, lighter and thinner.

Toshiba mini flat package (MFP) IC has been developed to solve these problems and to provide small and thin apparatus and hybrid IC.

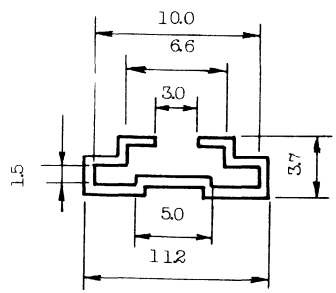
(1) Package form

Package form of Toshiba mini flat package (MFP) C MOS IC is divided into stick specification which is given electrostatic preventive treatment and taking specification which is convenient for automatic insertion.

(i) Stick specification



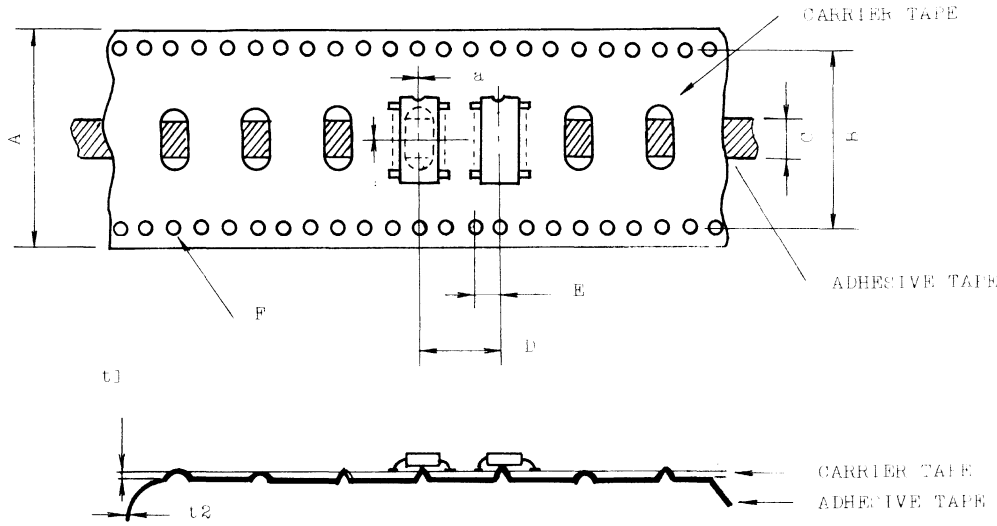
unit:mm
TOLERANCE:±0.3mm
t:0.6



Material: Vinyl chloride given electrostatic preventive treatment
Accommodation quantity : 14 pin, 16 pin → 50IC/stick
20 pin → 40IC/stick
* Stopper made of synthetic rubber is attached to both sides.

Fig. 9-1 Stick Dimension Drawing

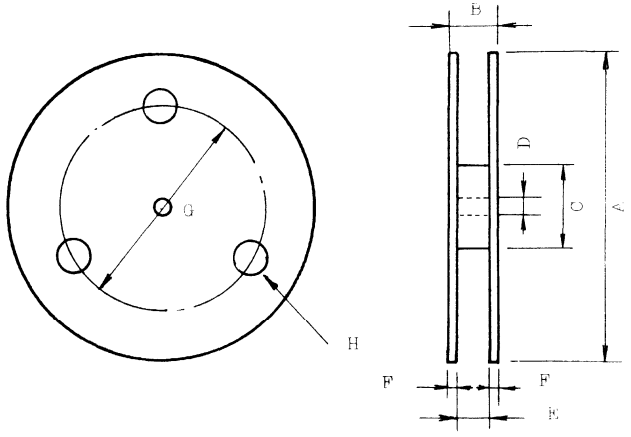
(ii) Taping specification



A	32 $^{+0.0}_{-0.4}$	D	12 ± 0.1	t_1	0.15
B	26 ± 0.1	E	4 ± 0.1	t_2	0.18
C	6 ± 0.1	F	ϕ=1.0 $^{+0.1}_{-0.0}$	a	0.0 ± 0.5

UNIT: mm

Fig. 9-2 Tape Shape and Dimension

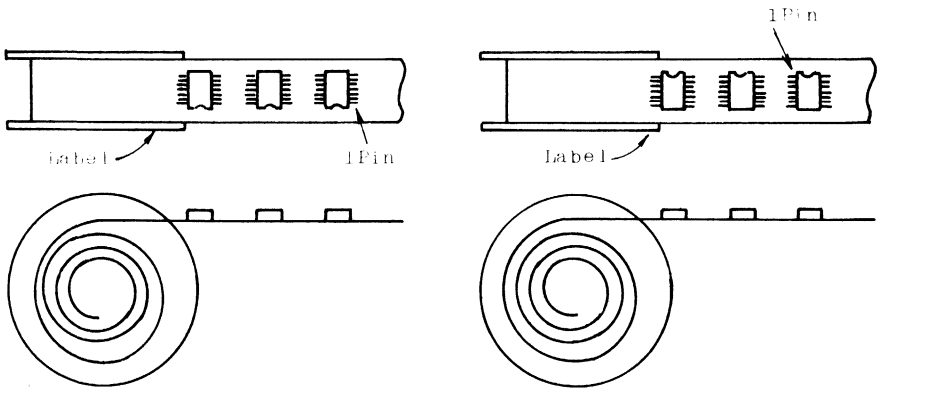


A	ϕ300±2.0
B	37.6±1
C	ϕ80±2.0
D	ϕ15.5±0.5
E	34±1
F	1.8±0.1
G	ϕ200
H	ϕ30±0.5

UNIT: mm

Fig. 9-3 Shape and Dimension of Take-up Reel

(iii) Coiling direction of tape



Type 1(TP1) Type 2(TP2)

(iv) Standard quantity

Reference unit will be 2,000/reel.
Kindly place orders with multiple unit of 2000.

(v) Ordering

When ordering the taping goods of Toshiba mini flat package (MFP) C MOS IC, kindly designate the name, taping direction and quantity in the following way.

(Example) TC74HC00F — TP2 12000 pieces

Quantity (based upon iv)

Taping direction

Name of goods

10. DATA SHEETS

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC00P/F

TC74HC00P/F QUAD 2-INPUT NAND GATE

The TC74HC00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

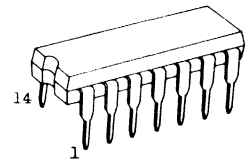
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

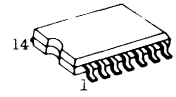
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTLL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS00

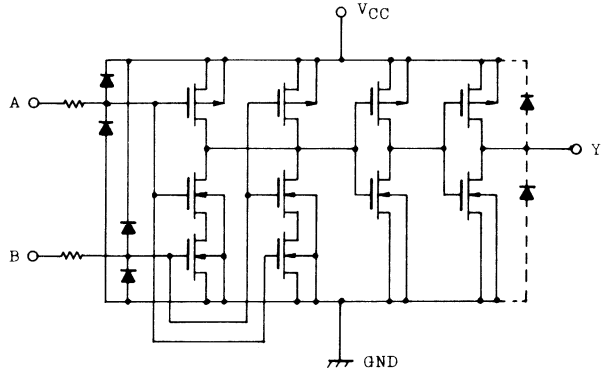


DIP14(3D14A-P)

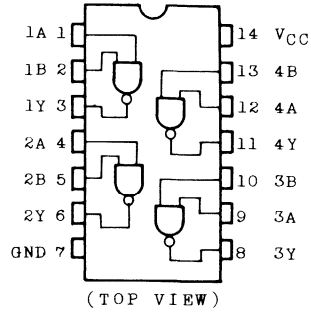


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC00P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC00P/F

DC ELECTRICAL CHARACTERISTICS

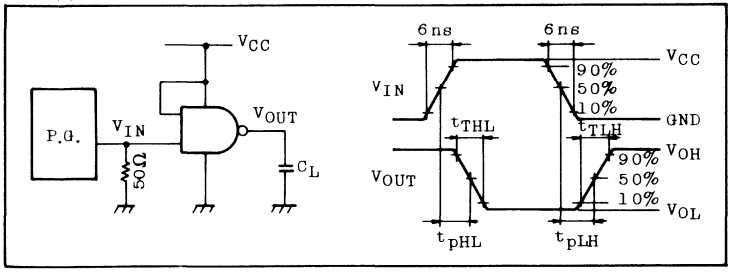
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

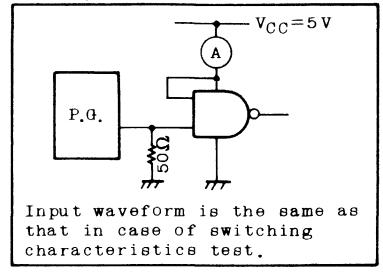
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	22	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC02P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC02P/F QUAD 2-INPUT NOR GATE

The TC74HC02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C²MOS technology.

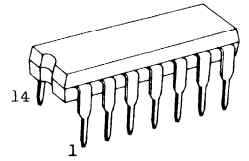
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

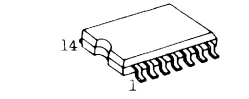
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS02

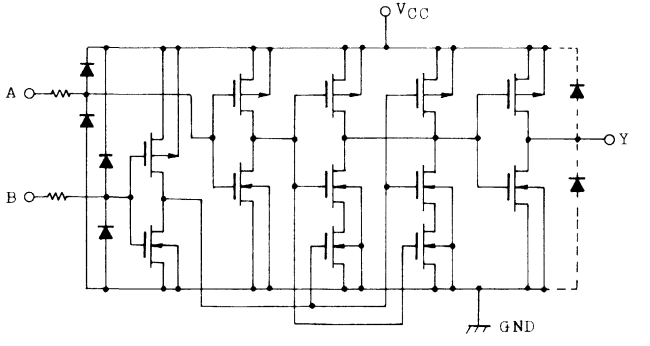


DIP14(3D14A-P)

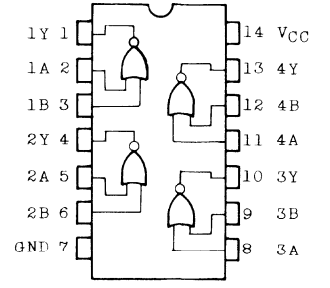


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC02P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC02P/F

DC ELECTRICAL CHARACTERISTICS

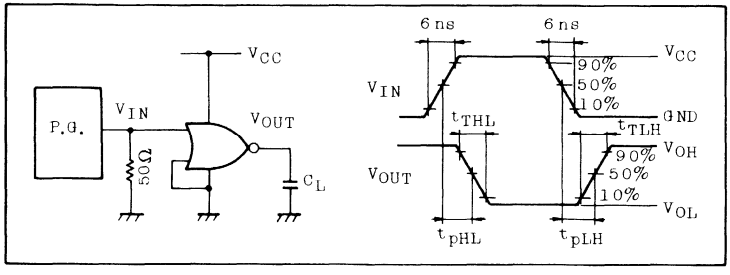
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

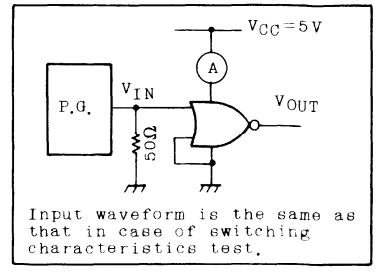
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC03P/F

TC74HC03P/F QUAD 2-INPUT NAND GATE (OPEN DRAIN)

The TC74HC03 is a high speed CMOS QUAD 2-INPUT NAND GATE (OPEN DRAIN) fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

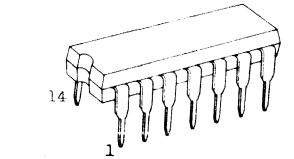
The TC74HC03 has, as its output, a high-performance MOS N-channel transistor. (OPEN-DRAIN outputs)

This device can, therefore, with a suitable pullup resistor, be used in wired-AND, LED driver and etc. application.

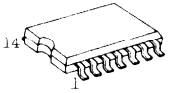
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{PLZ}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Open Drain Structure
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS03



DIP14(3D14A-P)



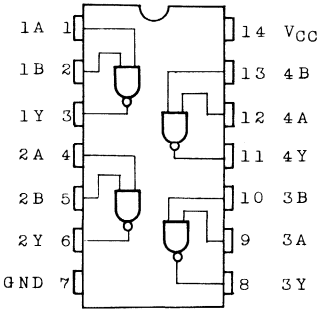
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

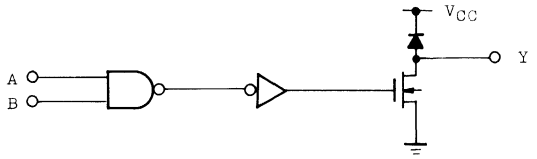
TC74HC03P/F

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z : HIGH IMPEDANCE

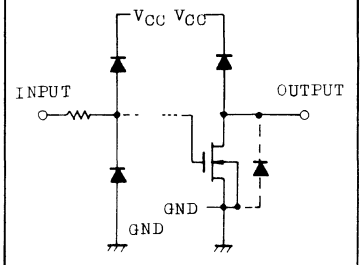
CIRCUIT DIAGRAM (PER GATE)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	A or B=V_{IL} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

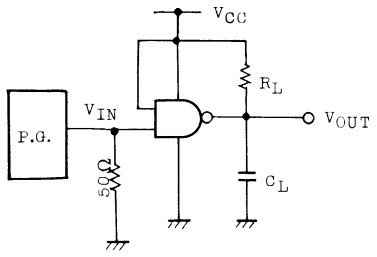
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	-	52	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	-	52	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	5	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	17	-	-	-	

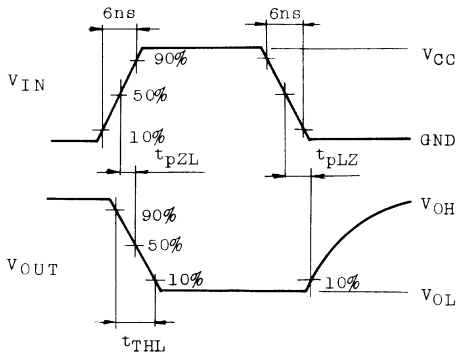
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per gate)}$$

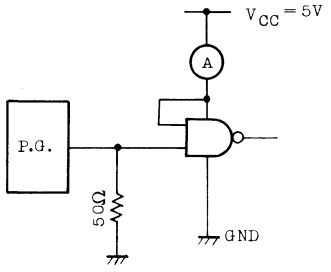
TC74HC03P/F

SWTICHING CHARACTERISTICS TEST CIRCUIT





I_{CC}(Opr.) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC04P/F

TC74HC04P/F HEX INVERTER

The TC74HC04 is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

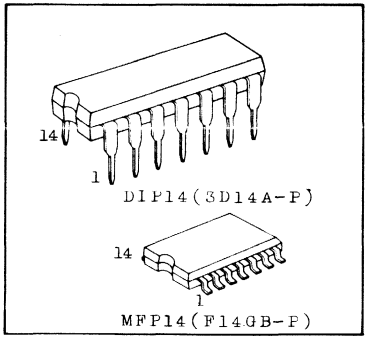
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=8ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS04

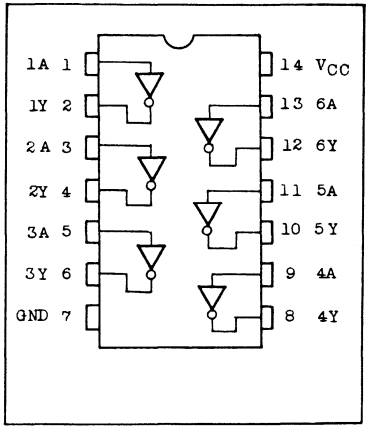


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

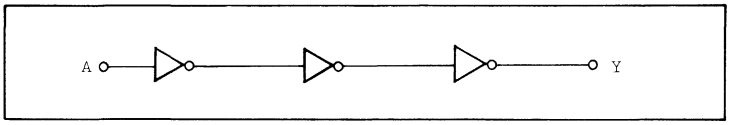
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

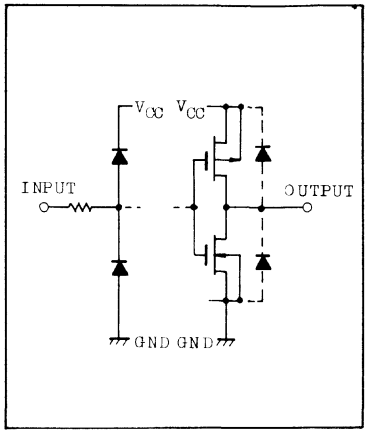


TC74HC04P/F

LOGIC DIAGRAM (per Gate)



INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

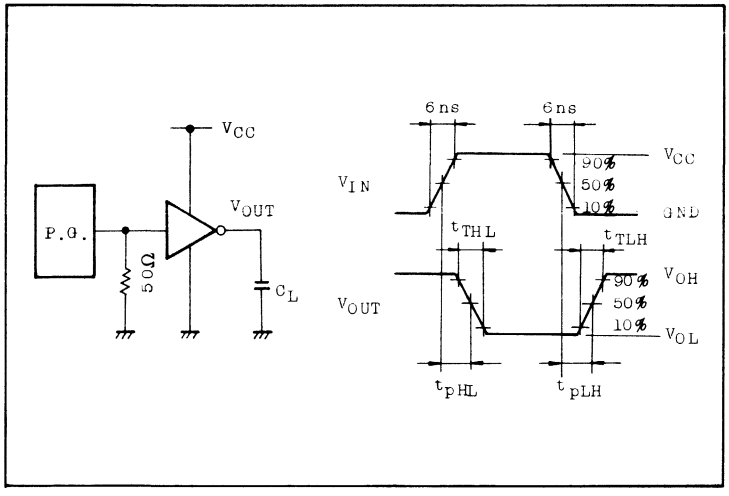
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH}		2.0	-	40	90	-	115	
	t_{PHL}		4.5	-	10	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	23	-	-	-	

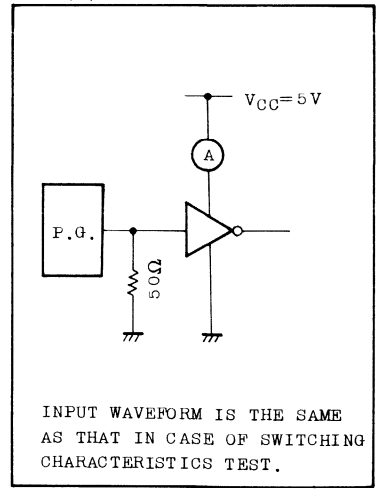
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HCT04P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT04P/F HEX INVERTER

The TC74HCT04 is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

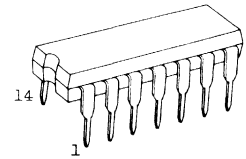
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

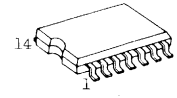
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS04



DIP14(3D14A-P)



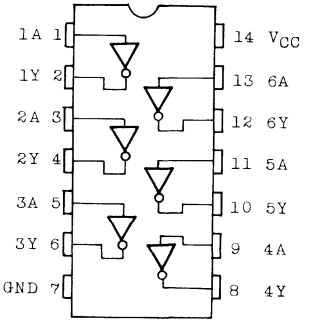
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

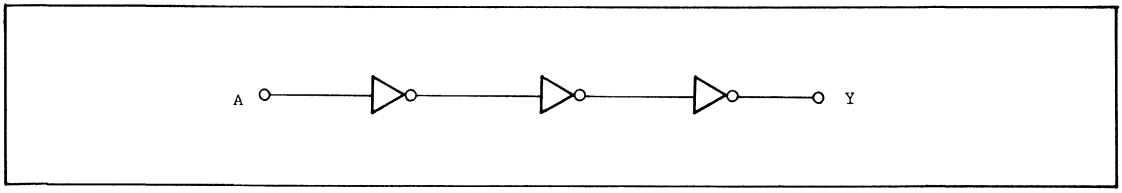
PIN ASSIGNMENT



(TOP VIEW)

TC74HCT04P/F

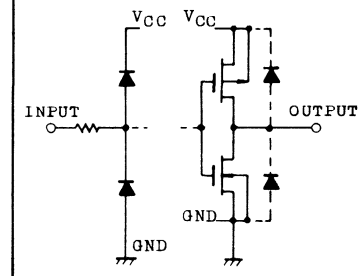
CIRCUIT DIAGRAM (per Circuit)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	V
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	1.0	-	10.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

TC74HCT04P/F

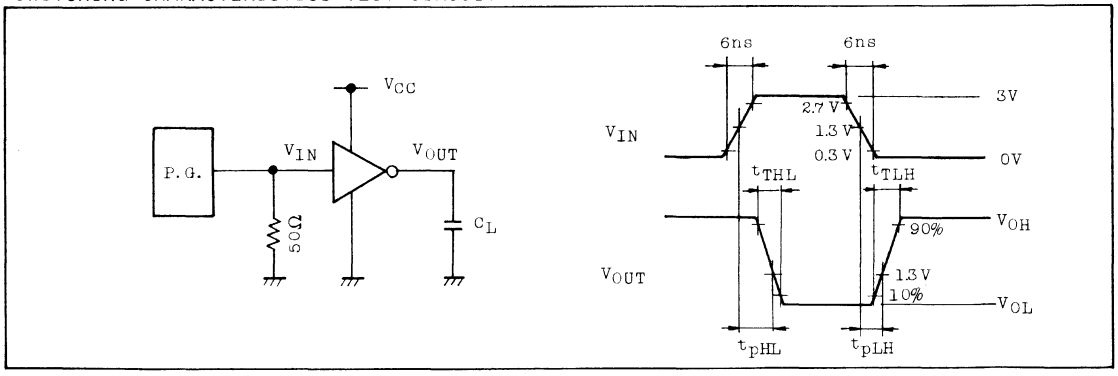
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	13	20	-	25	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	pF

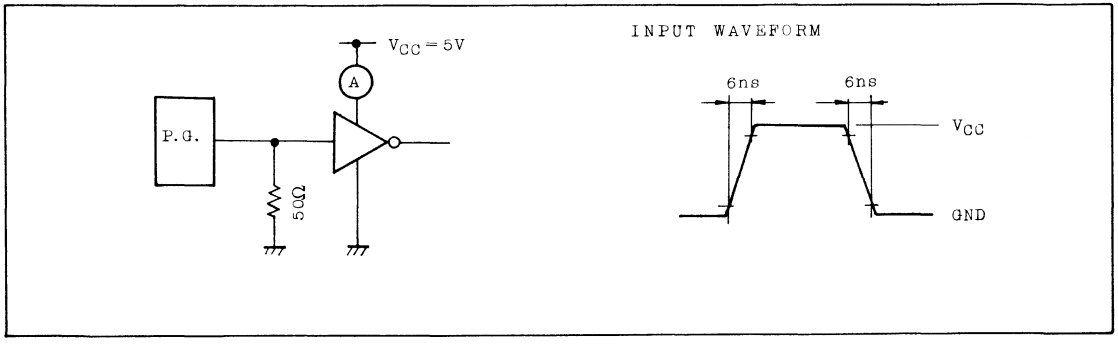
Note 1: C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCU04P/F

TC74HCU04P/F HEX INVERTER

The TC74HCU04 is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

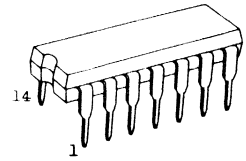
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

As the internal circuit is composed of single stage inverter, it can be applied for crystal oscillation.

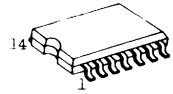
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=5ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....i_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=10% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS04

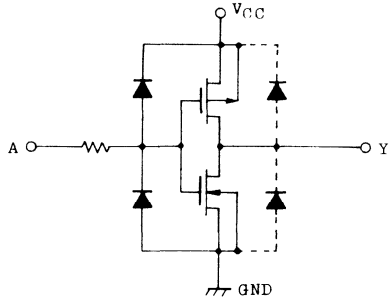


DIP14(3D14A-P)

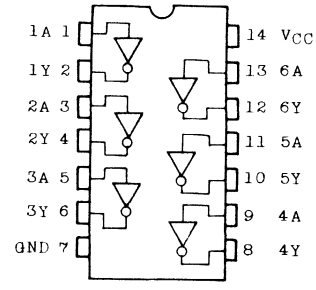


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HCU04P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.7	-	-	1.7	-	V
			4.5	3.6	-	-	3.6	-	
			6.0	4.8	-	-	4.8	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.3	-	0.3	V
			4.5	-	-	0.9	-	0.9	
			6.0	-	-	1.2	-	1.2	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}, I_{OH}=-20μA	2.0	1.8	2.0	-	1.8	-	V
			4.5	4.0	4.5	-	4.0	-	
			6.0	5.5	5.9	-	5.5	-	
		V_{IN}=GND, I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
		V_{IN}=GND, I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

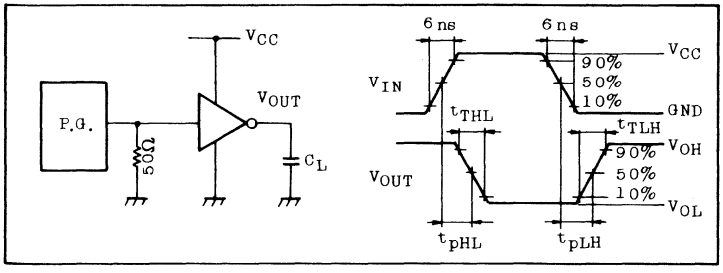
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$, I_{OL}=20μA	2.0	-	0.0	0.2	-	0.2	V
			4.5	-	0.0	0.5	-	0.5	
			6.0	-	0.1	0.5	-	0.5	
		$V_{IN}=V_{CC}$, I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
		$V_{IN}=V_{CC}$, I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

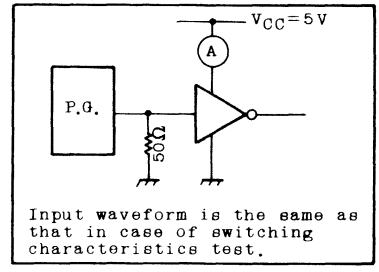
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	30	75	-	95	ns
	t_{pHL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	9	15	-	15	pF
Power Dissipation Capacitance	C_{PD}(1)			-	14	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC08P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC08P/F QUAD 2-INPUT AND GATE

The TC74HC08 is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C²MOS technology.

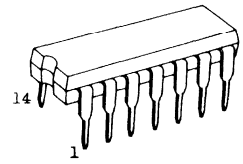
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output.

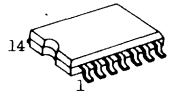
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS08

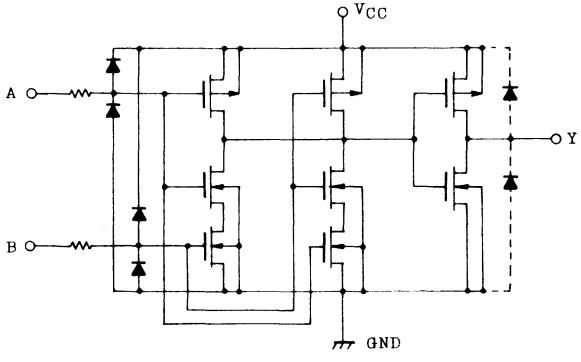


DIP14(3D14A-P)

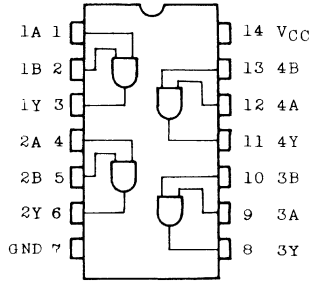


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC08P/F

DC ELECTRICAL CHARACTERISTICS

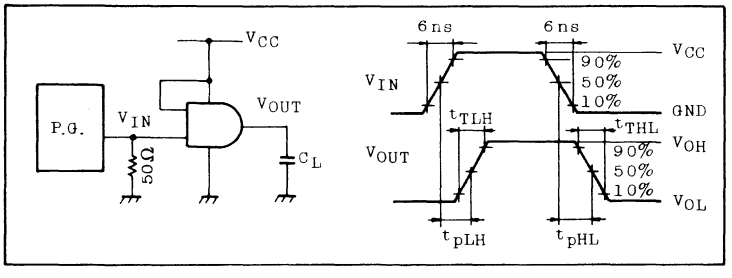
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0 1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

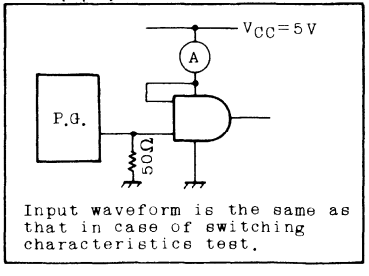
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
	t_{pHL}		4.5	-	10	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	21	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC10P/F

TC74HC10P/F TRIPLE 3-INPUT NAND GATE

The TC74HC10 is a high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

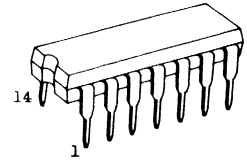
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

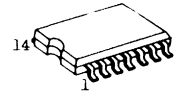
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS10

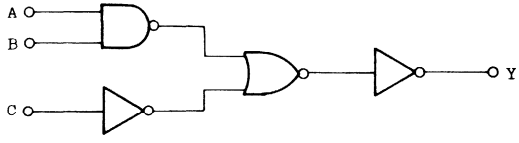


DIP14(3D14A-P)

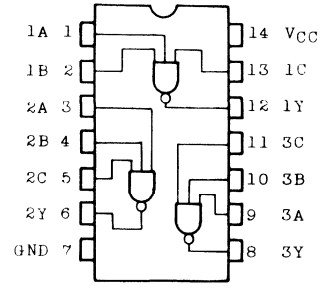


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC10P/F

ABSOLUTE MAXIMUM RATINGS

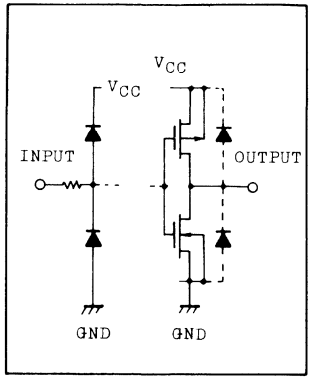
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

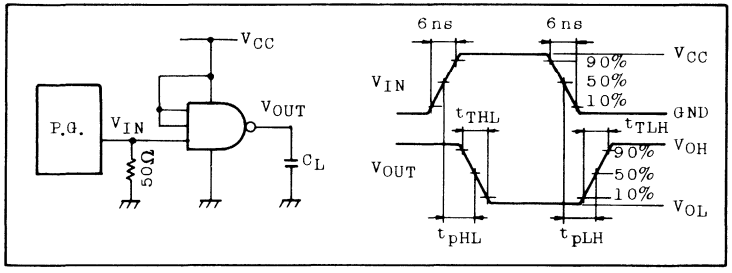
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

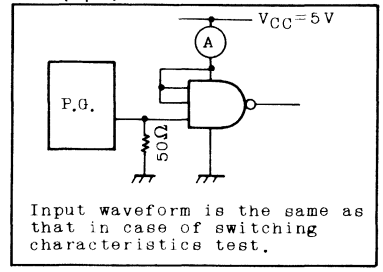
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	44	90	-	115	ns
	t_{PHL}		4.5	-	11	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC11P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC11P/F TRIPLE 3-INPUT AND GATE

The TC74HC11 is a high speed CMOS 3-INPUT AND GATE fabricated with silicon gate C²MOS technology.

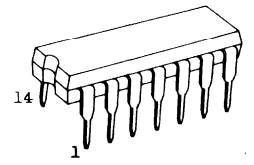
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

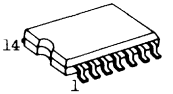
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS11

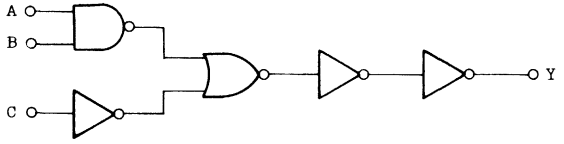


DIP14(3D14A-P)

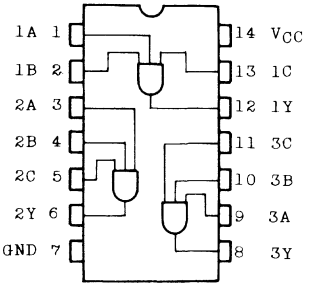


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMEMT



(TOP VIEW)

TC74HC11P/F

ABSOLUTE MAXIMUM RATINGS

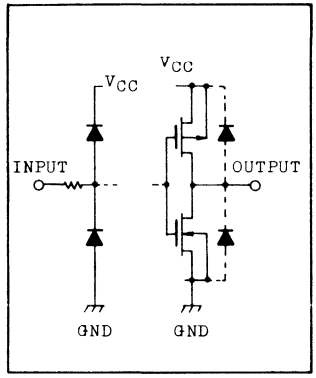
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC11P/F

DC ELECTRICAL CHARACTERISTICS

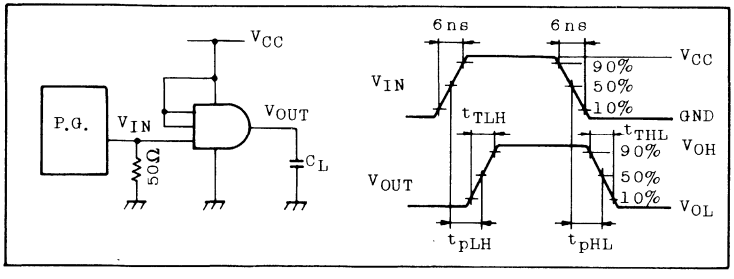
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

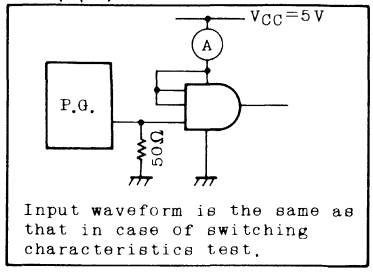
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	56	110	-	140	ns
			4.5	-	14	22	-	28	
	t_{pHL}		6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC14P/F

TC74HC14P/F HEX SCHMITT INVERTER

The TC74HC14 is a high speed CMOS HEX SCHMITT INVERTER fabricated with silicon gate C²MOS technology.

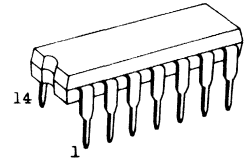
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as those of the TC74HCU04 but all the inputs have 20% V_{CC} hysteresis and with its schmitt trigger function, it can be applicable to line receivers which will receive slow input signals.

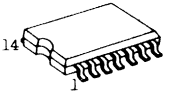
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_H=0.9V at V_{CC}=5V
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS14

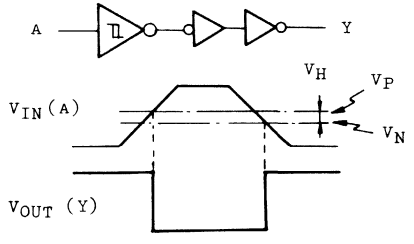


DIP14(3D14A-P)

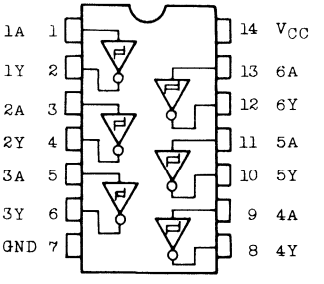


MFP14(F14GB-P)

LOGIC DIAGRAM, WAVEFORM



PIN ASSIGNMENT



(Top View)

TC74HC14P/F

ABSOLUTE MAXIMUM RATINGS

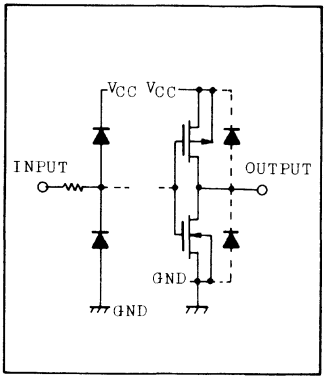
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Positive Threshold Voltage	V_P		2.0	0.8	1.25	1.5	0.8	1.5	V
			4.5	2.25	2.7	3.15	2.25	3.15	
			6.0	3.0	3.6	4.2	3.0	4.2	
Negative Threshold Voltage	V_N		2.0	0.4	0.75	1.0	0.4	1.0	V
			4.5	1.35	1.9	2.25	1.35	2.25	
			6.0	1.8	2.6	3.0	1.8	3.0	
Hysteresis Voltage	V_H		2.0	0.20	0.5	1.0	0.20	1.0	V
			4.5	0.4	0.8	1.4	0.4	1.4	
			6.0	0.6	1.0	1.7	0.6	1.7	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

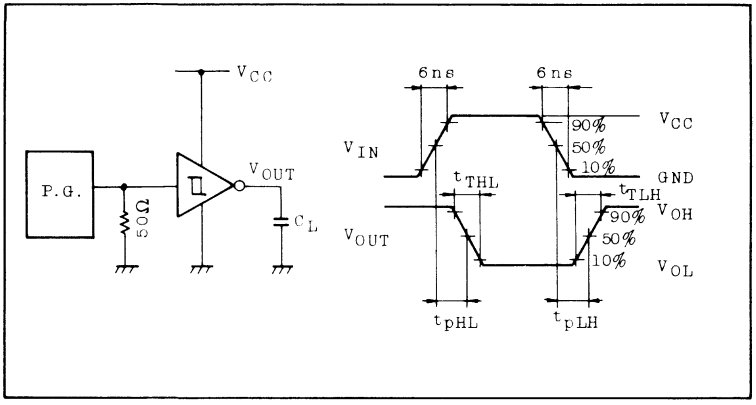
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	ns
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	31	-	-	-	

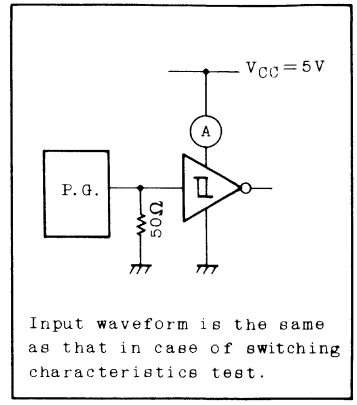
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}$=C_{PD}·V_{CC}·f_{IN}+I_{CC}/6 (per Gate)

TC74HC14P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



C_{PD} TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC20P/F

TC74HC20P/F DUAL 4-INPUT NAND GATE

The TC74HC20 is a high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

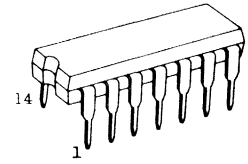
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

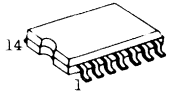
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS20

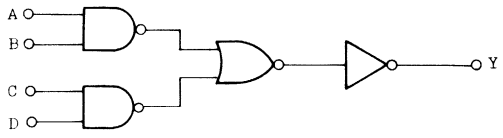


DIP14(3D14A-P)

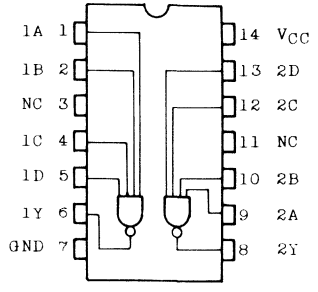


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC20P/F

ABSOLUTE MAXIMUM RATINGS

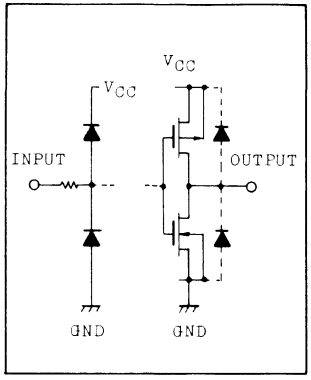
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

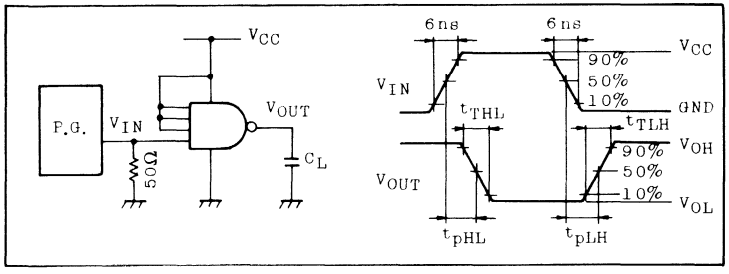
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

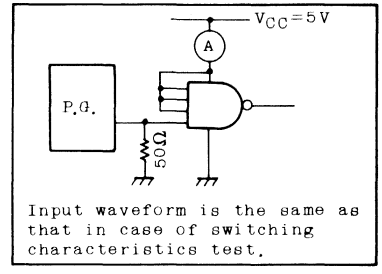
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	44	90	-	115	ns
			4.5	-	11	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC21P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC21P/F DUAL 4-INPUT AND GATE

The TC74HC21 is a high speed CMOS 4-INPUT AND GATE fabricated with silicon gate C²MOS technology.

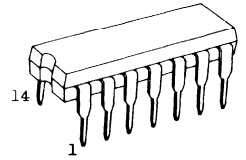
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

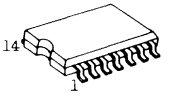
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS21

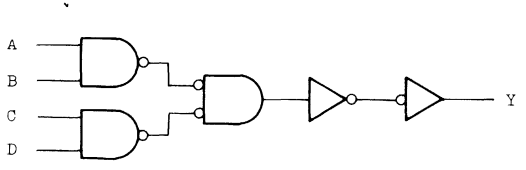


DIP14(3D14A-P)

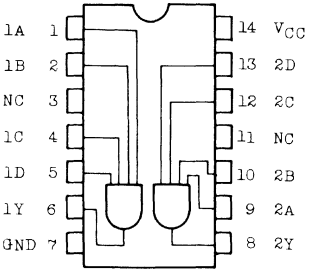


MFP14(F14GB-P)

LOGIC DIAGRAM (per Gate)



PIN ASSIGNMENT



(Top View)

TC74HC21P/F

ABSOLUTE MAXIMUM RATINGS

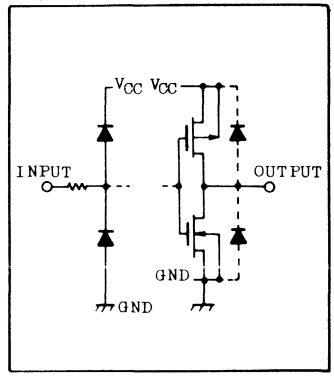
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC21P/F

DC ELECTRICAL CHARACTERISTICS

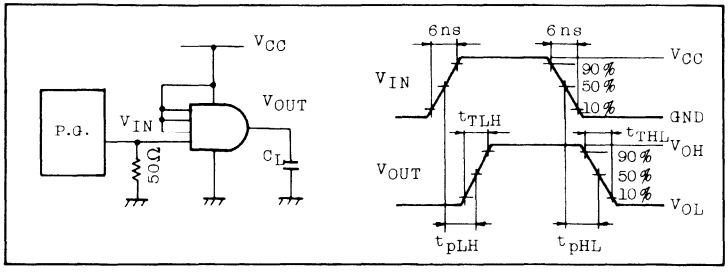
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

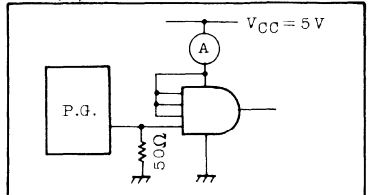
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	ns
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	29	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC27P/F

TC74HC27P/F TRIPLE 3-INPUT NOR GATE

The TC74HC27 is a high speed CMOS 3-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

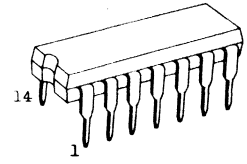
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

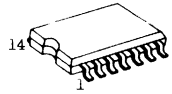
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$-2V ~6V
- Pin and Function Compatible with 74LS27

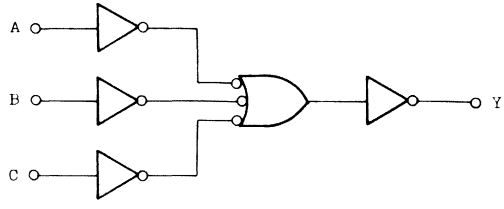


DIP14(3D14A-P)

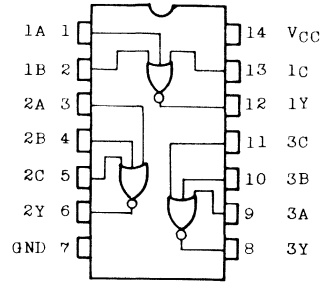


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC27P/F

ABSOLUTE MAXIMUM RATINGS

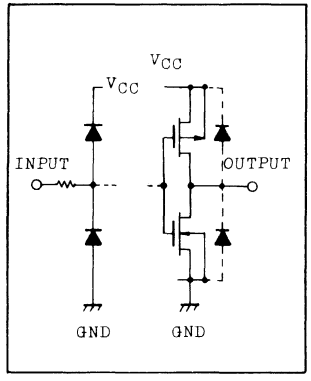
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

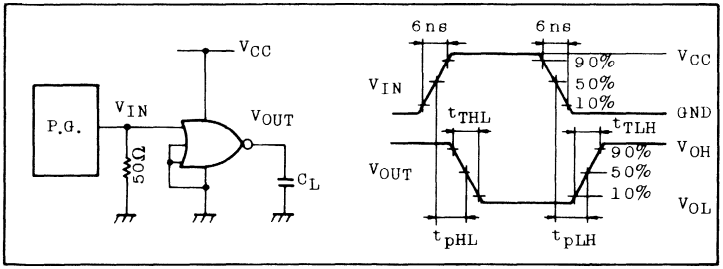
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

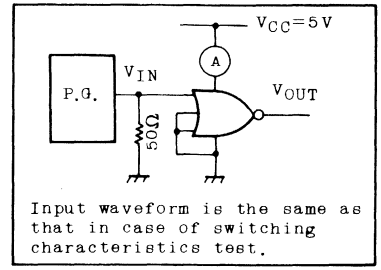
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	44	90	-	115	ns
			4.5	-	11	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC30P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC30P/F 8-INPUT NAND GATE

The TC74HC30 is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

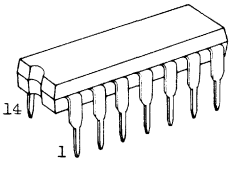
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 5 stages including buffer output, which enables high noise immunity and stable output.

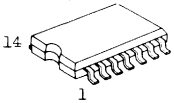
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=12ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA (Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA (Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS30.



DIP14(3D14A-P)



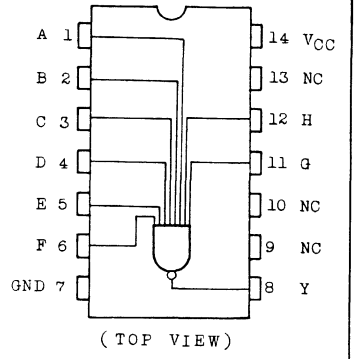
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

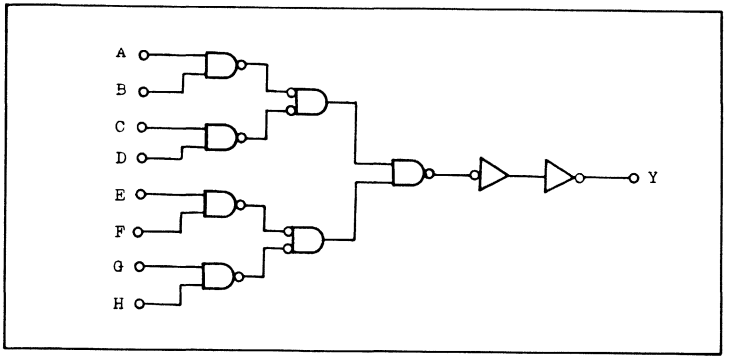


(TOP VIEW)

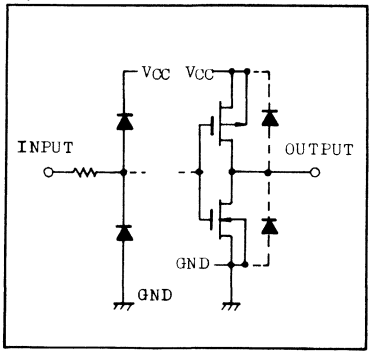
NC : No Connection

TC74HC30P/F

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC30P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

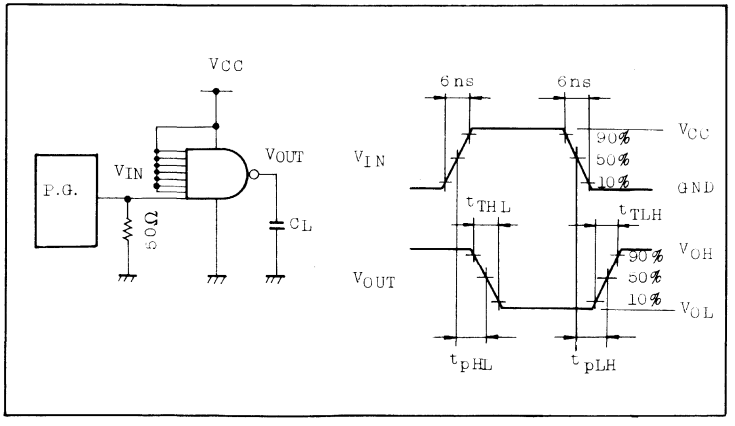
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

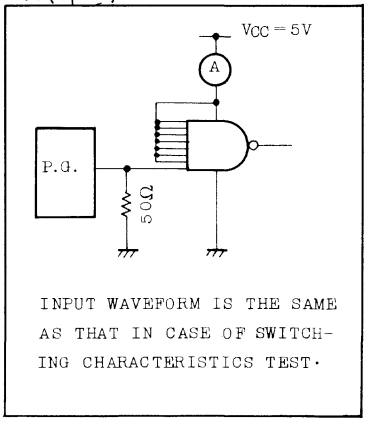
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	64	125	-	155	
	t_{pHL}		4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC32P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC32P/F QUAD 2-INPUT OR GATE

The TC74HC32 is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C²MOS technology.

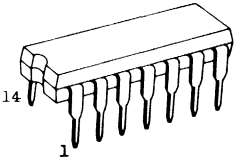
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output.

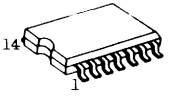
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS32

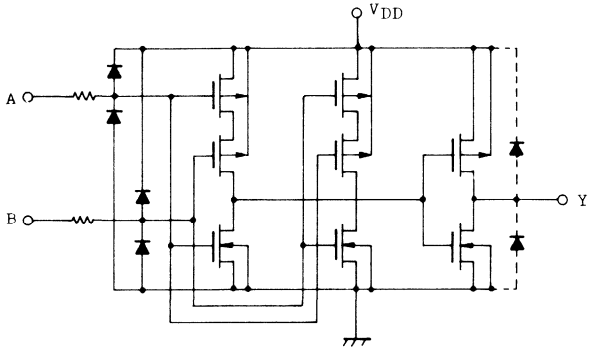


DIP14(3D14A-P)

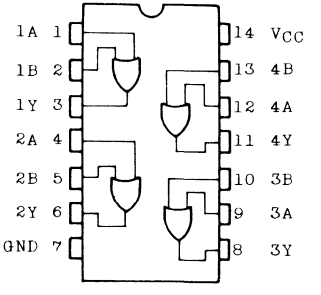


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC32P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

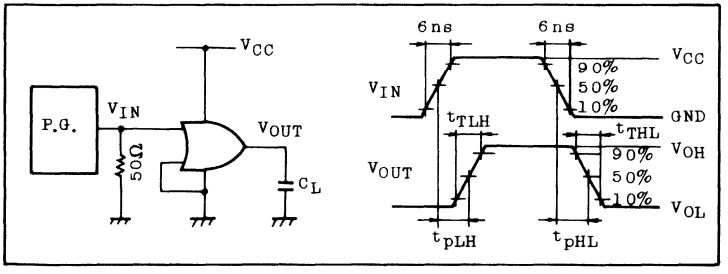
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

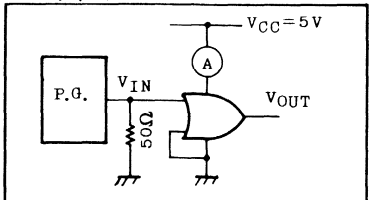
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	6	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	23	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC42P/F

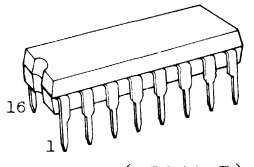
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC42P/F BCD-TO-DECIMAL DECODER

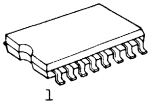
The TC74HC42 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining CMOS low power dissipation.
A BCD code applied to the four inputs (A - D) provides a low level at the selected one of ten decimal decoded outputs. A illegal BCD code such as eleven thru fifteen gives a high level at all outputs. This device also can be used as 3-to-8 LINE DECODER, when D input is assigned as a disable input.
This device is useful for code conversion, address decoding, memory selection, demultiplexing, or readout decoding.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=17ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V∿6V
- Pin and Function Compatible with 74LS42



DIP16(3D16A-P)



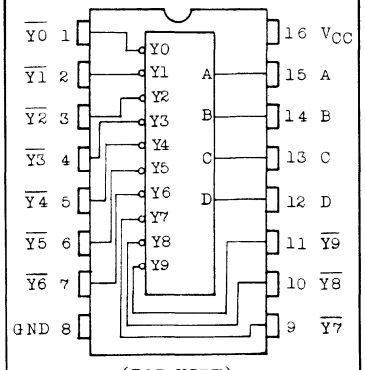
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

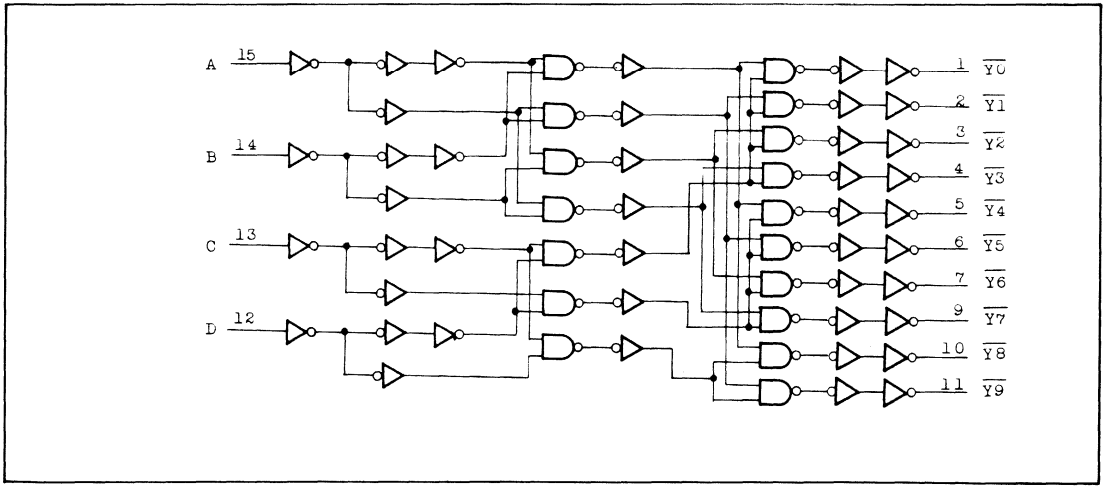
PIN·ASSIGNMENT



TRUTH TABLE

CODE No.	BCD INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DIAGRAM

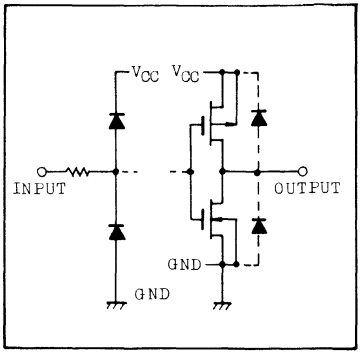


TC74HC42P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

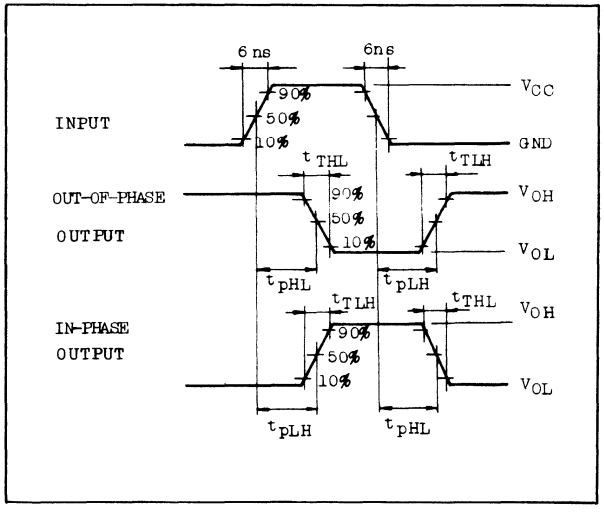
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH} t_{PHL}		2.0	-	76	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	67	-	-	-	

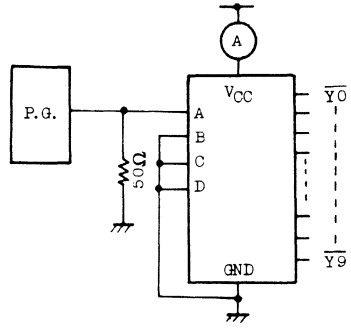
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC51P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC51P/F DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

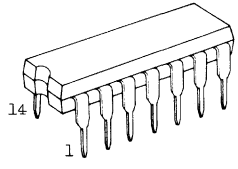
The TC74HC51 is a high speed CMOS 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE fabricated with silicon gate CMOS technology.

It acheives the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains a 2-WIDE 2-INPUT AND-OR-INVERT GATE and a 2-WIDE 3-INPUT AND-OR-INVERT GATE.

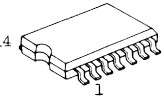
The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS51



DIP14(3D14A-P)



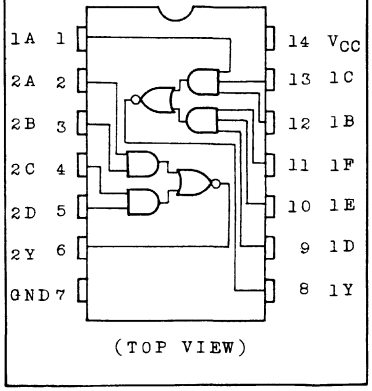
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

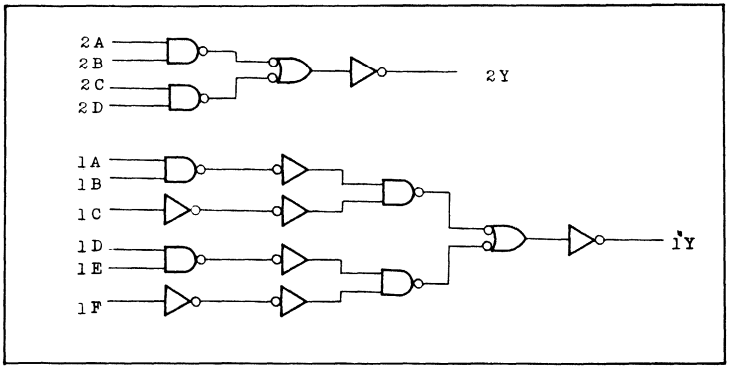
* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

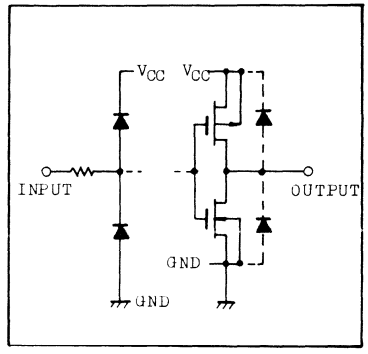
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC51P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

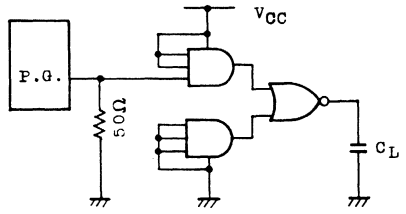
AC ELECTRICAL CAHRACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

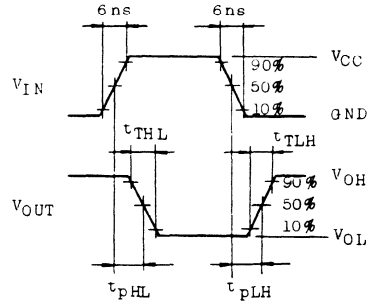
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40~85°C MIN.	-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
	t_{pHL}		6.0	-	11	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	33	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

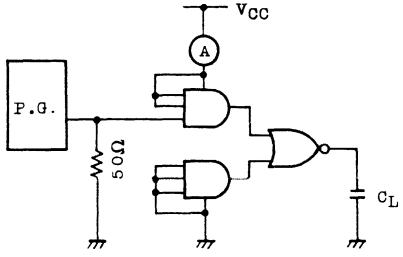
$$I_{DD(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT





$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC73P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC73P/F DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC73 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

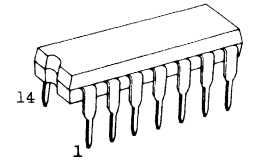
In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.

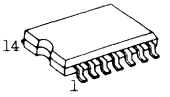
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=55MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=2μA(Max.) (Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS73



DIP14(3D14A-P)



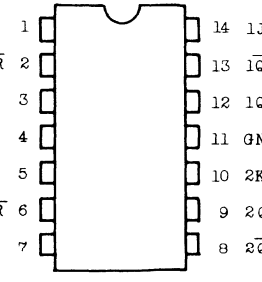
MFP14(F14GB-P)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	-
H	H	L	↓	H	L	-
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X: Don't care

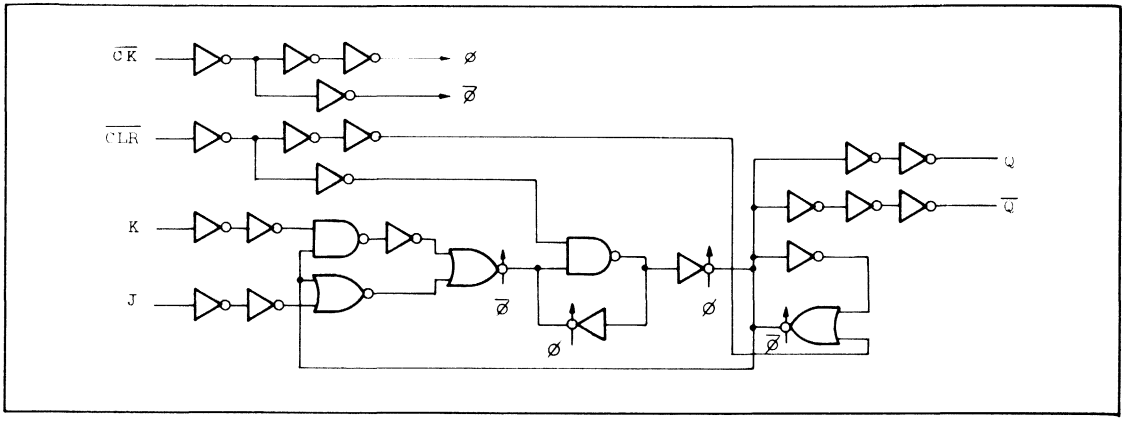
PIN ASSIGNMENT



(Top View)

TC74HC73P/F

LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)

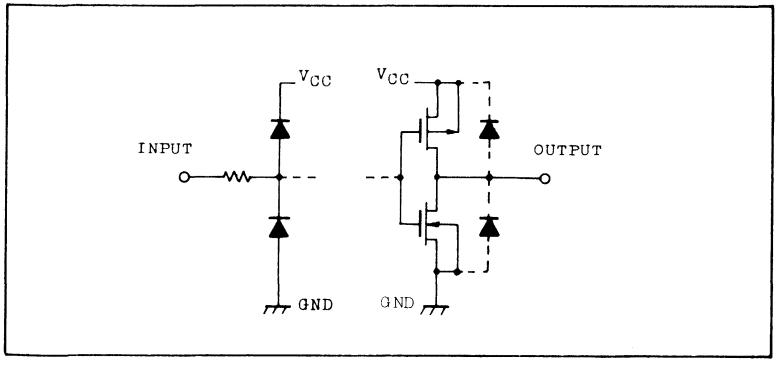


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC73P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

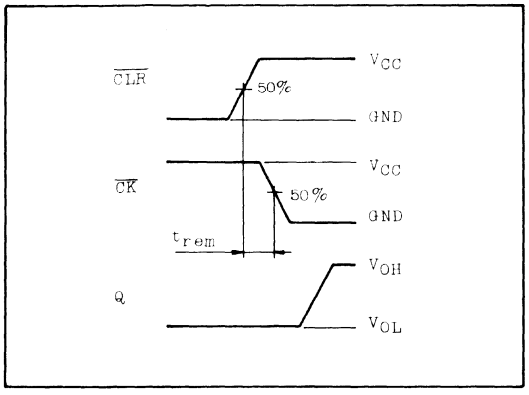
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	52	-	24	-	
			6.0	35	61	-	28	-	
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	42	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

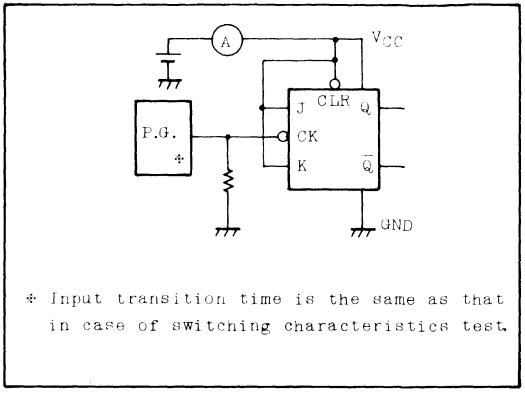
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \text{ (per FF)}$$

TC74HC73P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

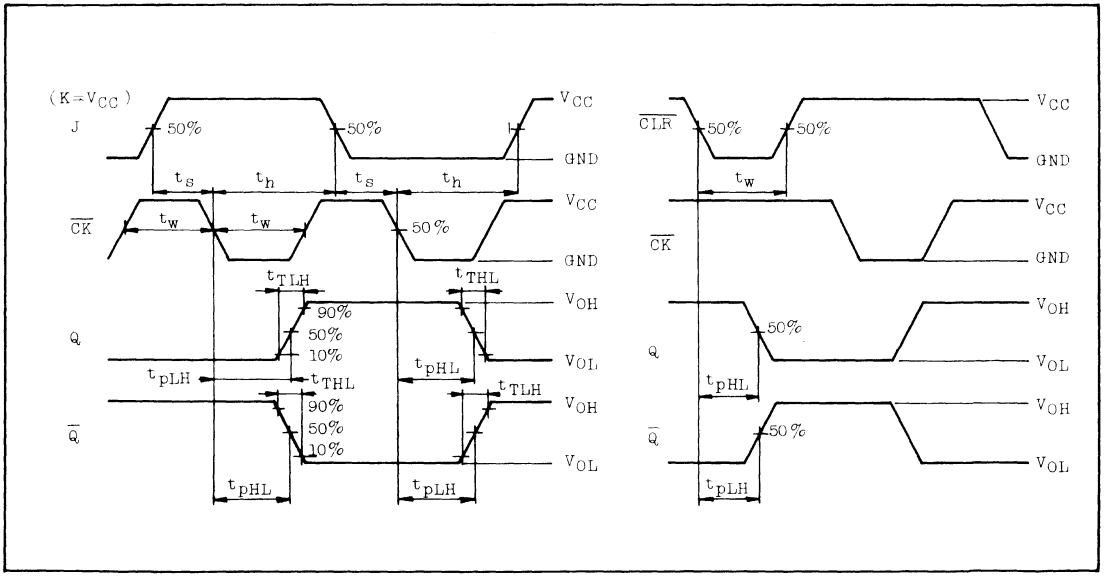


$I_{CC(opr)}$ TEST CIRCUIT



* Input transition time is the same as that in case of switching characteristics test.

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC74P/F

TC74HC74P/F DUAL D FLIP FLOP WITH PRESET AND CLEAR

The TC74HC74 is a high speed CMOS DUAL D FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

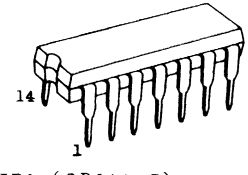
Signal given D INPUT is transferred to Q OUTPUT during the positive going transition of the clock pulse.

CLEAR and PRESET are independent of the clock and accomplished by "L" level at the appropriate input.

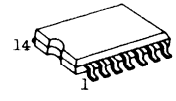
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS74



DIP14(3D14A-P)



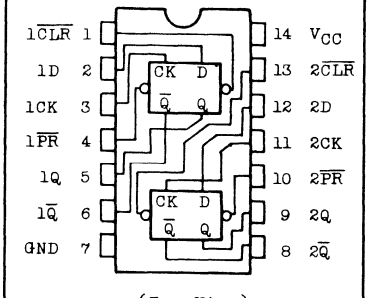
MFP14(F14GB-P)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	-
H	H	L	↓	L	H	-
H	H	H	↓	H	L	-
H	H	X	↑	Qn	$\overline{Q}$n	NO CHANGE

X: Don't care

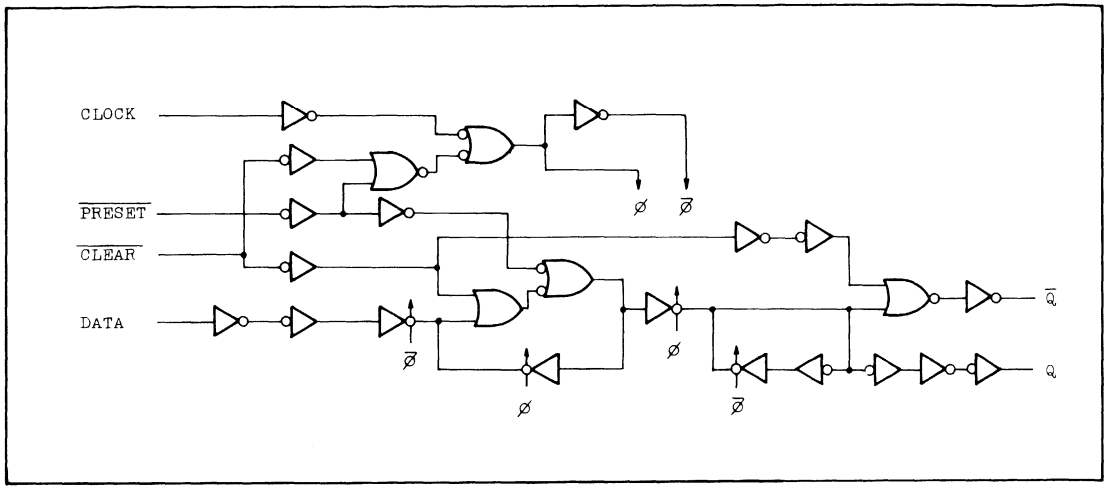
PIN ASSIGNMENT



(Top View)

TC74HC74P/F

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

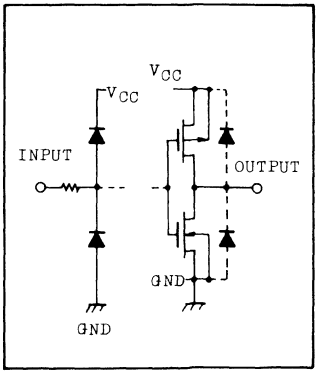
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	ns
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	104	205	-	255	ns
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	

TC74HC74P/F

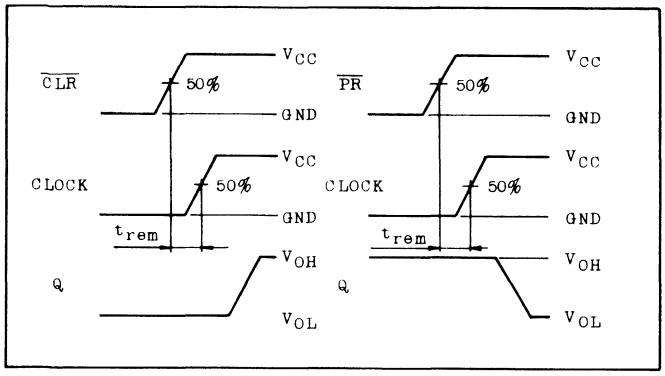
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	27	49	-	22	-	
			6.0	32	58	-	26	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	45	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	53	-	-	-	

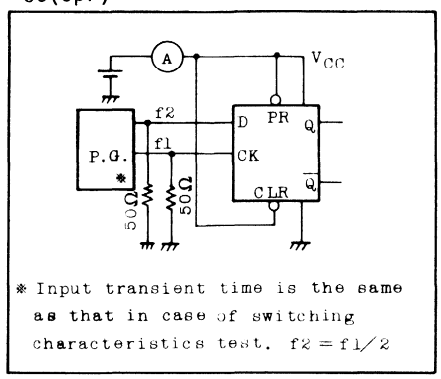
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \text{ (per FF)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

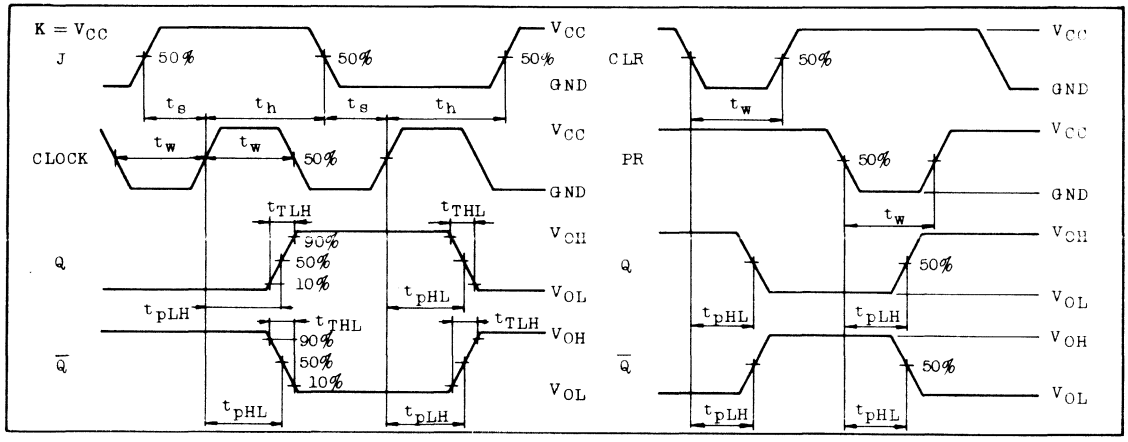


I_{CC}(opr) TEST CIRCUIT



* Input transient time is the same as that in case of switching characteristics test. f2 = f1/2

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC75P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

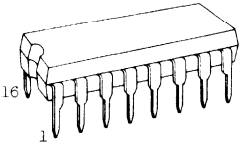
TC74HC75P/F 4-BIT D-TYPE LATCH

The TC74HC75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C²MOS technology.

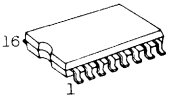
It achieves the high speed operation similar to equivalent LS TTL while maintaining the CMOS low power dissipation.

It contains two groups of 2-bit latches controled by a enable input (G1·2 or G3·4). And those two latch groups can be used in the different circuits.

Each latch has Q and $\overline{Q}$ outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at a time is retained at the outputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

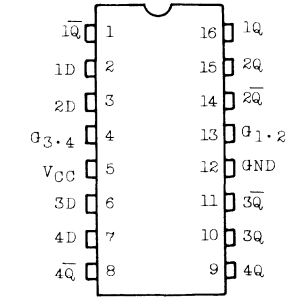


MFP16(F16GC-P)

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{HIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS75

PIN ASSIGNMENT



(Top View)

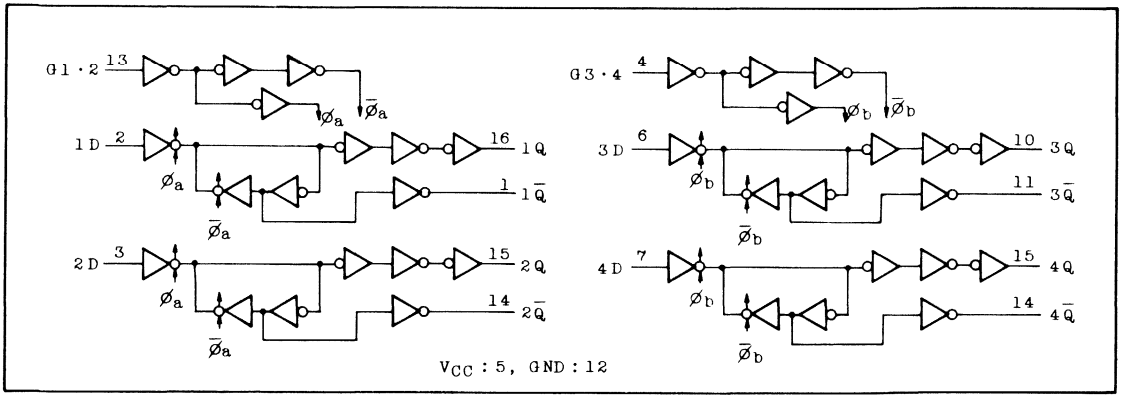
TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	-
H	H	H	L	-
X	L	Q_n	$\overline{Q}_n$	LATCH

X : Don't care

TC74HC75P/F

LOGIC DIAGRAM

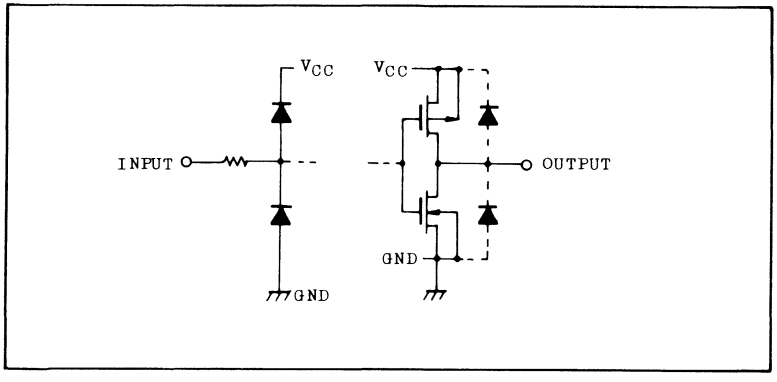


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC75P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

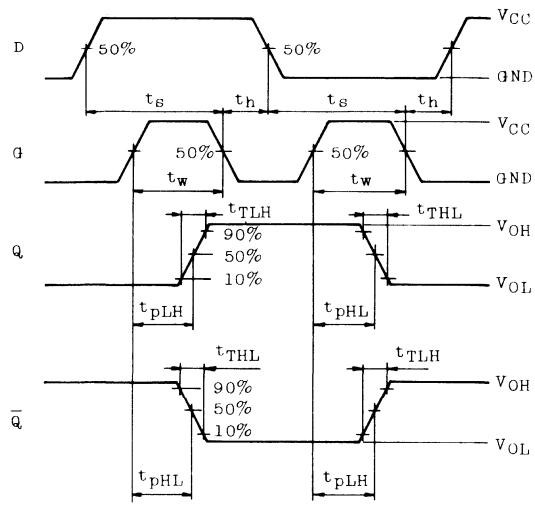
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Minimum Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	4	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	48	-	-	-	

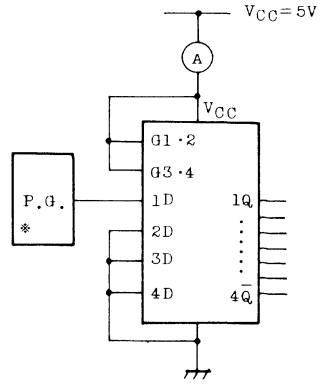
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}/4$ (per Latch)

TC74HC75P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC76P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC76P/F DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC76 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

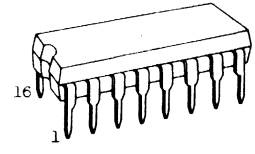
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

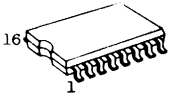
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS76.



DIP16(3D16A-P)



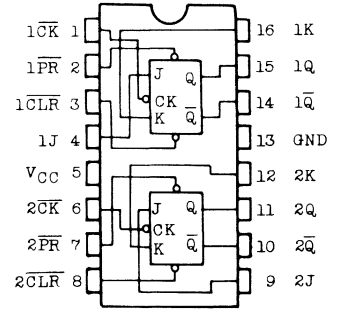
MFP16(F16GC-P)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: Don't care

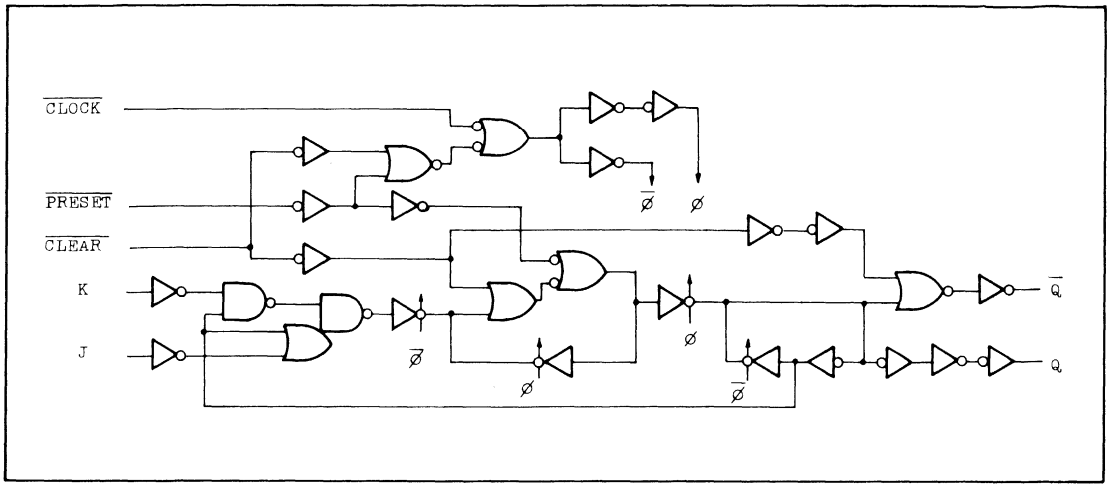
PIN ASSIGNMENT



(TOP VIEW)

TC74HC76P/F

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

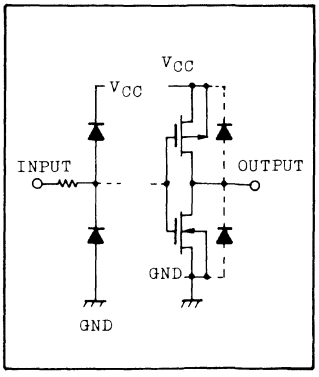
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	ns
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	

TC74HC76P/F

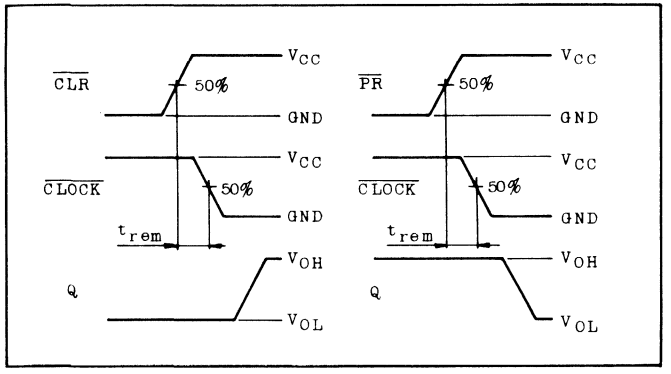
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	35	75	-	95	
			4.5	-	9	20	-	19	
			6.0	-	8	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

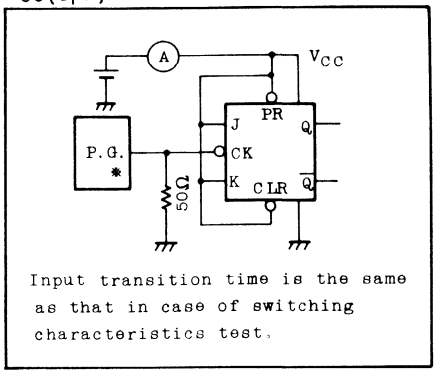
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \text{ (per FF)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

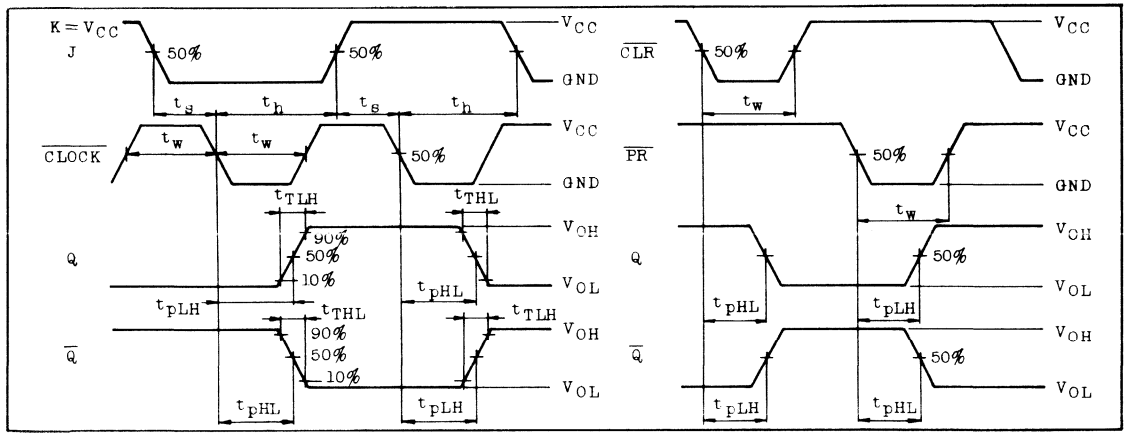


$I_{CC(opr)}$ TEST CIRCUIT



Input transition time is the same as that in case of switching characteristics test.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC77P/F

CMOS DIGITAL INTEGRATED CIRCUIT

TC74HC77P/F 4-BIT D-TYPE LATCH

The TC74HC77P is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate CMOS technology.

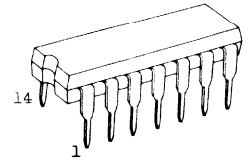
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains two groups of 2-bit latches controled by a enable input (G1·2 or G3·4). And these two latch groups can be used in the different circuits.

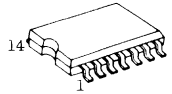
The data applied to the data inputs (1D, 2D or 3D, 4D) are transfered to the Q outputs (1Q, 2Q or 3Q, 4Q) respectively when the enable input (G1·2 or G3·4) is taken high and the Q outputs will follow the data inputs as long as the enable input is kept high.

When the enable input is taken low, the information data applied to the data inputs at a time are retained at the Q outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14(3D14A-P)

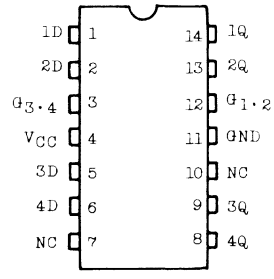


MFP14(F14GB-P)

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS77

PIN ASSIGNMENT

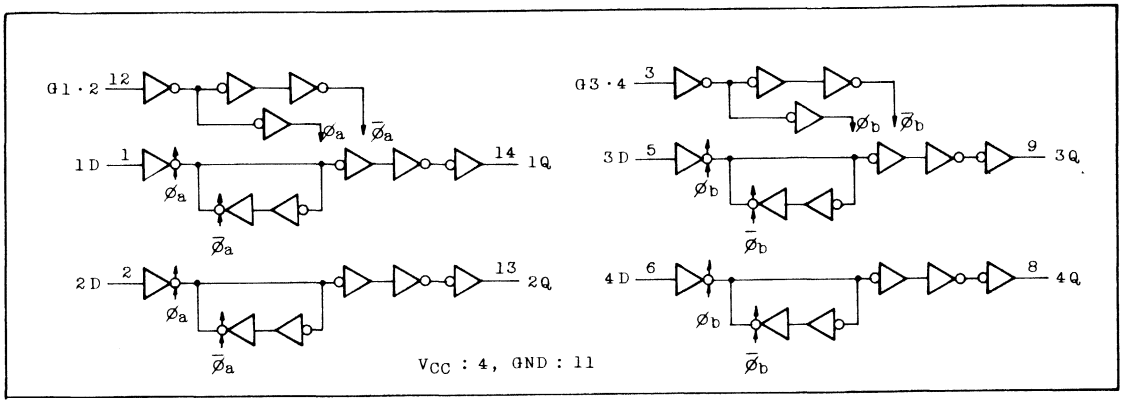


(Top View)

NC : No Connection

TC74HC77P/F

LOGIC DIAGRAM

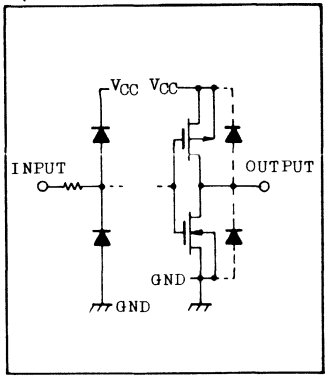


TRUTH TABLE

INPUTS		OUTPUT	FUNCTION
D	G	Q	
L	H	L	-
H	H	H	-
X	L	Q_n	Latch

X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC77P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IN}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

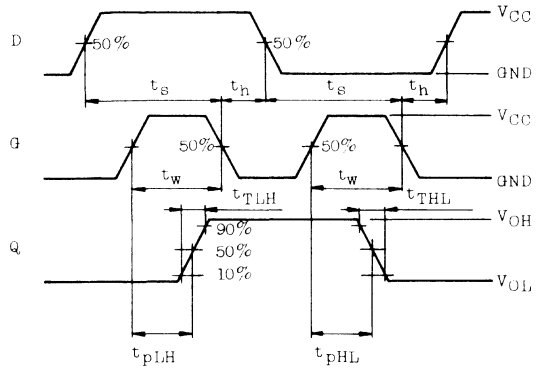
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q)	t_{pLH} t_{pHL}		2.0	-	75	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Minimum Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	4	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

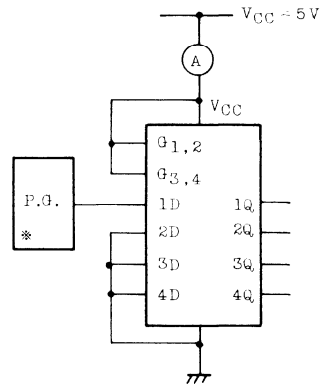
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Latch)

TC74HC77P/F

AC CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



* Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

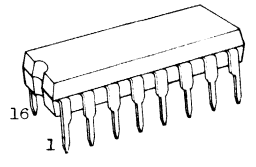
TC74HC85P/F

TC74HC85P/F 4-BIT MAGNITUDE COMPARATOR

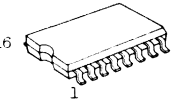
The TC74HC85 is a high speed CMOS 4-BIT MAGNITUDE COMPARATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This comparator compares two 4-bit words and provides a high voltage level on one of the A > Bout, A = Bout and A < Bout output. The comparing bit number is easily expanded by cascading several devices as shown at the typical application. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=24ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS85



DIP16(3D16A-P)



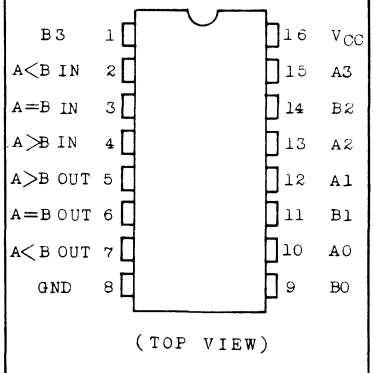
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

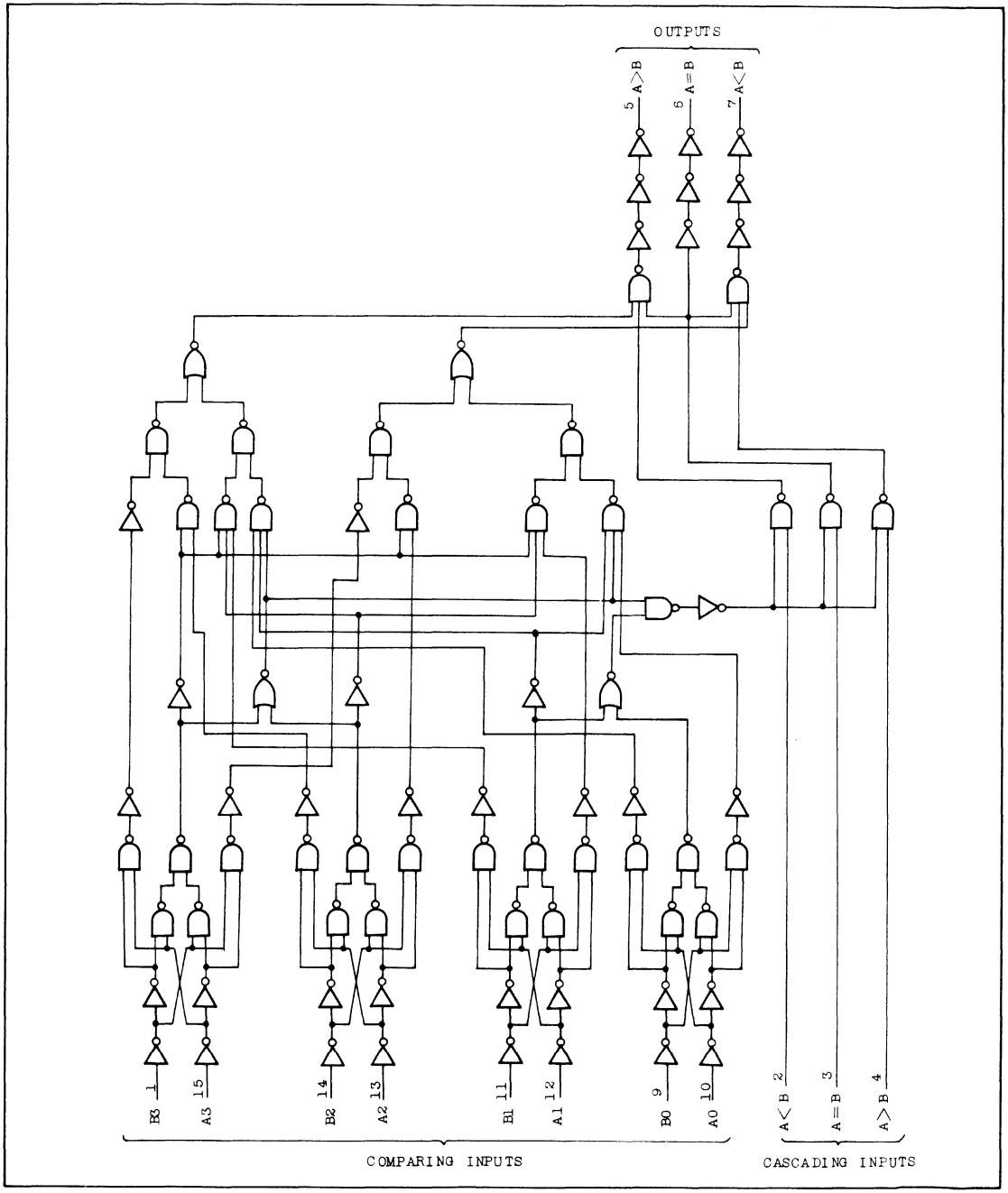
PIN ASSIGNMENT



(TOP VIEW)

TC74HC85P/F

LOGIC DIAGRAM



TC74HC85P/F

TRUTH TABLE

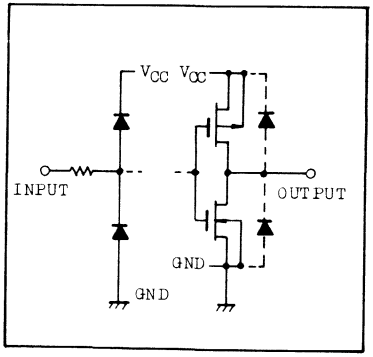
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3 , A2=B2 , A1=B1 , A0=B0				L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC85P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

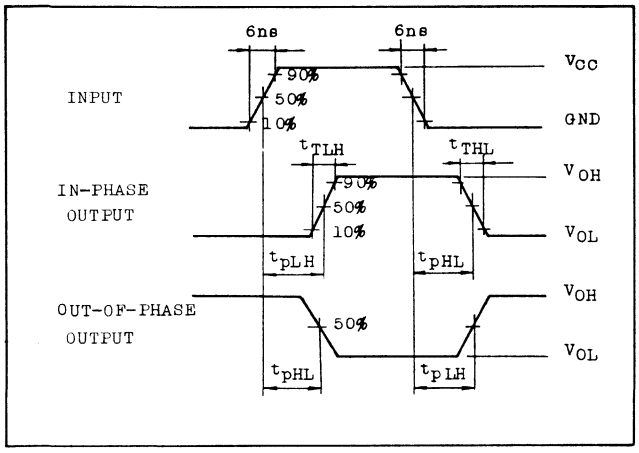
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40∿85°C MIN.	-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, B - OUT)	t_{PLH} t_{PHL}		2.0	-	112	230	-	290	
			4.5	-	28	46	-	58	
			6.0	-	24	39	-	49	
Propagation Delay Time (CASCADE - OUT)	t_{PLH} t_{PHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

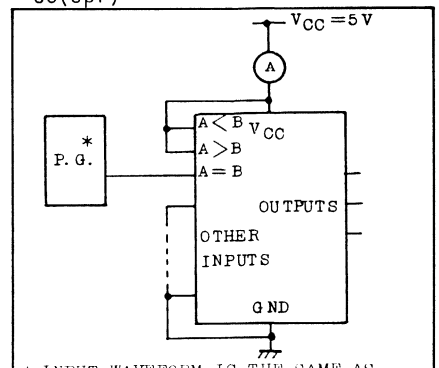
$$I_{CC(opr.)}=C_{PD} \cdot V_{GC} \cdot f_{IN} + I_{CC}$$

TC74HC85P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



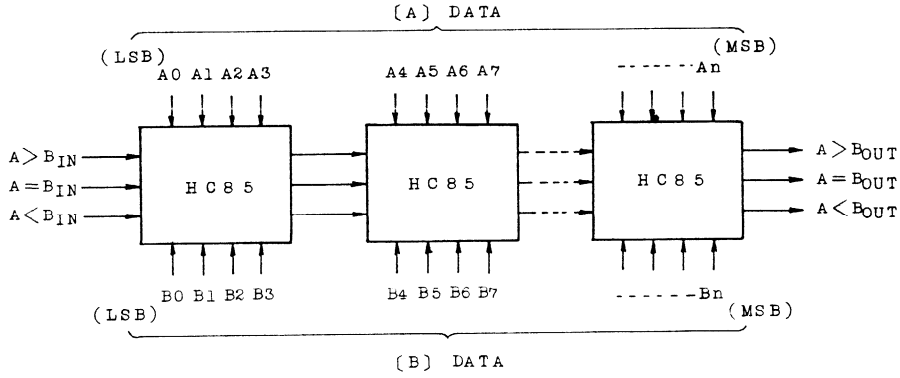
$I_{CC(opr)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

N-BIT CASCADE CONNECTION



COMPARING INPUTS	CASCADING INPUTS			OUTPUTS		
	A>B	A=B	A<B	A>B	A=B	A<B
(A) > (B)	X	X	X	H	L	L
(A) = (B)	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
(A) < (B)	X	X	X	L	L	H

X : DON'T CARE

TC74HC86P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC86P/F QUAD EXCLUSIVE OR GATE

The TC74HC86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate C^2MOS technology.

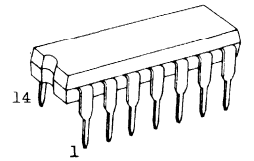
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Input and output buffer are installed, which enables high noise immunity and stable output.

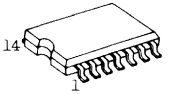
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS86

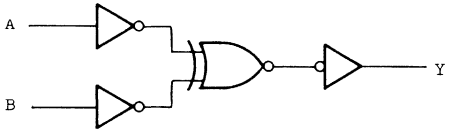


DIP14(3D14A-P)

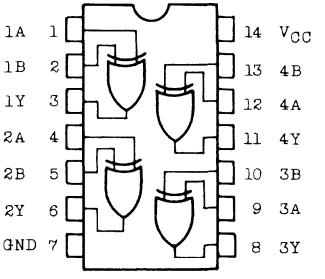


MFP14(F14GB-P)

LOGIC DIAGRAM (per Gate)



PIN ASSIGNMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

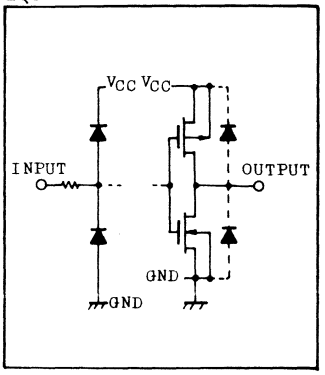
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC86P/F

DC ELECTRICAL CHARACTERISTICS

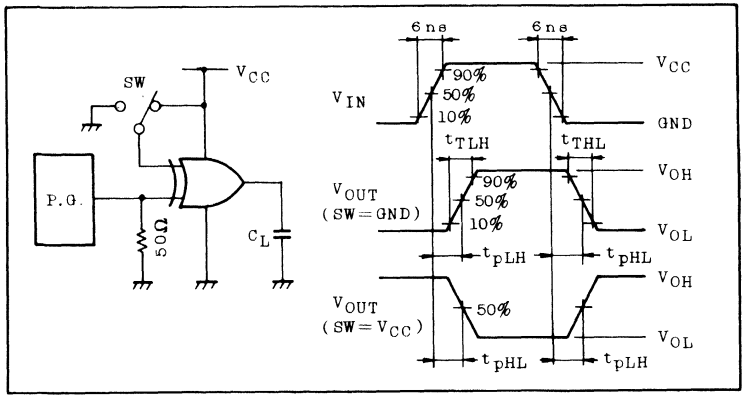
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

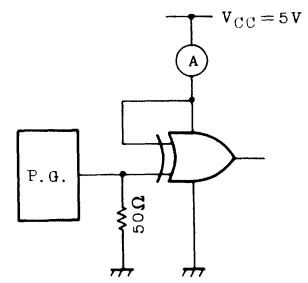
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	120	-	150	ns
			4.5	-	16	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC107P/F

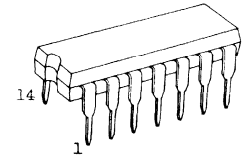
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC107P/F DUAL J-K FLIP FLOP WITH CLEAR

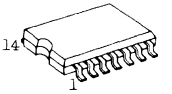
The TC74HC107 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=52MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=2μA(Max.) (Ta=25°C)
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS107



DIP14(3D14A-P)



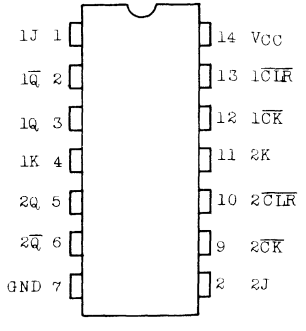
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Doide Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{STG}	-65∿150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

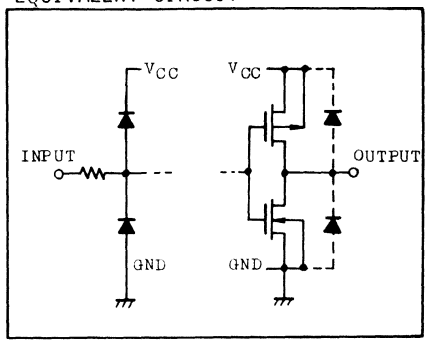


(TOP VIEW)

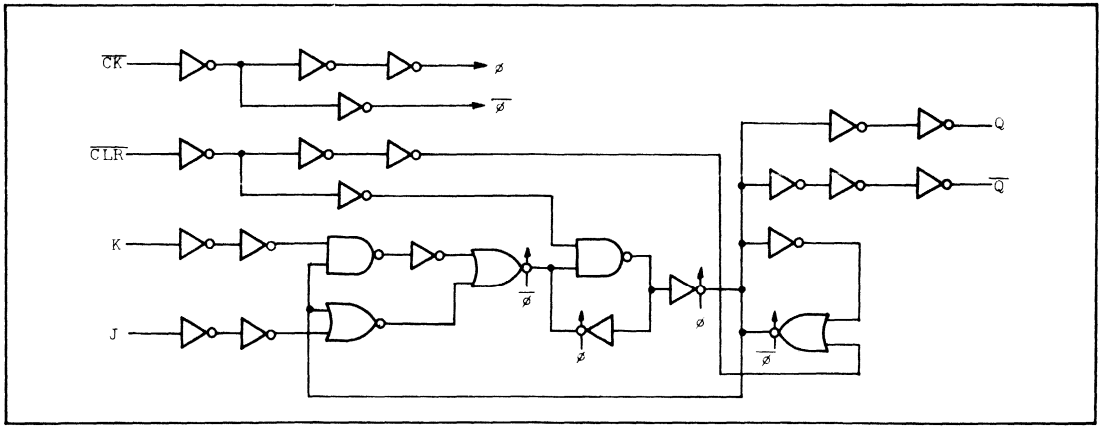
TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	—
H	H	L	↓	H	L	—
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

INPUT and OUTPUT
EQUIVALENT CIRCUIT



LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

TC74HC107P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	48	-	24	-	
			6.0	35	56	-	28	-	

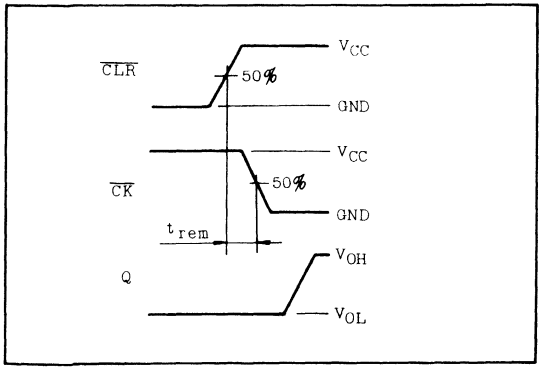
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

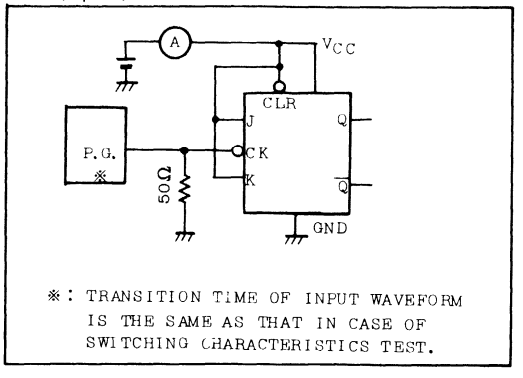
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



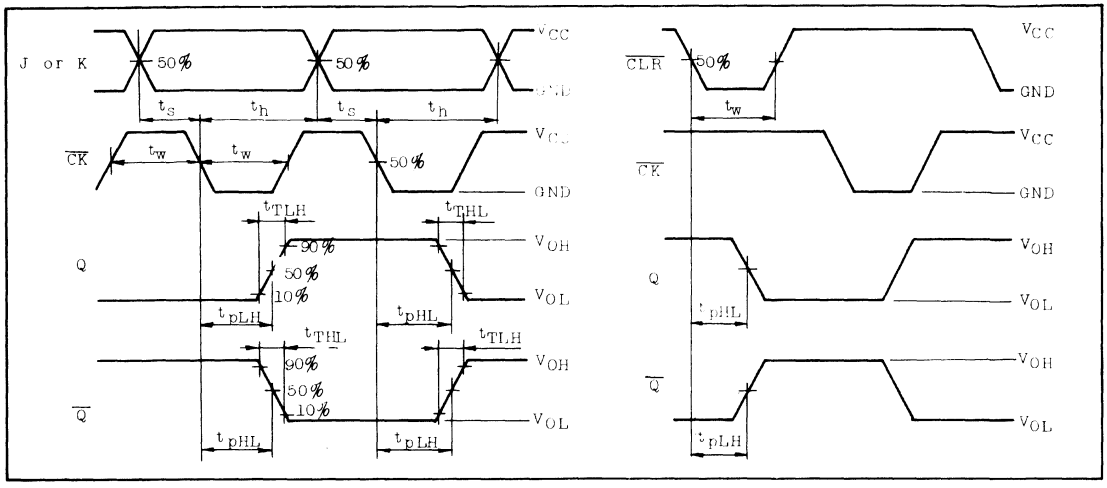
$I_{CC(opr.)}$ TEST CIRCUIT



※ : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC107P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC109P/F

TC74HC109P/F DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC109 is a hgih speed CMOS DUAL J-$\overline{K}$ FLIP FLOP fabricated with silicon gate C²MOS technology.

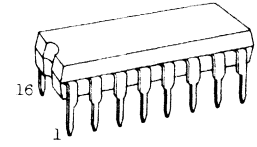
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and $\overline{K}$ input this device changes state on positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

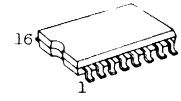
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS109



DIP16(3D16A-P)



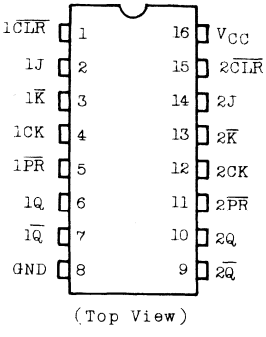
MFP16(F16GC-P)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	L	↓	L	H	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

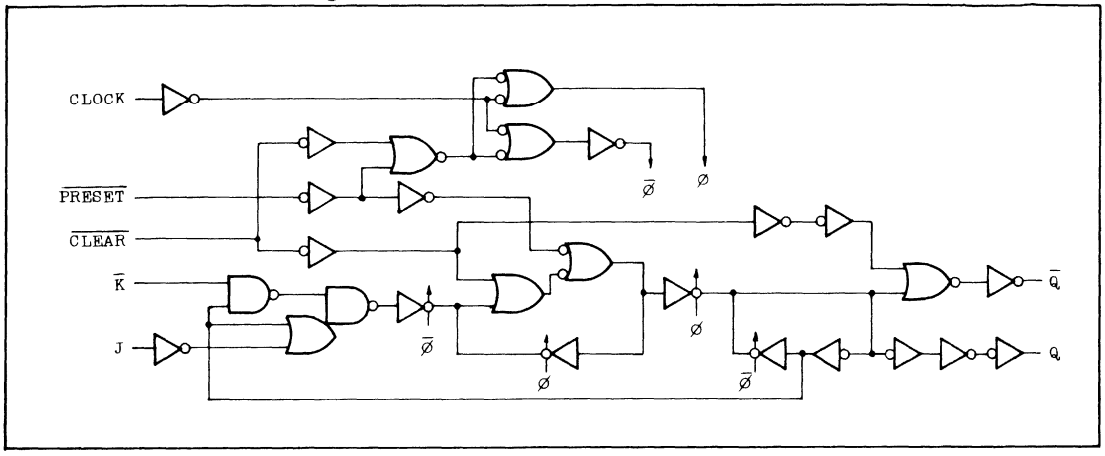
PIN ASSIGNMENT



(Top View)

TC74HC109P/F

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

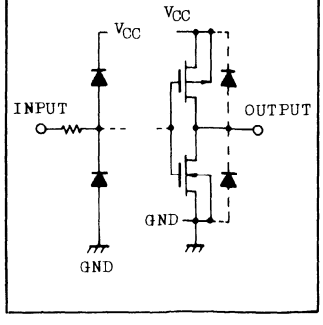
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~500 (V_{CC}=4.5V) 0~400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	ns
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	ns
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	

TC74HC109P/F

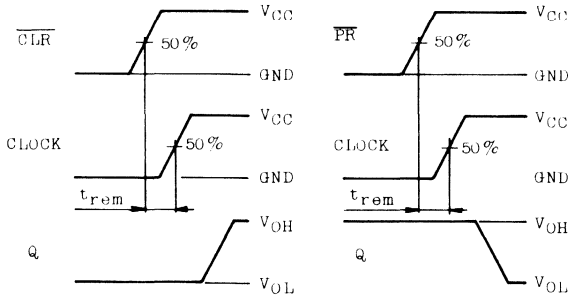
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

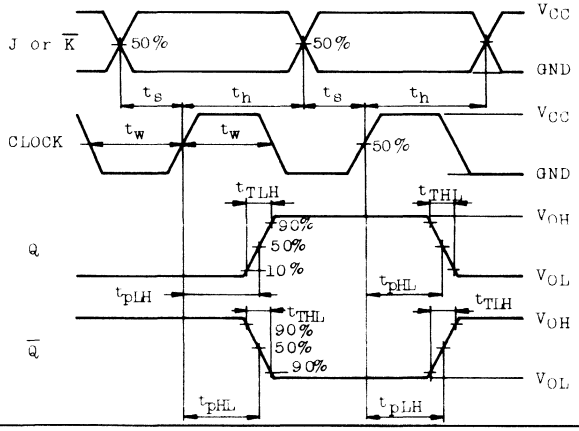
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	57	-	24	-	
			6.0	35	67	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	5	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

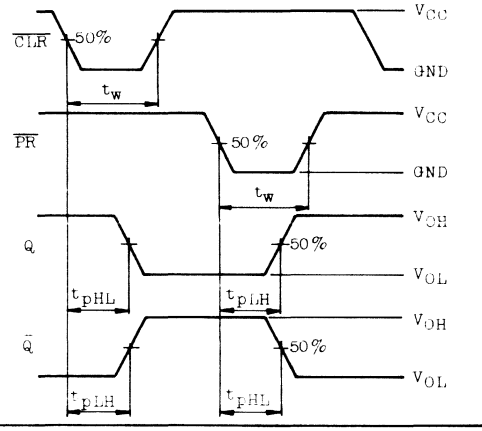
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \quad \text{(Per FF)}$$

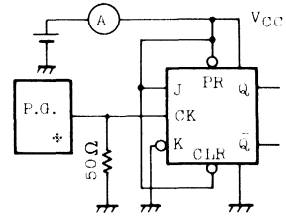
SWITCHING CHARACTERISTICS TEST WAVEFORM







I_{CC}(opr) TEST CIRCUIT



Input transition time is the same as that in case of switching characteristics test.

TC74HC112P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC112P/F DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC112 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

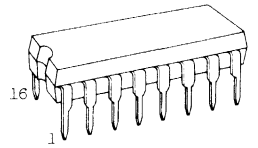
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

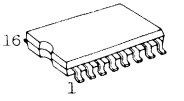
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=58MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS112



DIP16(3D16A-P)



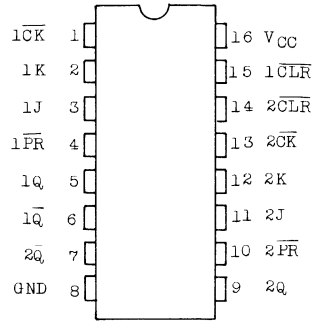
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

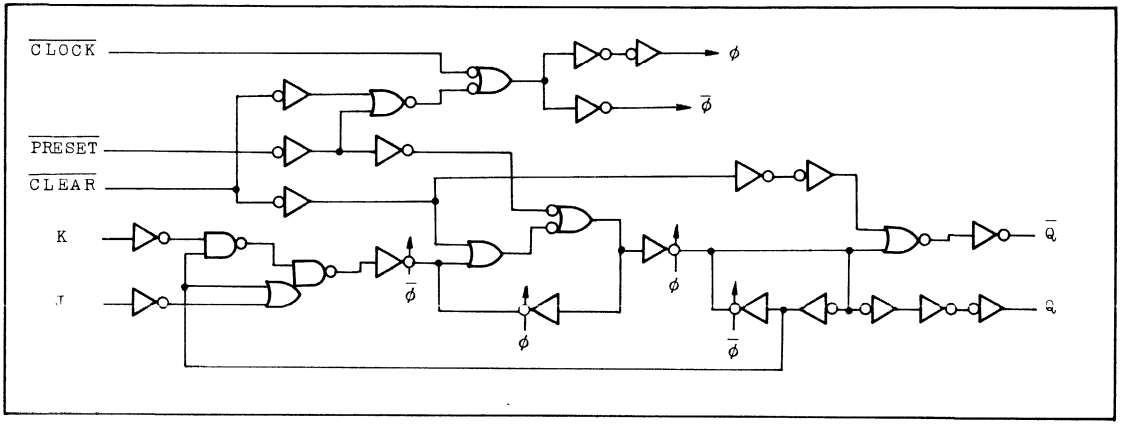
TC74HC112P/F

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

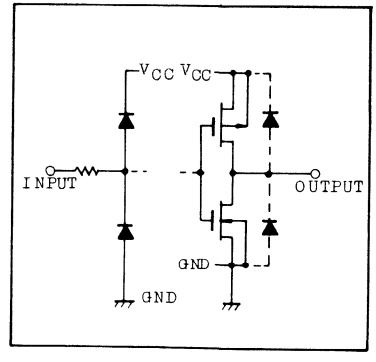
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC112P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	92	180	-	225	
	t_{pHL}		4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	53	-	24	-	
			6.0	35	62	-	28	-	

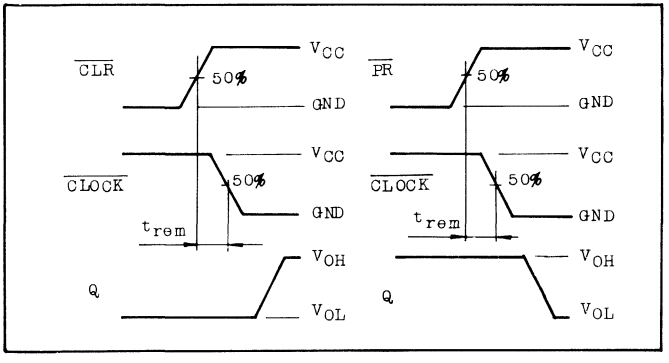
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	40	100	-	120	
			4.5	-	10	20	-	24	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	54	-	-	-	

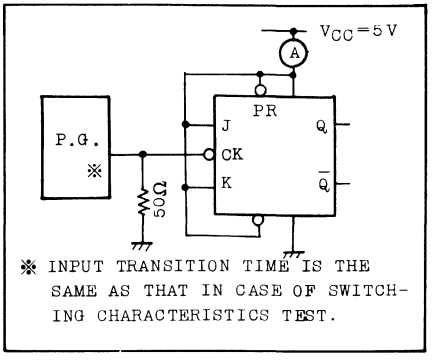
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



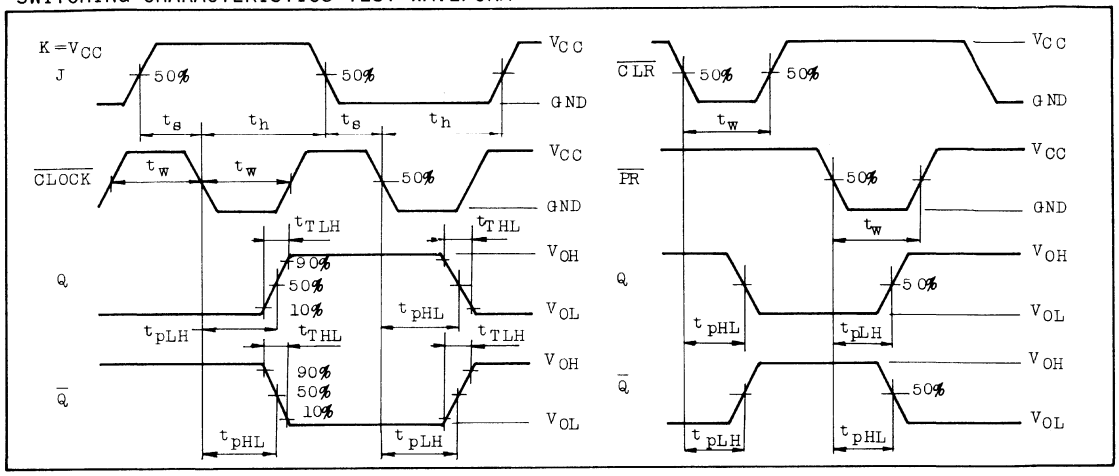
I_{CC}(opr.) TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC112P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC113P/F

TC74HC113P/F DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC113 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

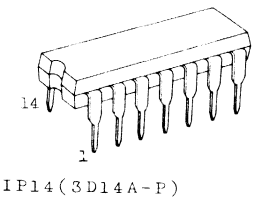
In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The preset function is accomplished independently of the clock condition when the preset input ($\overline{PR}$) is taken low.

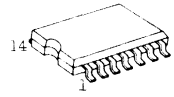
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=63MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS113



DIP14(3D14A-P)



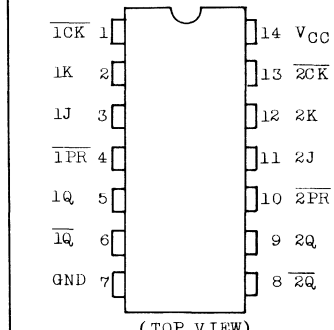
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

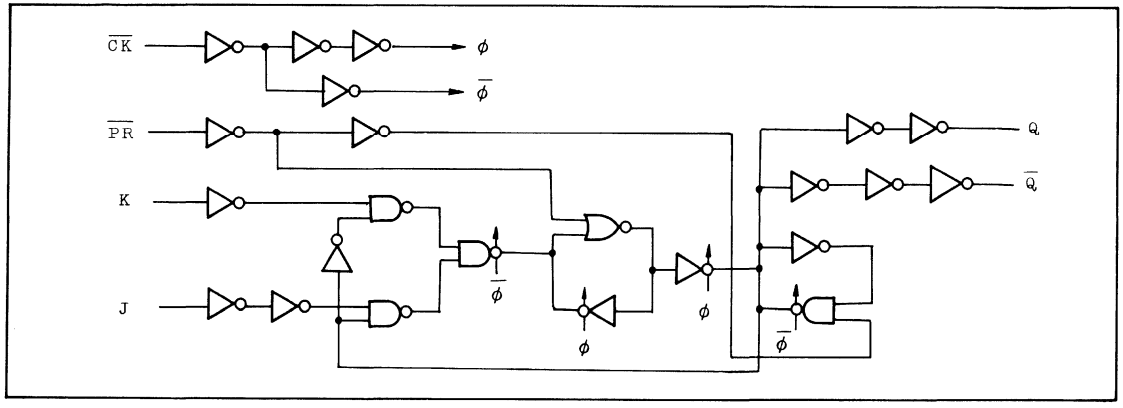
TC74HC113P/F

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	Preset
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	-
H	H	L	↓	H	L	-
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X:DON'T CARE

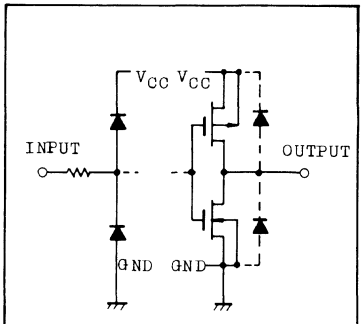
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	68	135	-	170	
	t_{pHL}		4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	80	160	-	200	
	t_{pHL}		4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	-	5	-	MHz
			4.5	32	58	-	27	-	
			6.0	38	68	-	32	-	

TC74HC113P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

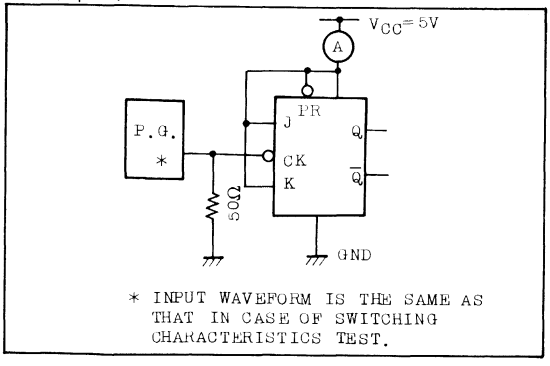
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	25	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{PR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	38	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

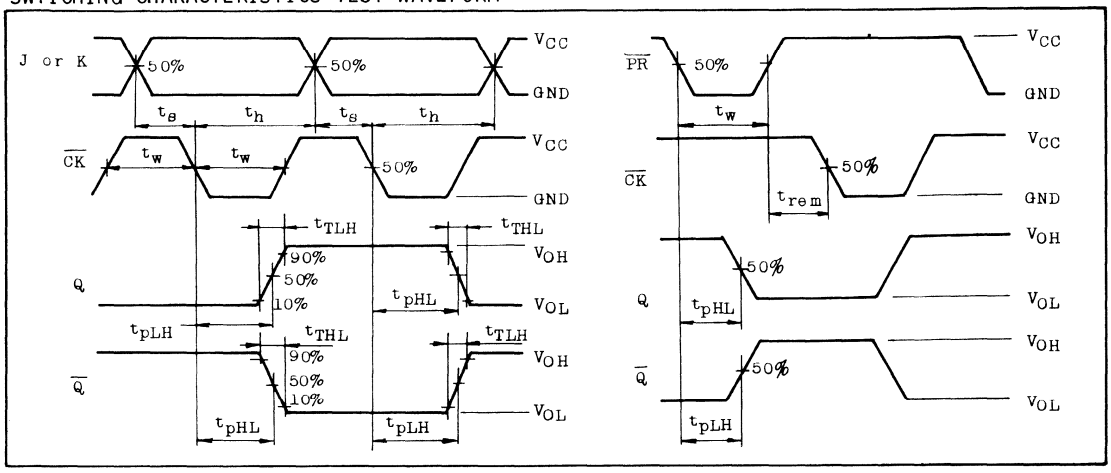
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWTICHING CHARACTERISTICS TEST WAVEFORM



TC74HC123P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC123P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

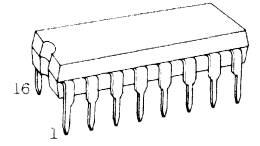
The TC74HC123 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CL}$ INPUT (Positive-edge input). After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5KΩ to 1MΩ
..... $V_{CC}\geqq$3.0V from 1KΩ to 1MΩ

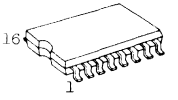
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=28ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range .... $t_{W(OUT)}$=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



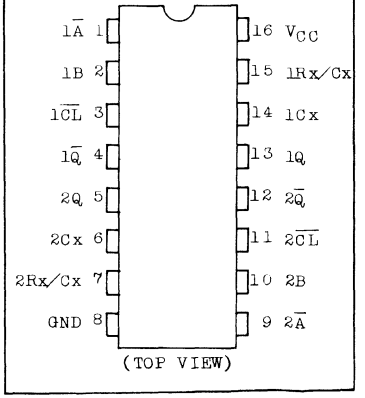
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



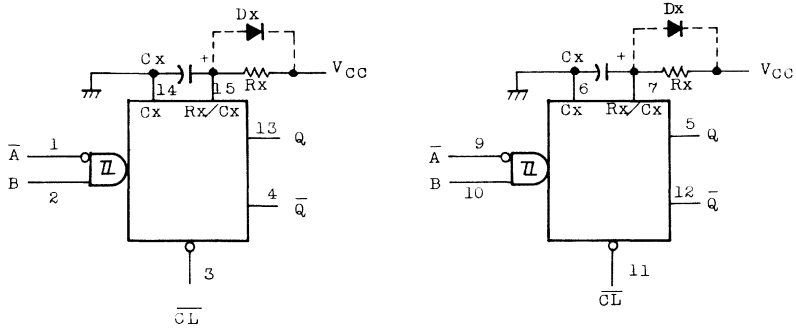
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎎	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⎍	⎎	OUTPUT ENABLE
L	H	↑	⎍	⎎	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

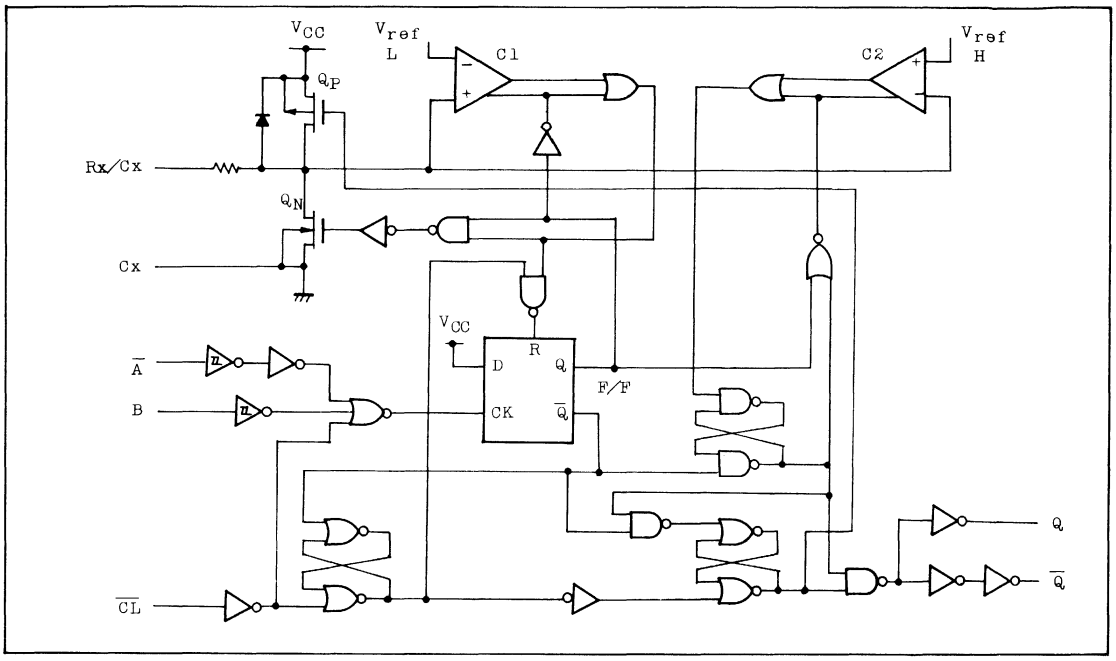
$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

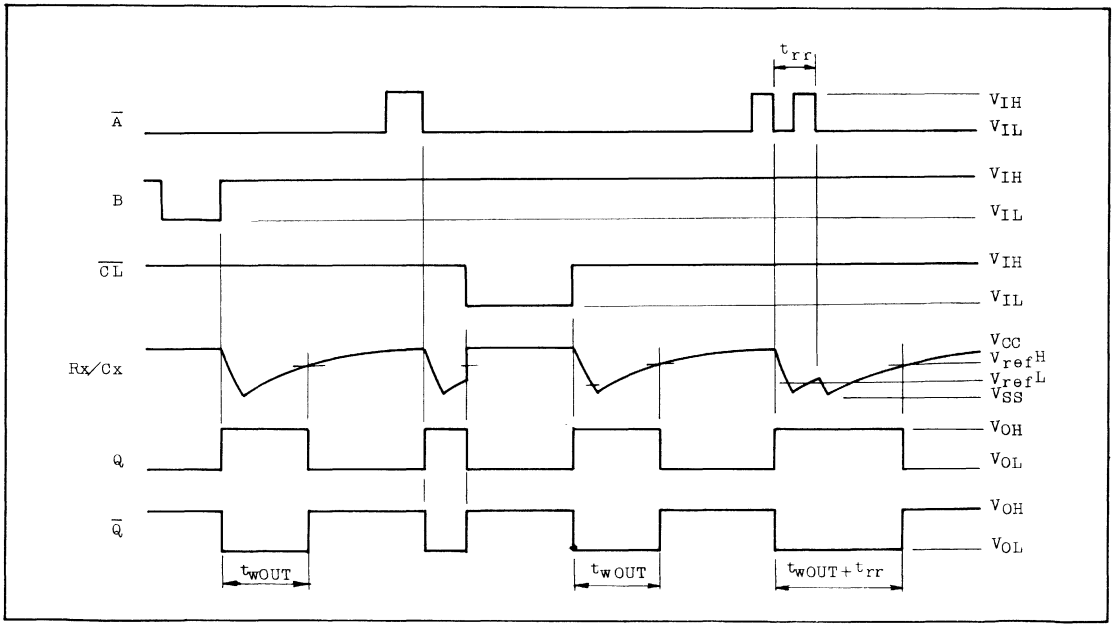
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

TC74HC123P/F

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\bar{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\bar{A}$ INPUT has rising up signal. Under the condition $\bar{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CL}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.46 \quad Cx \; Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

(4) Reset operation

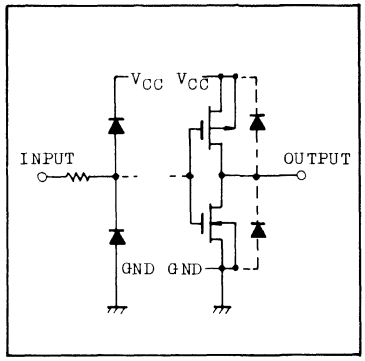
$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC123P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=VCC or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per Circuit

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time ($\bar{A}$, B - Q, $\bar{Q}$)	t_{PLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{PHL}		6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\bar{Q}$)	t_{pLH}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
	t_{pHL}		6.0	-	29	45	-	55	
Propagation Delay Time ($\overline{CLR}$ - Q, $\bar{Q}$)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Minimum Pulse Width (TRIGGER)	$t_{w(H)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
	$t_{w(L)}$		6.0	-	9	17	-	21	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error Between Circuits In Same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	ns
			6.0	-	63	-	-	-	
		Cx=0.01μF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	t_{wOUT} (MIN.)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	t_{wOUT}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1μF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	113	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

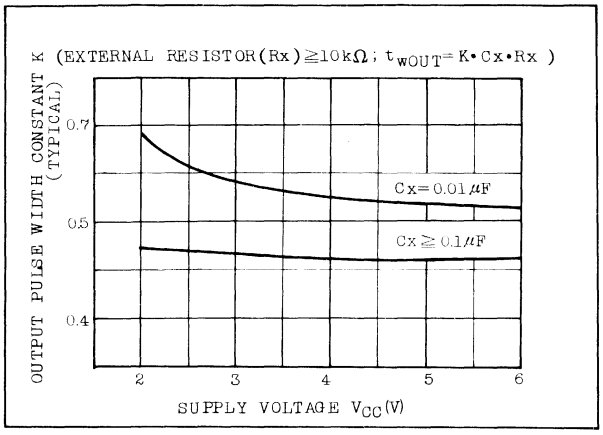
$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current)

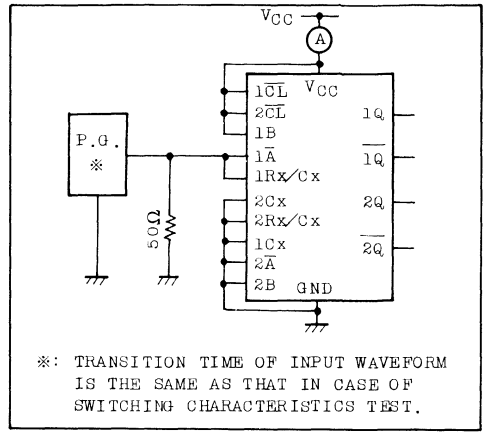
(Duty: %)

TC74HC123P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

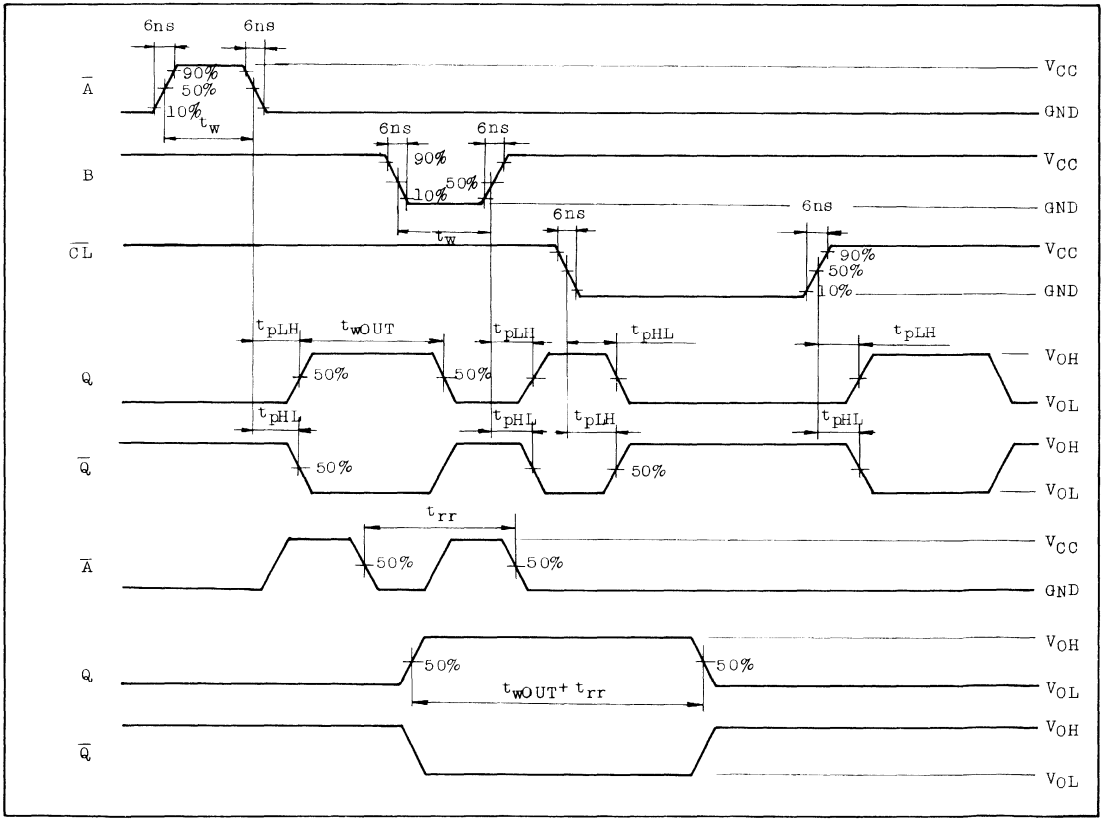


$I_{CC(opr.)}$ TEST WAVEFORM

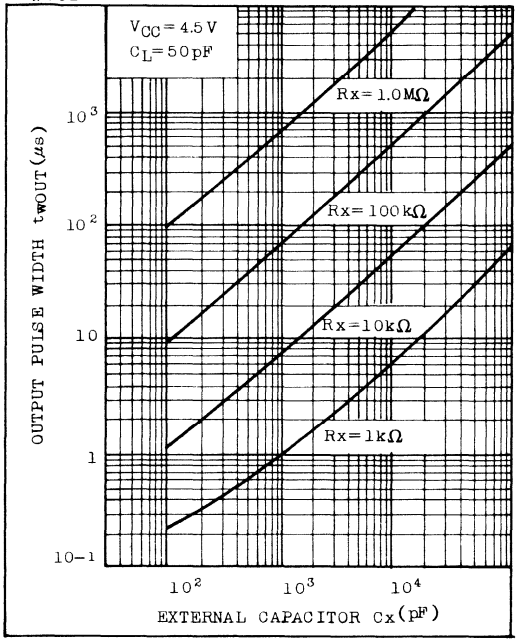


※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

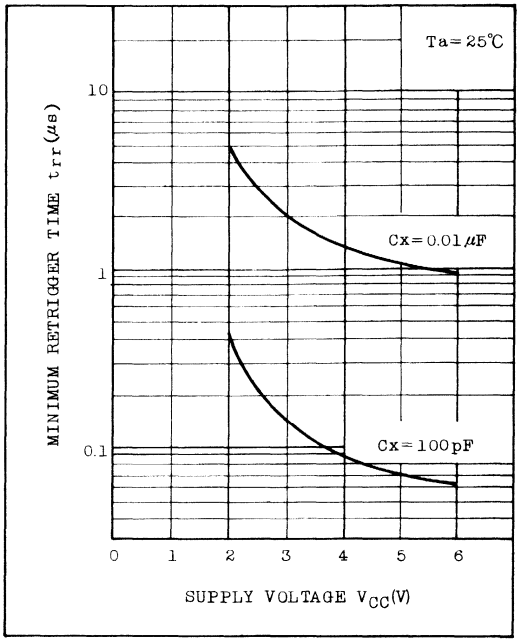
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



TC74HC125P/F
TC74HC126P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

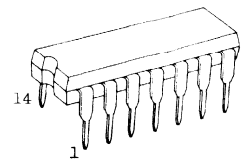
TC74HC125P/F QUAD BUS BUFFER
TC74HC126P QUAD BUS BUFFER

The TC74HC125 and the TC74HC126 are high speed CMOS QUAD BUS BUFFER fabricated with silicon gate C^2MOS technology.

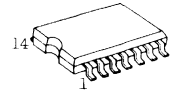
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC125 require the 3-STATE control input $\overline{G}$ to be taken high to put the output into the high impedance condition, whereas the TC74HC126 requires the control input to be taken low to put the output into high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14(3D14A-P)



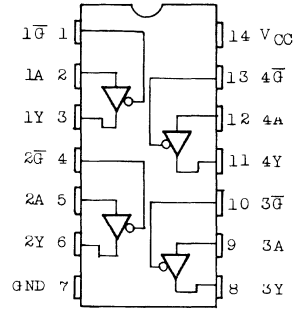
MFP14(F14GB-P)

FEATURES:

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS125/126

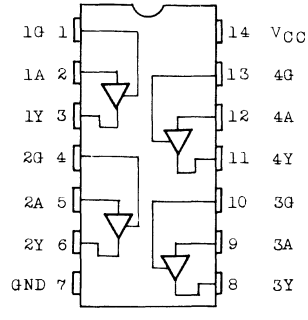
PIN ASSIGNMENT

TC74HC125



(TOP VIEW)

TC74HC126



(TOP VIEW)

TRUTH TABLE

TC74HC125

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC126

INPUTS		OUTPUT
G	A	Y
L	X	Z
H	L	L
H	H	H

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC125P/F
TC74HC126P/F

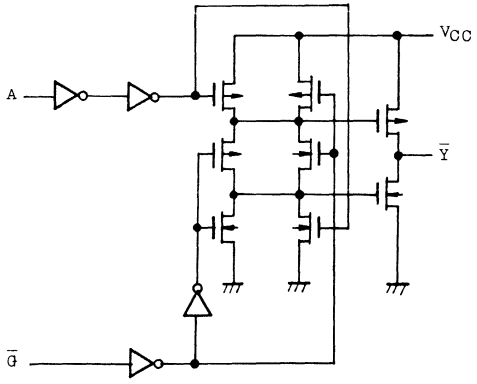
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

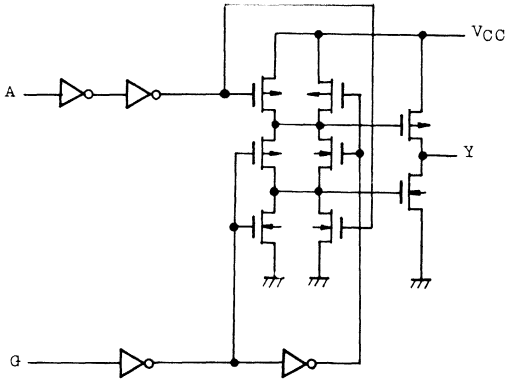
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

CIRCUIT DIAGRAM (Per circuit)

TC74HC125



TC74HC126

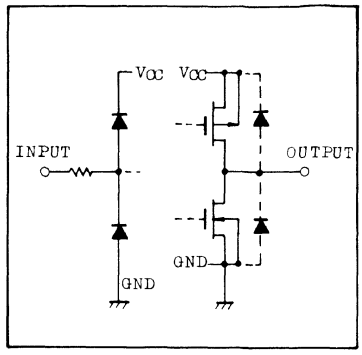


TC74HC125P/F
TC74HC126P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

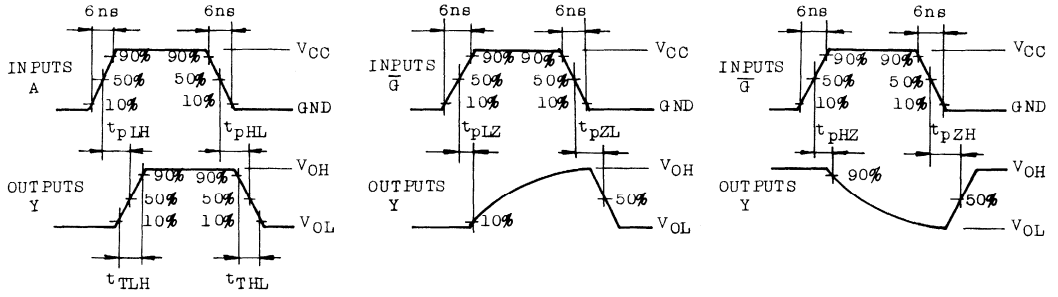
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH}		2.0	-	52	100	-	125	
	t_{pHL}		4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
3-State Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	44	90	-	115	
	t_{pZH}		4.5	-	11	18	-	23	
			6.0	-	19	15	-	20	
3-State Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	68	120	-	150	
	t_{pHZ}		4.5	-	17	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

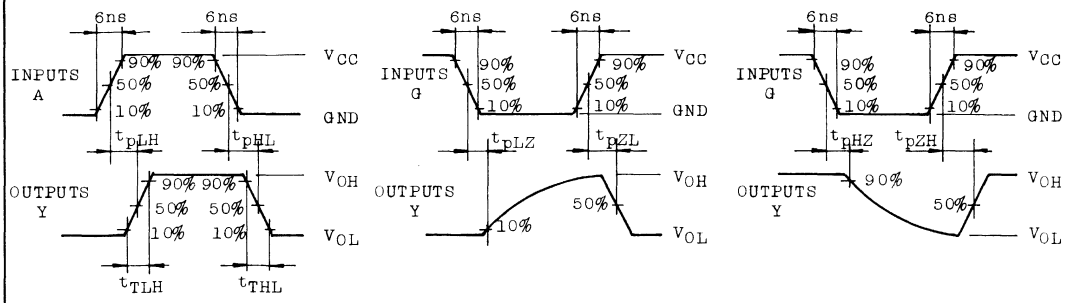
TC74HC125



TC74HC125P/F
TC74HC126P/F

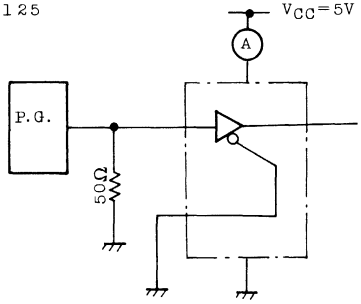
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

TC74HC126

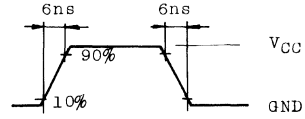


I_{CC}(Opr.) TEST CIRCUIT

TC74HC125

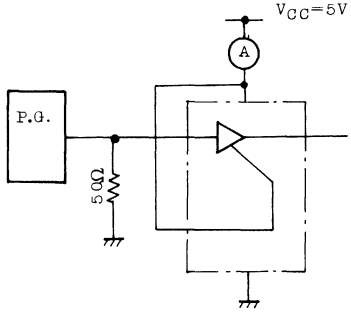


INPUT WAVEFORM

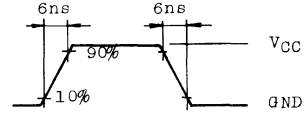


THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

TC74HC126



INPUT WAVEFORM



THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

TC74HC131P/F

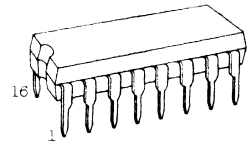
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC131P/F 3-TO-8 LINE DECODER/LATCH

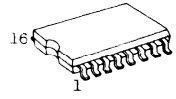
The TC74HC131 is a high speed CMOS 3-TO-8 LINE DECODER with input register fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input register with a common CLOCK input and 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into input register on the positive going transition of the clock pulse, determine which one of outputs will go low.
Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=24ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS131



DIP16(3D16A-P)



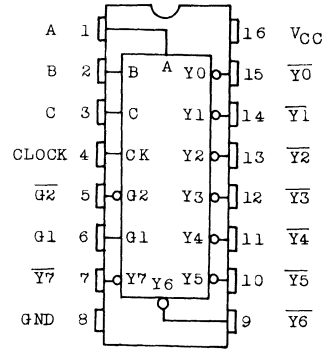
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

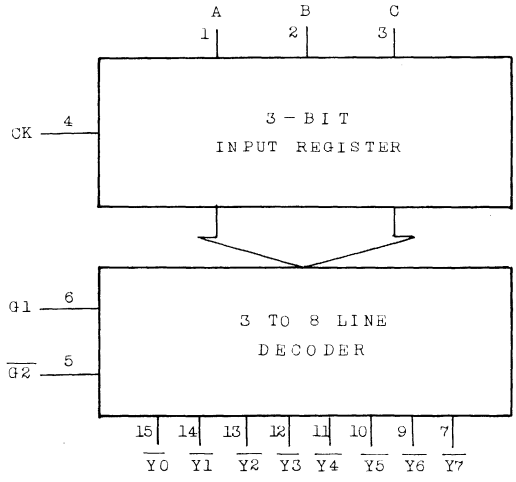
TC74HC131P/F

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE		CLOCK	SELECT										
G1	$\overline{G2}$		C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	↓	L	L	L	L	H	H	H	H	H	H	H
H	L	↓	L	L	H	H	L	H	H	H	H	H	H
H	L	↓	L	H	L	H	H	L	H	H	H	H	H
H	L	↓	L	H	H	H	H	H	L	H	H	H	H
H	L	↓	H	L	L	H	H	H	H	L	H	H	H
H	L	↓	H	L	H	H	H	H	H	H	L	H	H
H	L	↓	H	H	L	H	H	H	H	H	H	L	H
H	L	↓	H	H	H	H	H	H	H	H	H	H	L
H	L	↑	X	X	X	Outputs corresponding to stored address ····· L All others ····· H							

X : Don't care

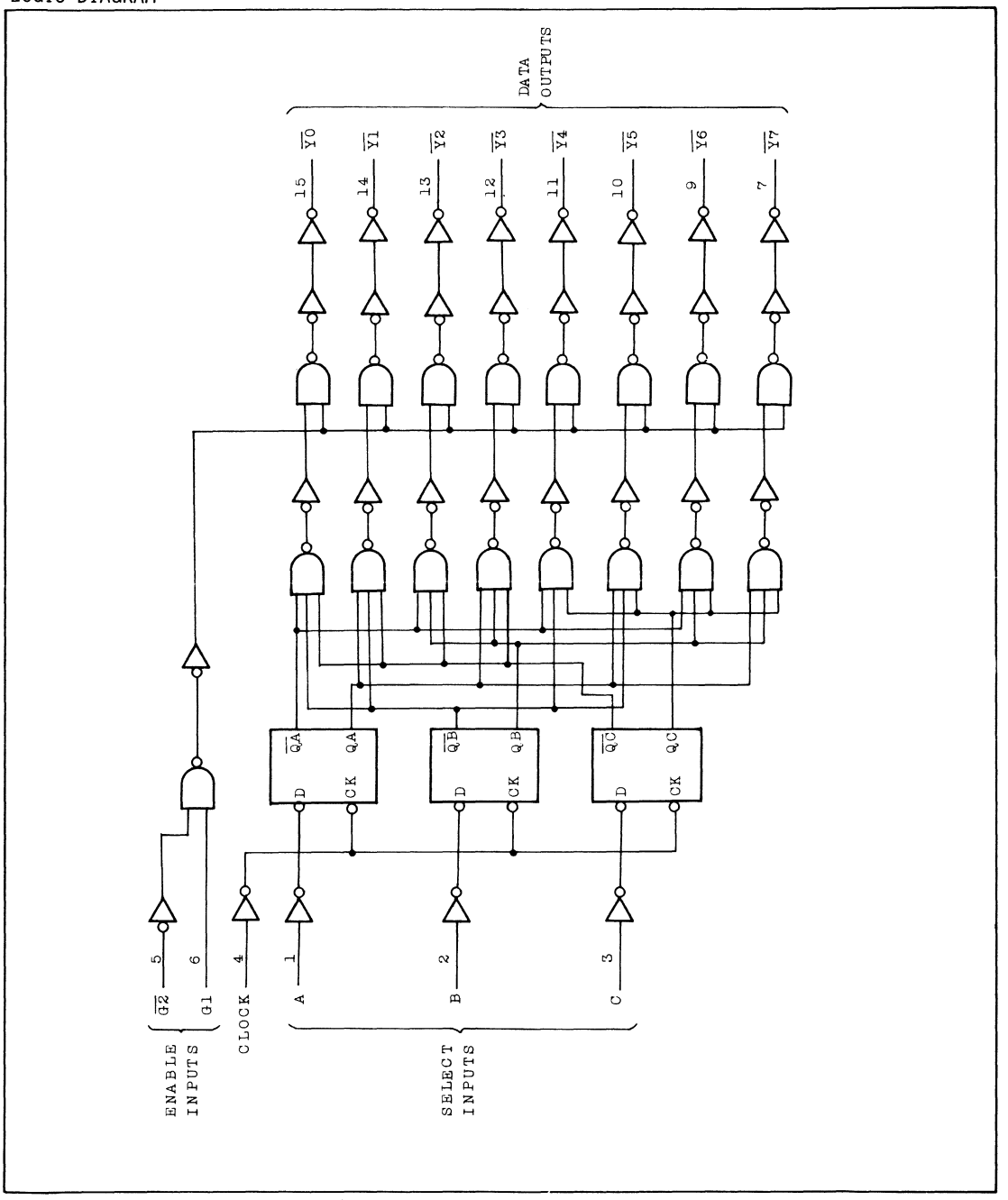
BLOCK DIAGRAM



V_{CC} = 16
GND = 8

TC74HC131P/F

LOGIC DIAGRAM

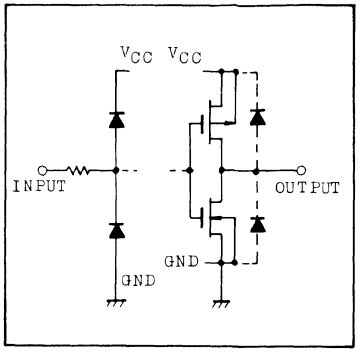


TC74HC131P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{Yn}$)	t_{pLH} t_{pHL}		2.0	-	112	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (G1, $\overline{G2}$ - $\overline{Yn}$)	t_{pLH} t_{pHL}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
			6.0	-	16	24	-	30	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	12	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	89	-	-	-	

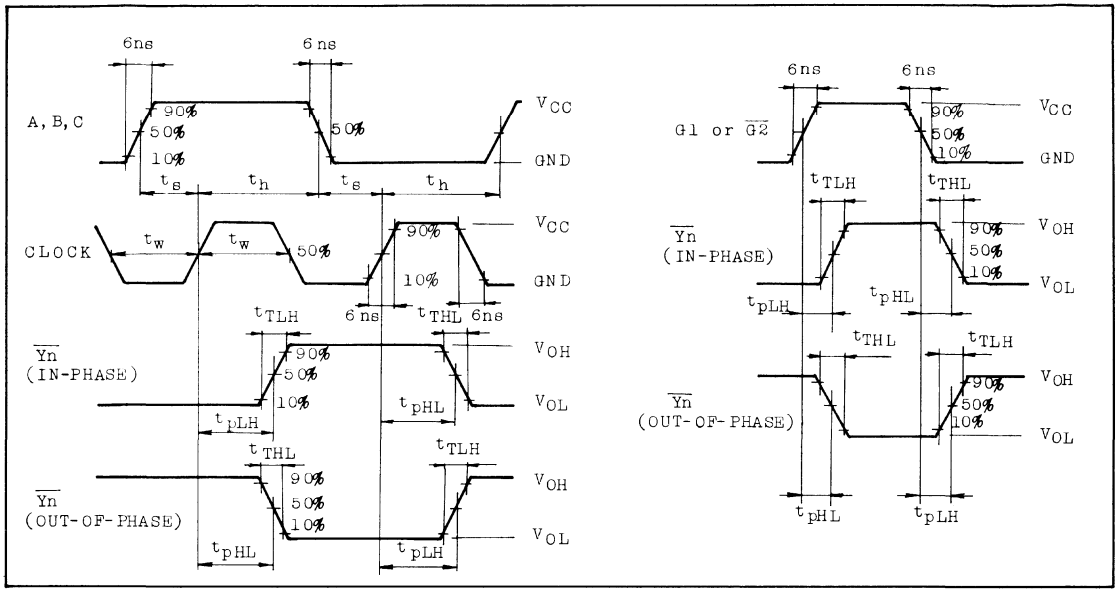
Note 1 C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

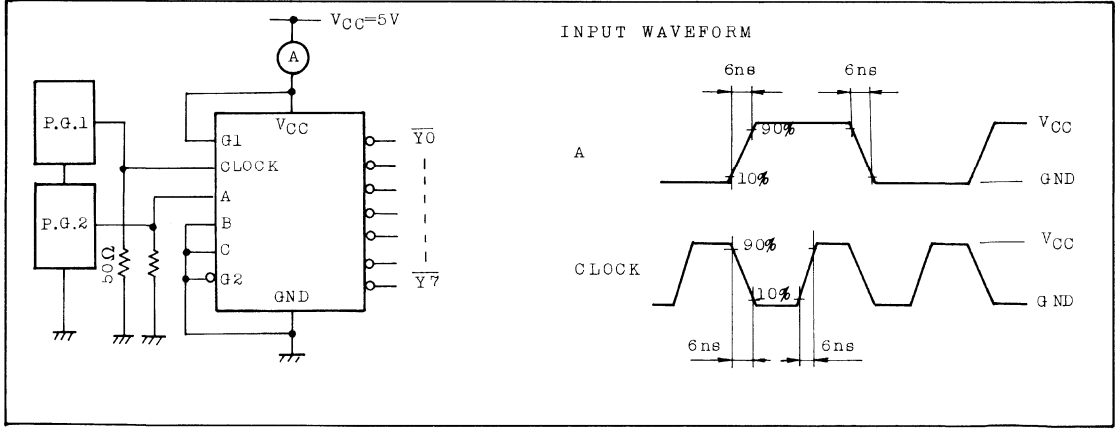
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC131P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC132P/F

TC74HC132P/F QUAD 2-INPUT SCHMITT NAND GATE

The TC74HC132 is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fablicated with silicon gate C²MOS technology.

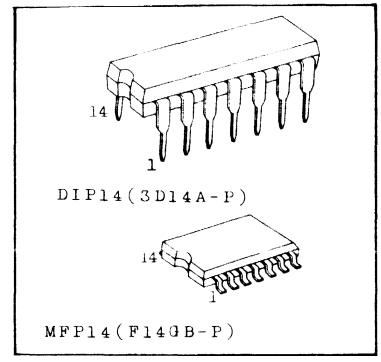
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin connection and function are identical to those of the TC74HC00, and provided hysteresis characteristics (around 20% V_{CC}) of all input enables transforming slowly changing input signals into sharply defined jitter-free output signals.

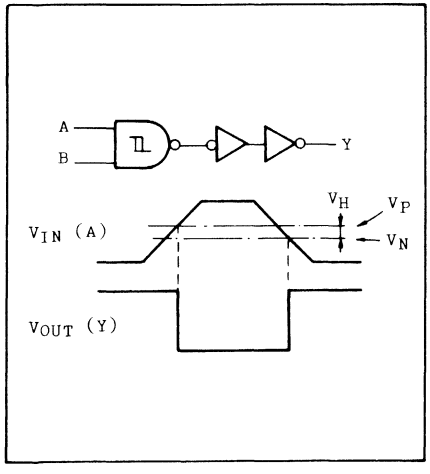
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

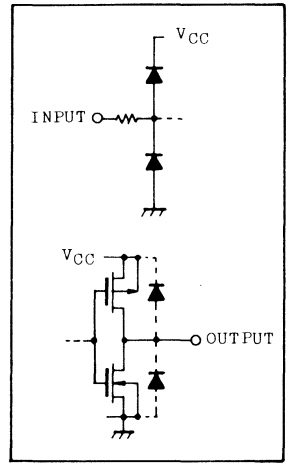
- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_H=0.9V at V_{CC}=5V
- Output Drive Capability.....10 LSTTL Loads
- Symmertical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS132



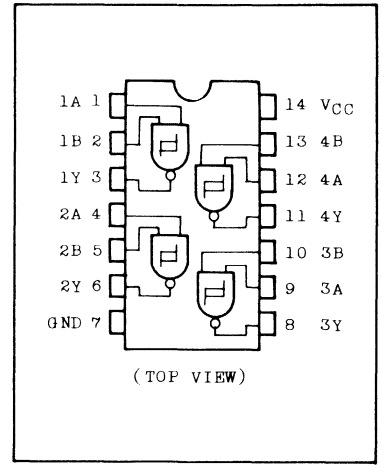
LOGIC DIAGRAM and INPUT OUTPUT WAVEFORM



INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGNMENT



(TOP VIEW)

TC74HC132P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Threshold Voltage	V_P		2.0	0.8	1.25	1.5	0.8	1.5	V
			4.5	2.25	2.7	3.15	2.25	3.15	
			6.0	3.0	3.6	4.2	3.0	4.2	
Low-Level Threshold Voltage	V_N		2.0	0.4	0.75	1.0	0.4	1.0	V
			4.5	1.35	1.9	2.25	1.35	2.25	
			6.0	1.8	2.6	3.0	1.8	3.0	
Hysteresis Voltage	V_H		2.0	0.20	0.5	1.0	0.20	1.0	V
			4.5	0.4	0.8	1.4	0.4	1.4	
			6.0	0.6	1.0	1.7	0.6	1.7	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

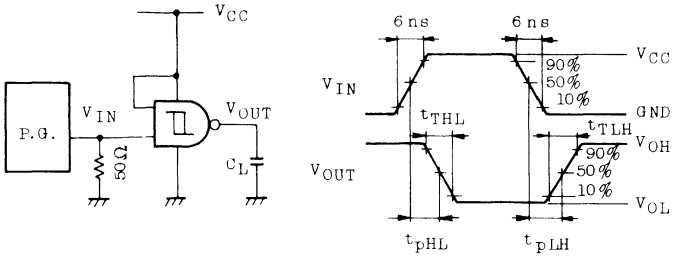
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	ns
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	35	-	-	-	

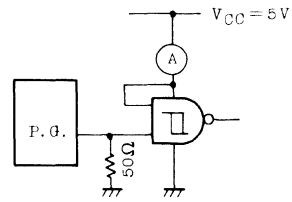
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

TC74HC132P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC133P/F

TC74HC133P/F 13-INPUT NAND GATE

The TC74HC133 is a high speed CMOS 13-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

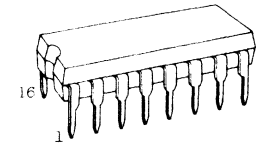
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 7 stages including buffer output, which enables high noise immunity and stable output.

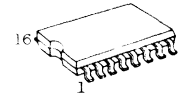
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS133

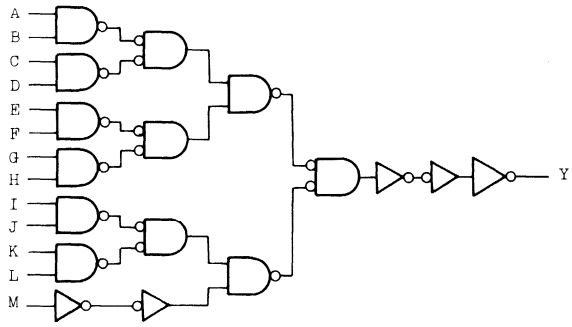


DIP16(3D16A-P)

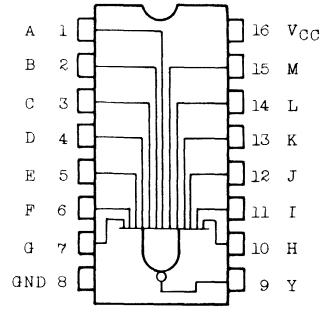


MFP16(F16GC-P)

LOGIC DIAGRAM



PIN ASSIGNMENT



(Top View)

TC74HC133P/F

ABSOLUTE MAXIMUM RATINGS

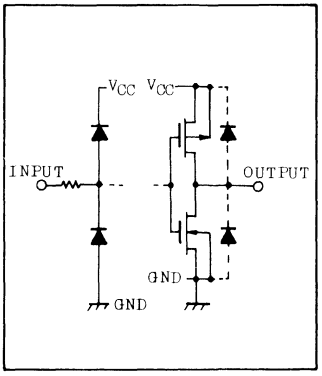
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

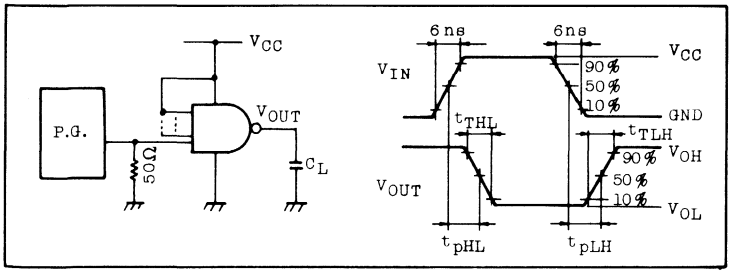
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	80	150	-	190	ns
			4.5	-	20	30	-	38	
			6.0	-	17	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

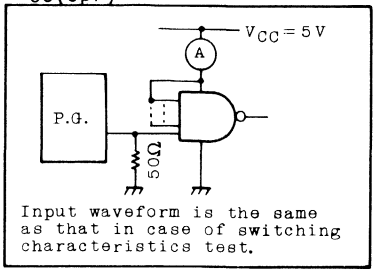
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC137P/F

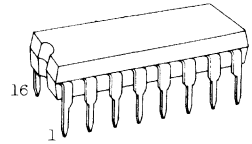
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC137P/F 3-TO-8 LINE DECODER/LATCH

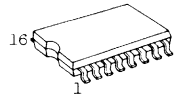
The TC74HC137 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go low. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS137.



DIP16(3D16A-P)



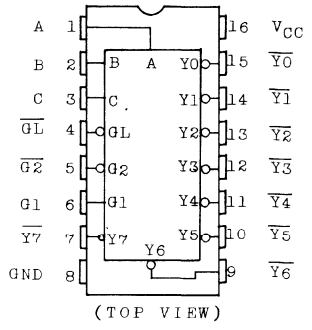
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



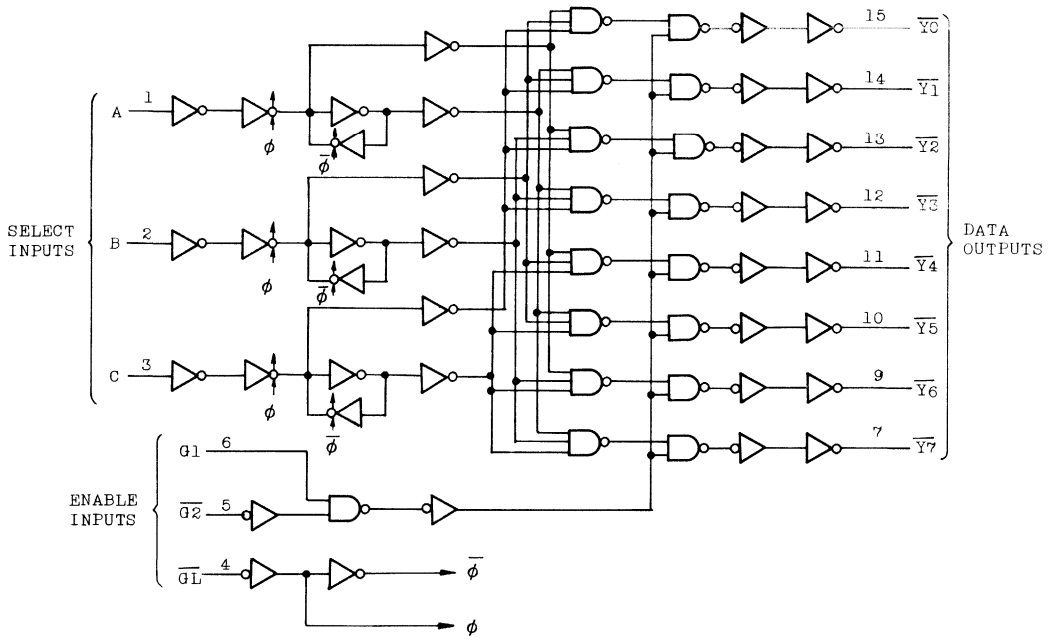
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	Output corresponding to stored address, L; all others, H							

X: Don't care

LOGIC DIAGRAM

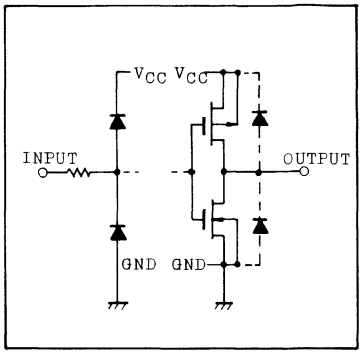


TC74HC137P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

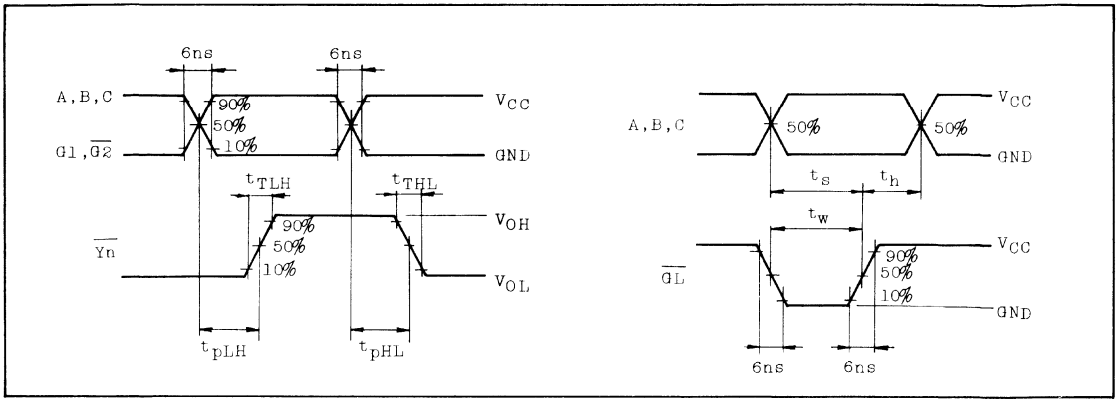
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH}		2.0	-	72	145	-	180	
	t_{pHL}		4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	t_{pLH}		2.0	-	80	155	-	195	
	t_{pHL}		4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH}		2.0	-	112	220	-	275	
	t_{pHL}		4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH}		2.0	-	100	195	-	245	
	t_{pHL}		4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C, - $\overline{GL}$)	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time (A, B, C, - $\overline{GL}$)	t_h		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	65	-	-	-	

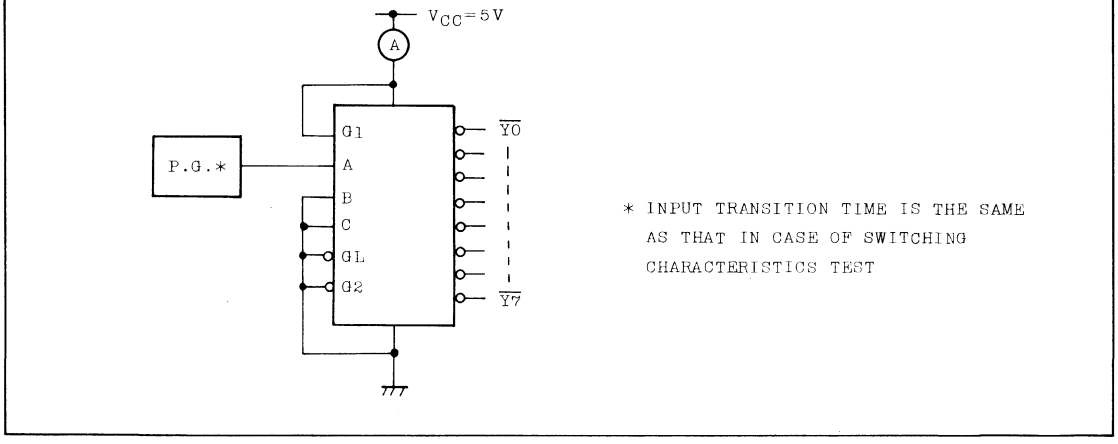
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TC74HC137P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

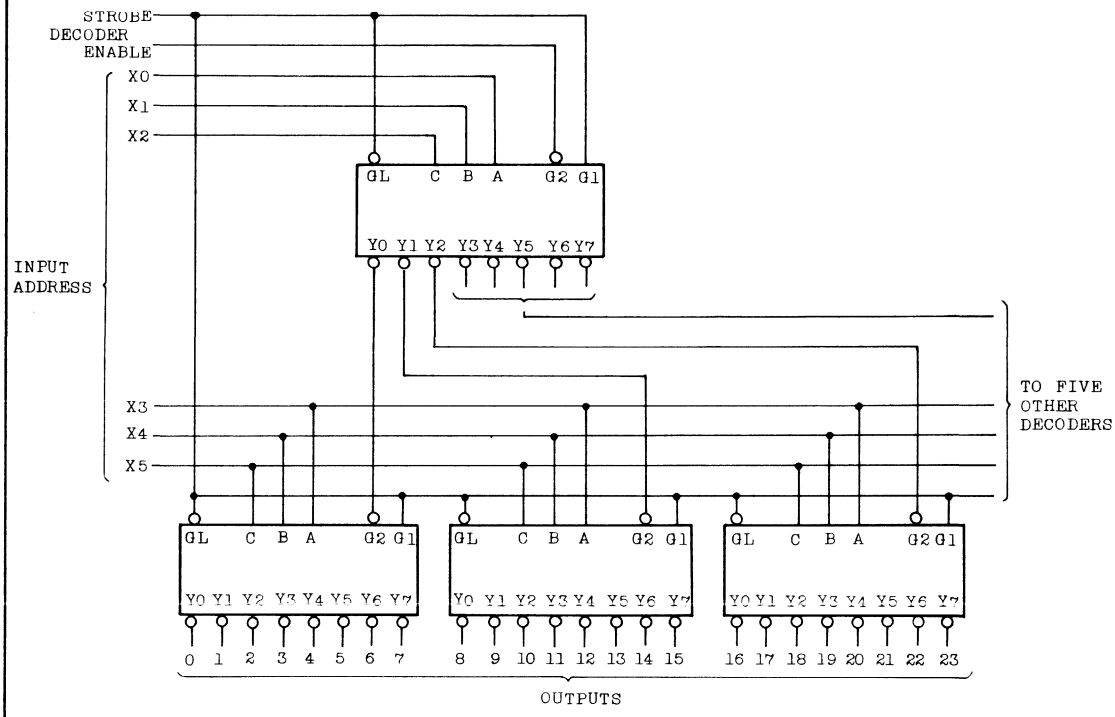


$I_{CC(Opr.)}$ TEST CIRCUIT



* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HCT137P/F

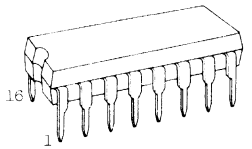
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT137P/F 3-TO-8 LINE DECODER/LATCH

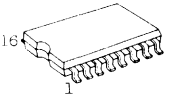
The TC74HCT137 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C²MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go low. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS137



DIP16(3D16A-P)



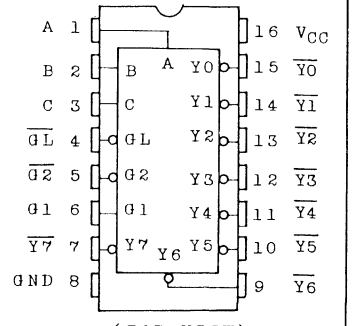
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

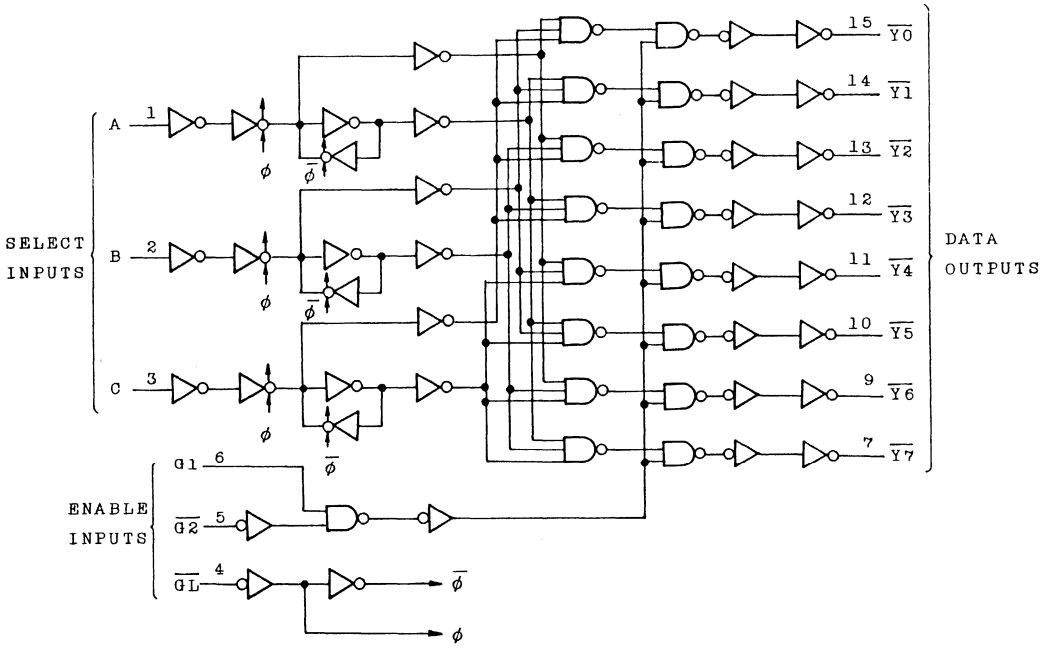
TC74HCT137P/F

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	Output corresponding to stored address, L; all others, H							

X : DON'T CARE

LOGIC DIAGRAM

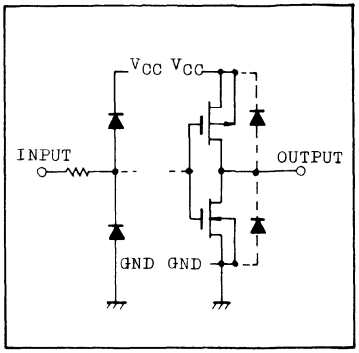


TC74HCT137P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

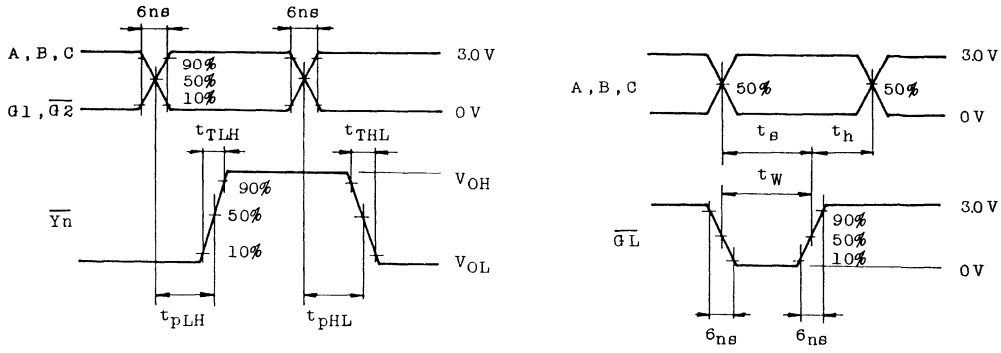
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	25	39	-	49	
Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	24	37	-	46	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	34	52	-	65	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	29	45	-	56	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		4.5	-	8	15	-	19	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		4.5	-	2	10	-	13	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		4.5	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	68	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

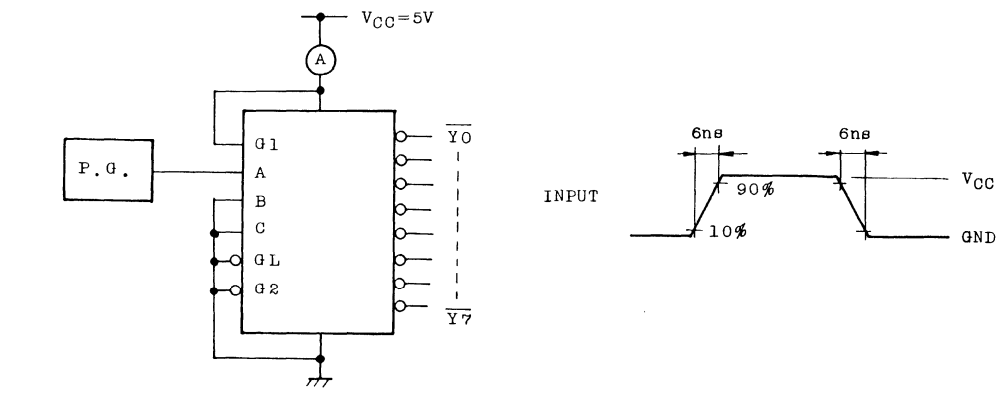
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HCT137P/F

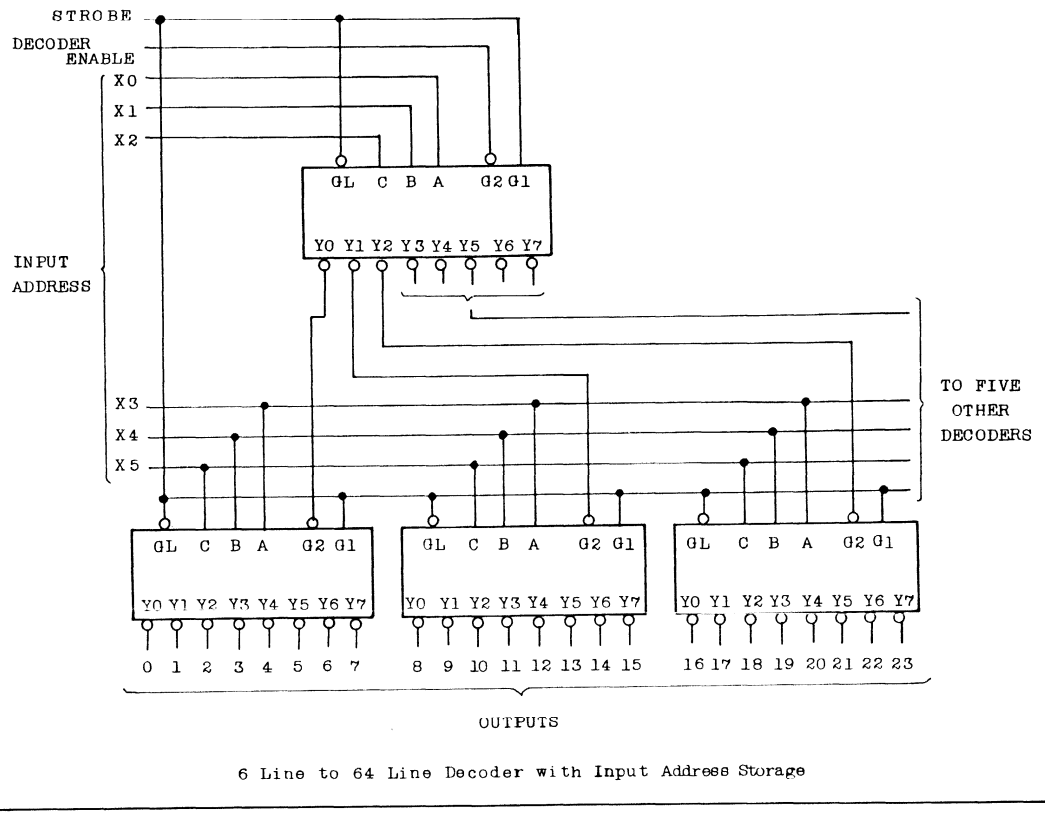
SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HC138P/F

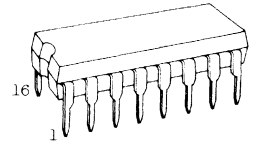
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC138P/F 3-TO-8 LINE DECODER

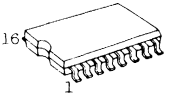
The TC74HC138 is a high speed CMOS DECODER (3-8 LINE) fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
If the device is enabled, 3 binary select inputs (A,B and C) determine which one of outputs will go low.
Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=17ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS138.

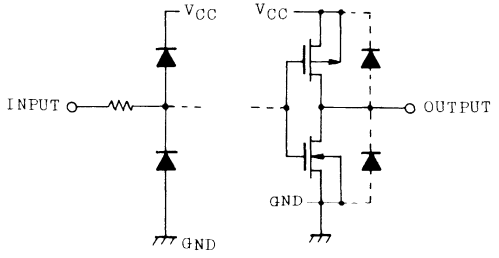


DIP16(3D16A-P)

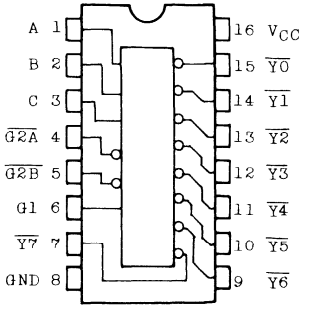


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT



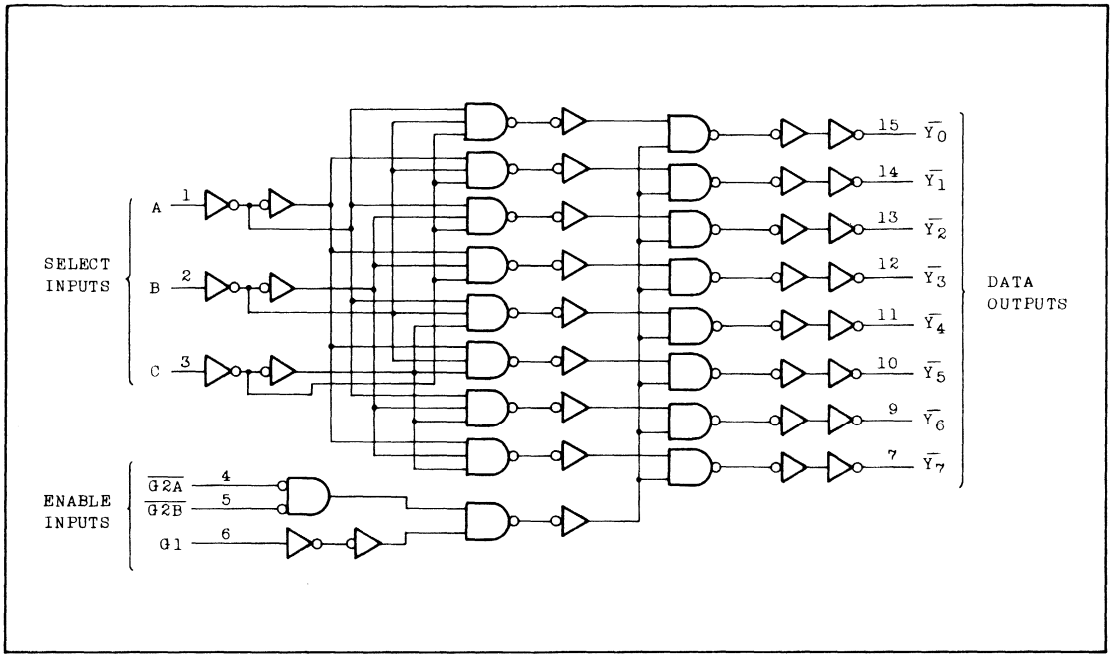
PIN ASSIGNMENT



(TOP VIEW)

TC74HC138P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}_0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}_1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}_2$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}_3$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}_4$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}_5$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}_6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}_7$

X : Don't Care

TC74HC138P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

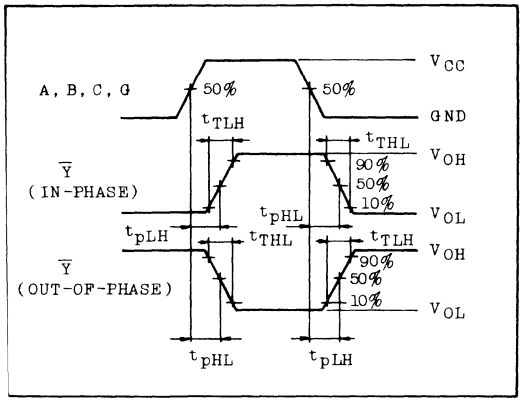
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A,B,C - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	ns
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (G, $\overline{G}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	57	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

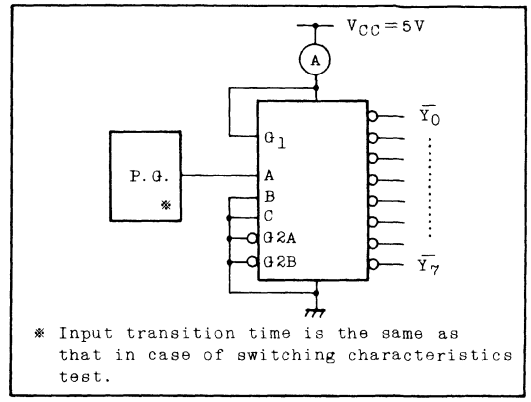
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

TC74HC138P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



※ Input transition time is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

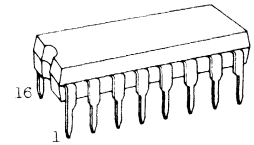
TC74HCT138P/F

TC74HCT138P/F 3-TO-8 LINE DECODER

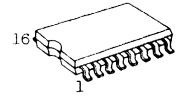
The TC74HCT138 is a high speed CMOS DECODER (3-8 LINE) fabricated with silicon gate C²MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go low.
Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discahrge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL Outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}| = I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS138

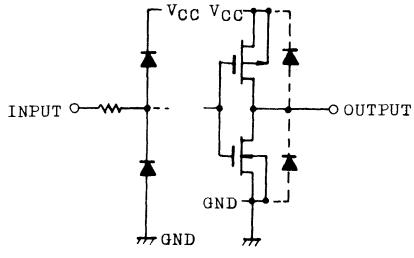


DIP16(3D16A-P)

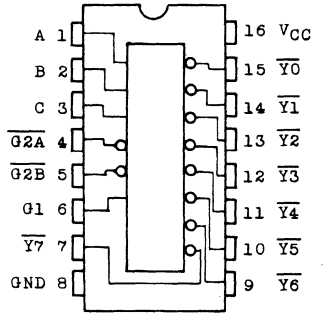


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT



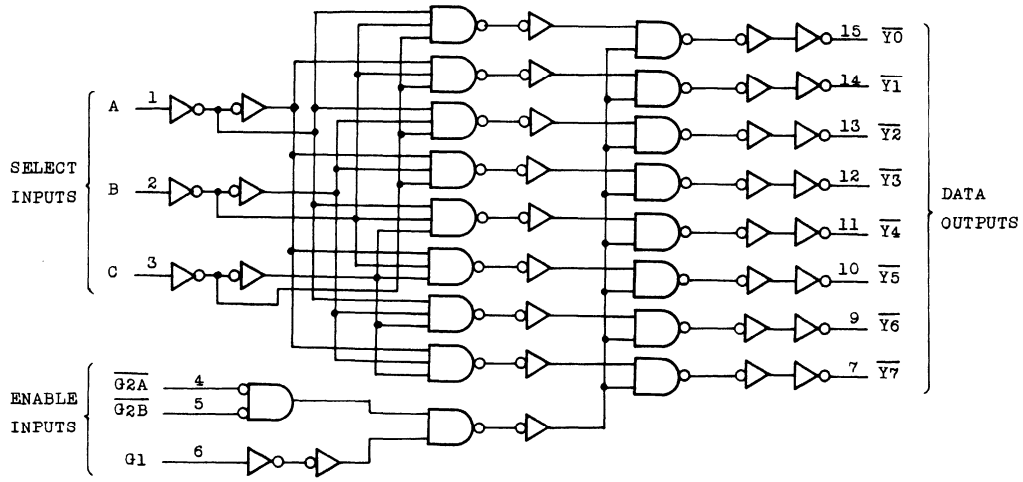
PIN ASSIGNMENT



(Top View)

TC74HCT138P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : DON'T CARE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ∫ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∫ 5.5	-	-	0.8	-	0.8	
High-Level Ouptut Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA

TC74HCT138P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	μA
	I_C	Per Input: V_{IN}=2.4V or 0.5 Other Input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

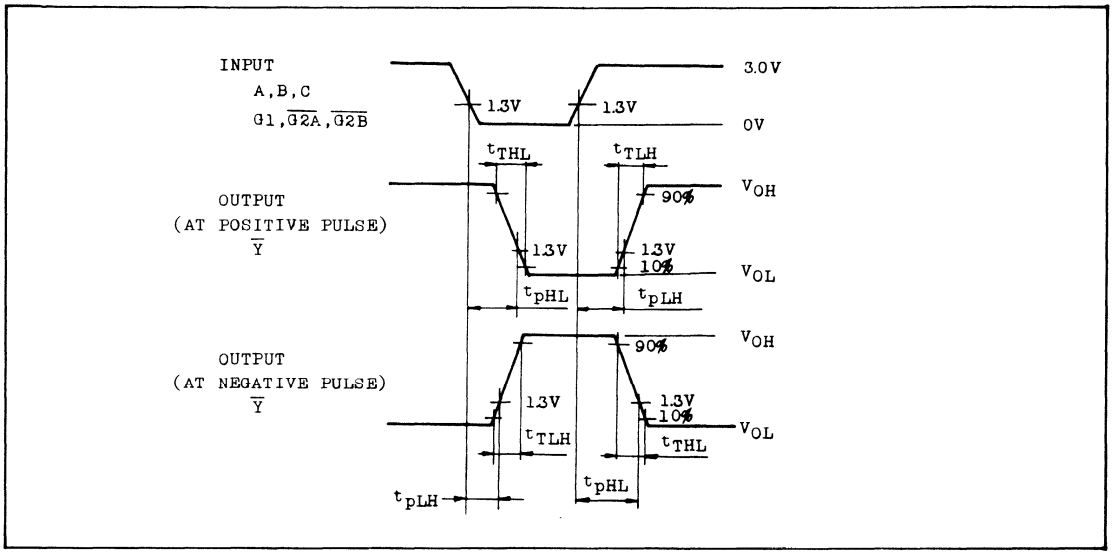
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	26	41	-	51	
Propagation Delay Time (G2 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	30	47	-	59	
Propagation Delay Time (A, B, C, - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	32	50	-	63	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	65	-	-	-	

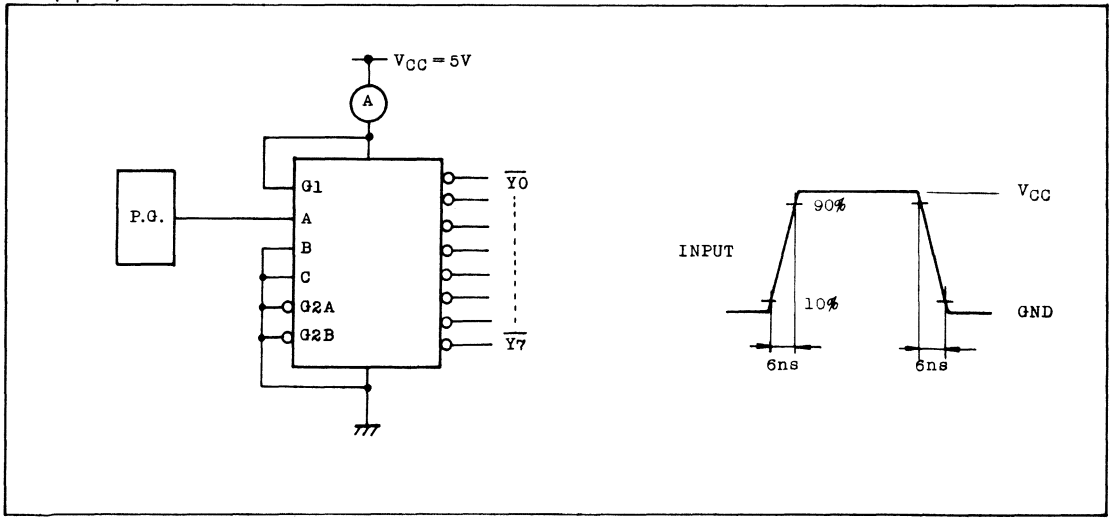
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



TC74HC139P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC139P/F DUAL 2-TO-4 LINE DECODER

The TC74HC139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology.

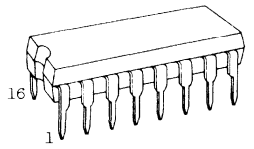
The active low enable input can be used for gating or can be used as a data input for demultiplexing applications.

While the enable input is held high, all four outputs are fixed in high logic level independent of the other inputs.

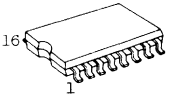
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS139

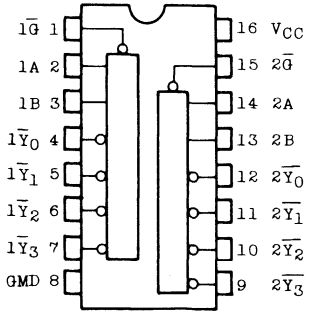


DIP16(3D16A-P)



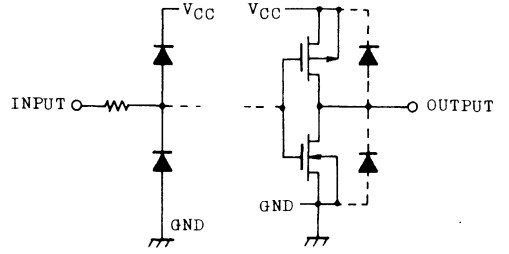
MFP16(F16GC-P)

PIN ASSIGNMENT



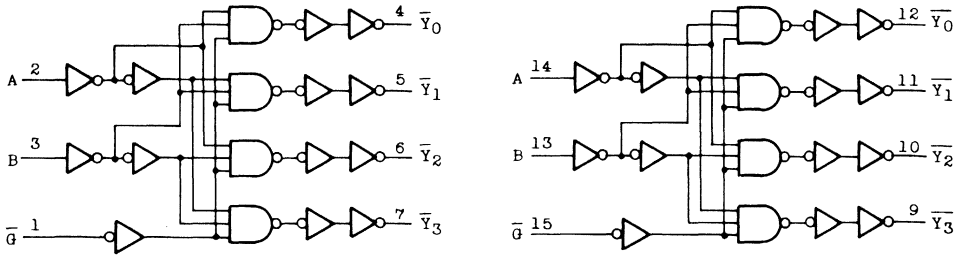
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC139P/F

BLOCK DIAGRAM



INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y}_0$
L	L	H	H	L	H	H	$\overline{Y}_1$
L	H	L	H	H	L	H	$\overline{Y}_2$
L	H	H	H	H	H	L	$\overline{Y}_3$

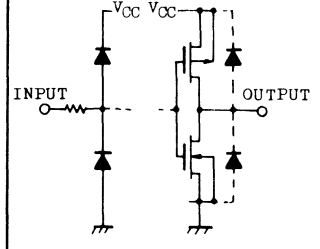
Note
X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT

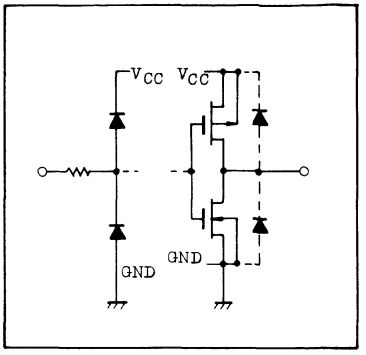


TC74HC139P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

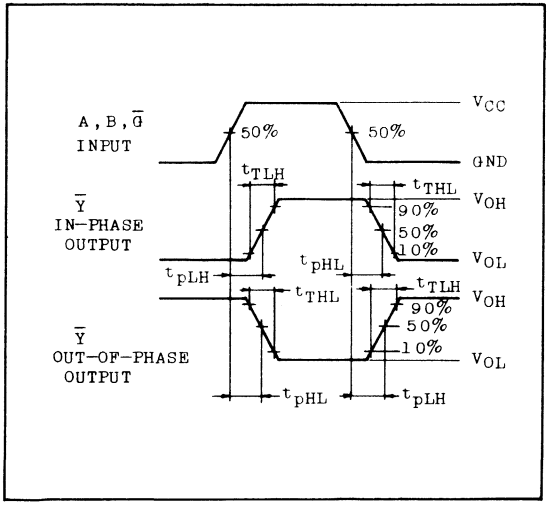
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Suppl Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

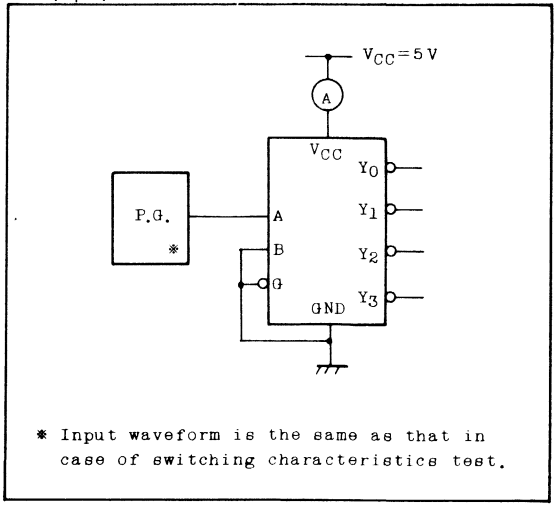
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75		95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time A,B-Y	t_{pLH} t_{pHL}		2.0	-	76	150		190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time $\overline{G}$ - Y	t_{pLH} t_{pHL}		2.0	-	68	135		170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	49	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Decoder)

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



* Input waveform is the same as that in case of switching characteristics test.

TC74HC147P/F

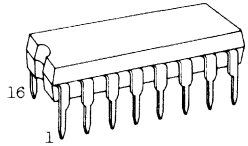
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC147P/F 10-TO-4 LINE PRIORITY ENCODER

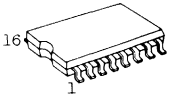
The TC74HC147 is a high speed CMOS 10-TO-4 LINE PRIORITY ENCODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS147



DIP16(3D16A-P)



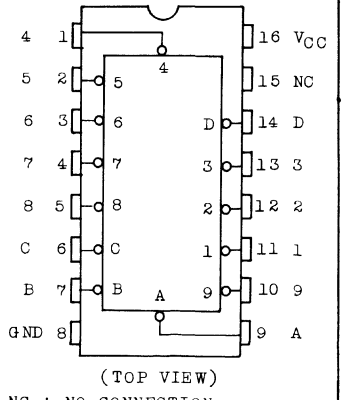
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

NC : NO CONNECTION

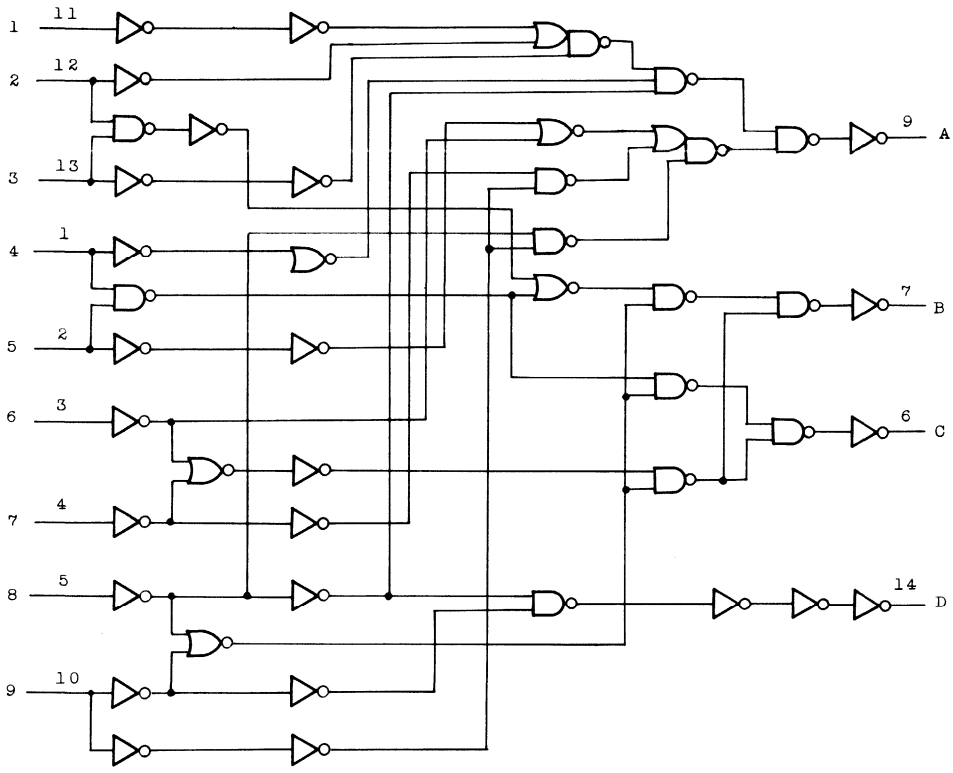
TC74HC147P/F

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

LOGIC DIAGRAM

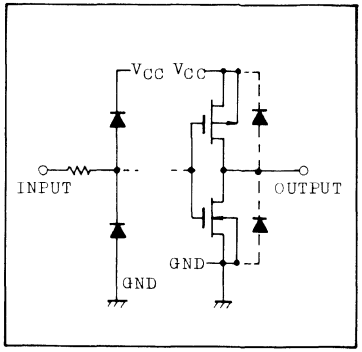


TC74HC147P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

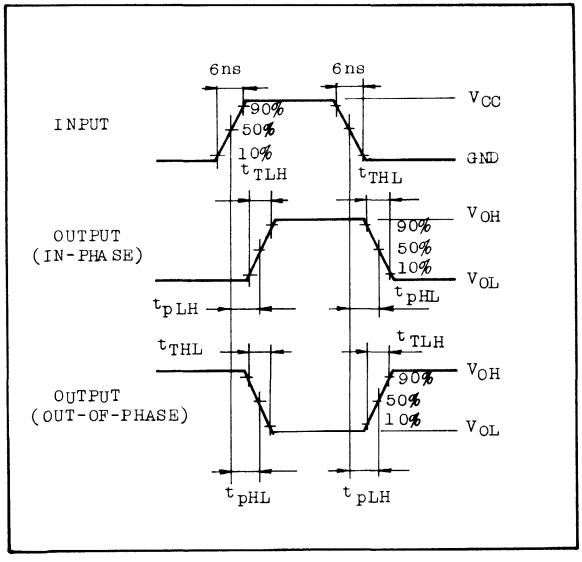
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	37	-	-	-	

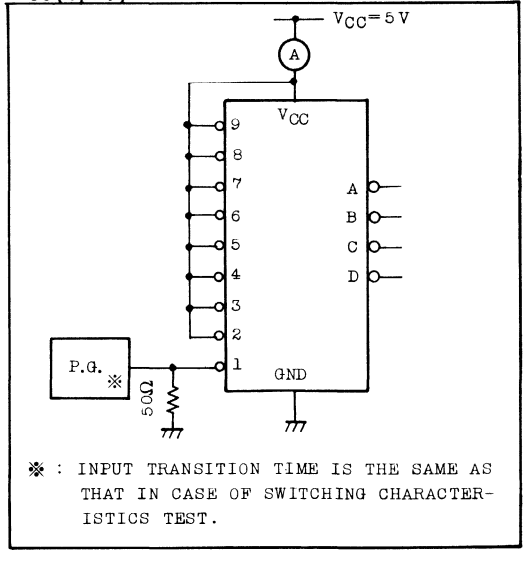
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST WAVEFORM



※ : INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC148P/F

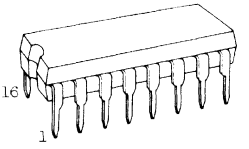
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC148P/F 8-TO-3 LINE PRIORITY ENCODER

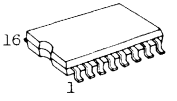
The TC74HC148 is a high speed CMOS 8-TO-3 LINE PRIORITY ENCODER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The encoder detects "L" level of the highest order among eight input signals and outputs the corresponding signal position in binary code. The inputs are eight input signals of 0 through 7 and input EI and when EI is set to "H" level, the encode operation is inhibited making all the outputs at "H" level. The encoded output appears on three signal lines A0 through A2 in binary. Outputs EO and GS are the outputs to indicate the operational mode of encoder and used when the number of bits is to be increased by cascade connection. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS148



DIP16(3D16A-P)



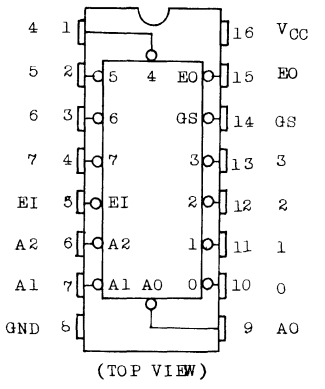
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



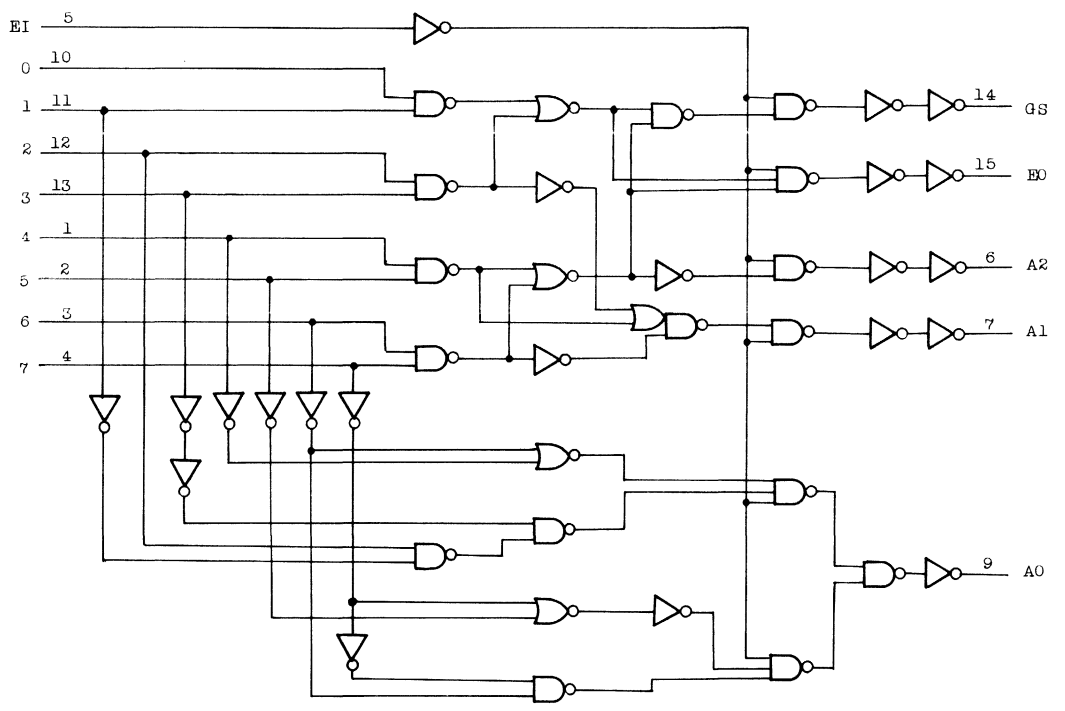
(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X : Don't Care

LOGIC DIAGRAM

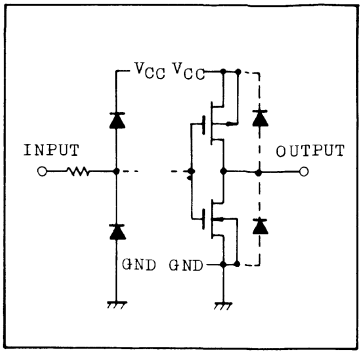


TC74HC148P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

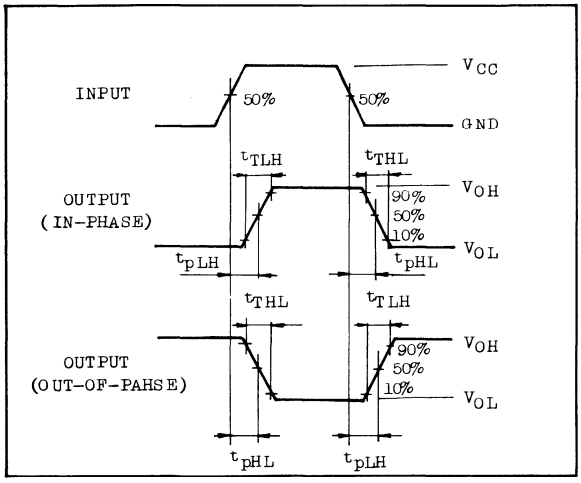
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (IN - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (IN - EO, GS)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (EI - EO)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (EI - GS)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Propagation Delay Time (EI - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10		10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	57	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

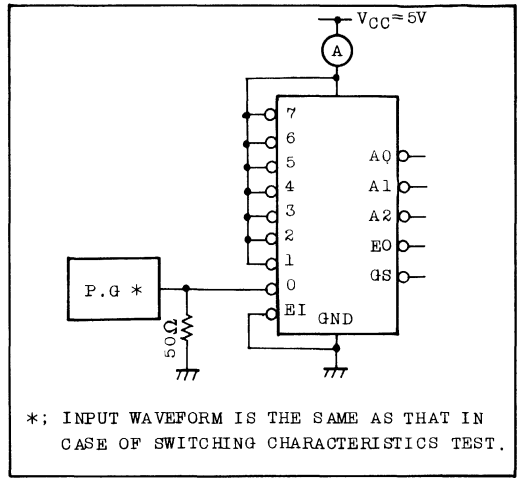
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN}$$

TC74HC148P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



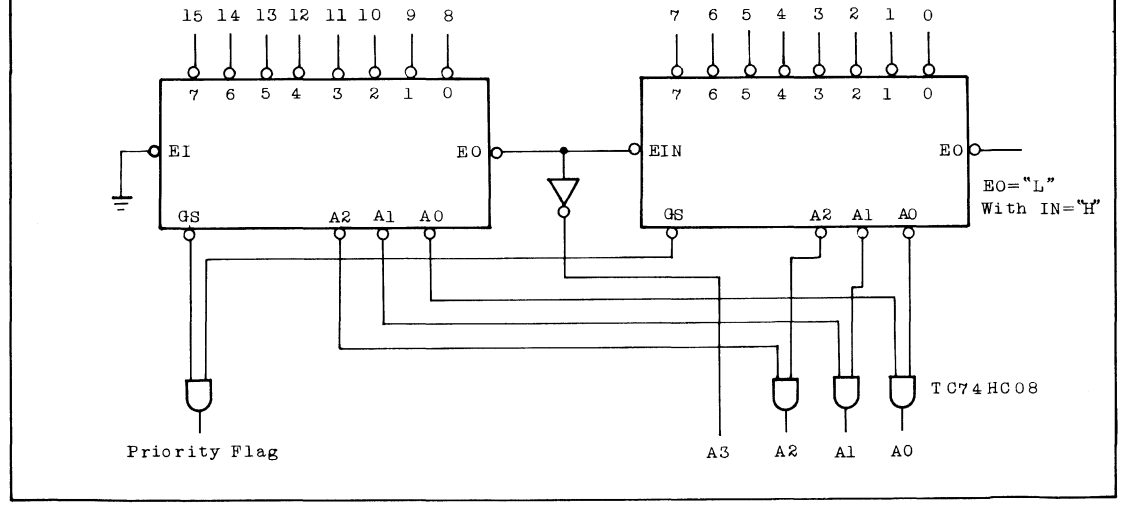
I_{CC}(Opr.) TEST WAVEFORM



*; INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

4-bit CASCADE CONNECTION



C²MOS DIGITAL INTEGRATED CIRCUIT

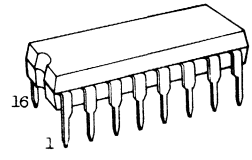
TC74HC151P/F

TC74HC151P/F 8-CHANNEL MULTIPLEXER

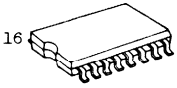
The TC74HC151 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. One of the eight data input signal (D0 - D7) is selected by a three-bit address input (A, B, C) and the selected data will be provided on two outputs; a non-invering output (Y) and a invering output (W). A strobe input is provided to control the output conditions; a low level on the strobe input brings the selected data on the outputs. On the other hand a high level on the strobe input provides the low level with Y output and the high level with W output without regard to the other input conditions.
All outputs are equipped protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS151



DIP16(3D16A-P)



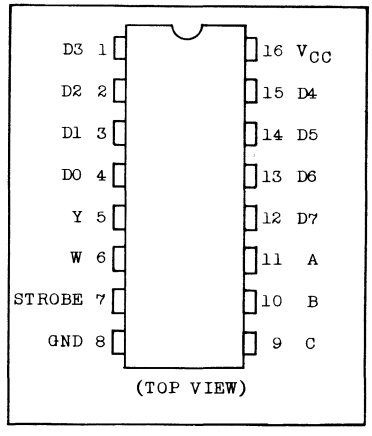
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

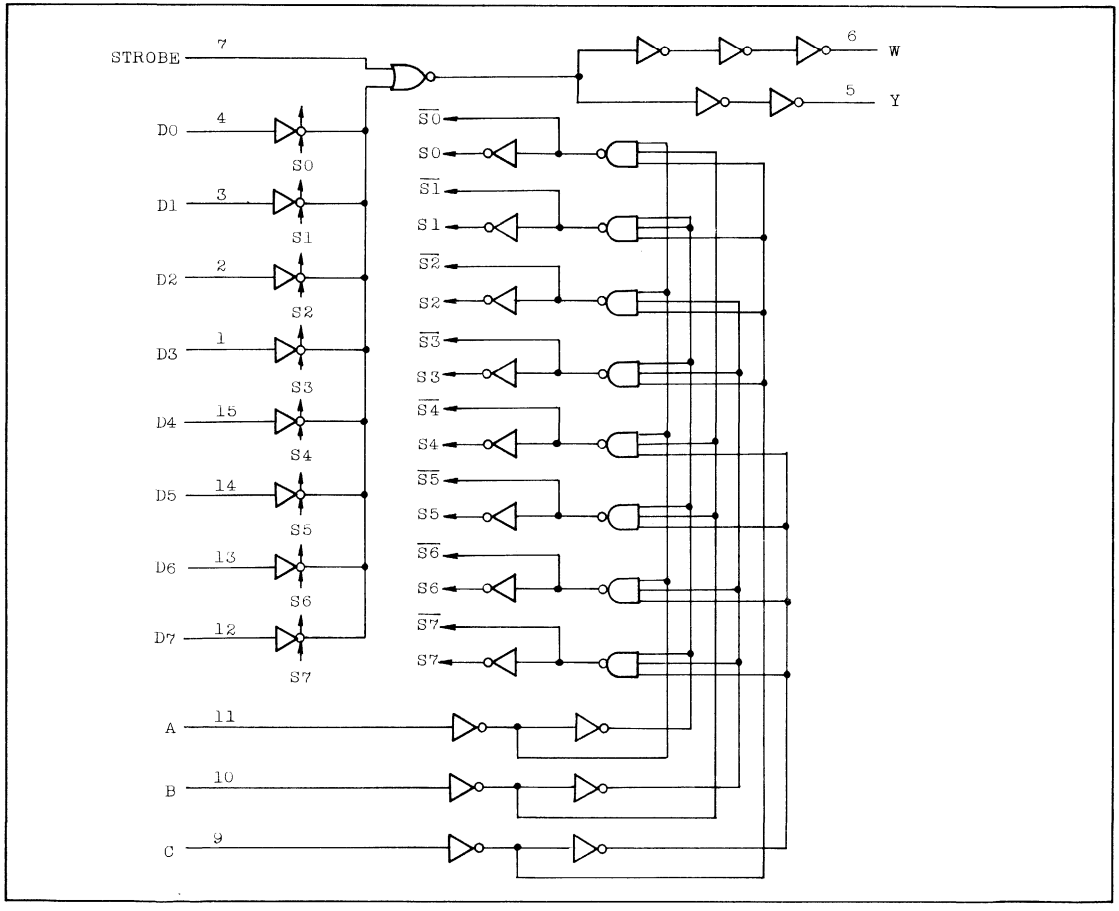
TC74HC151P/F

TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't Care

LOGIC DIAGRAM

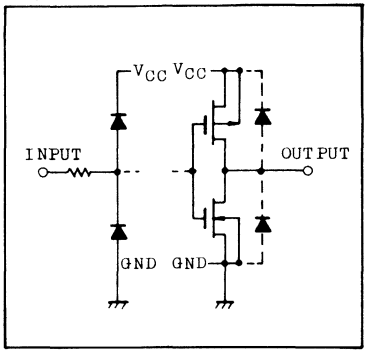


TC74HC151P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC151P/F

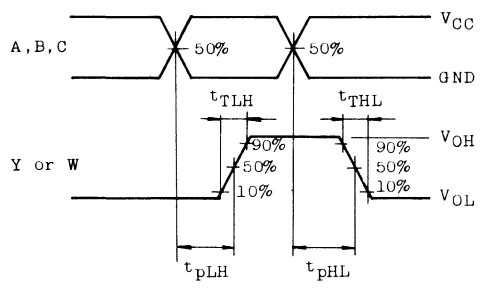
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

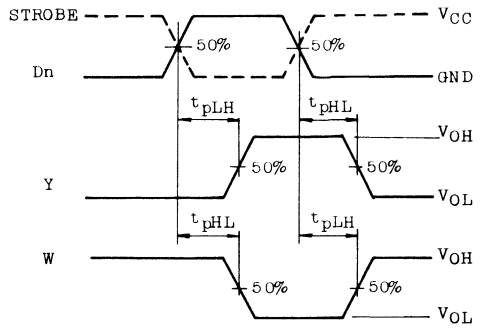
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (D - W)	t_{pLH}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
	t_{pHL}		6.0	-	18	28	-	35	
Propagation Delay Time (D - Y)	t_{pLH}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
	t_{pHL}		6.0	-	17	27	-	34	
Propagation Delay Time (ST - W)	t_{pLH}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
	t_{pHL}		6.0	-	12	20	-	25	
Propagation Delay Time (ST - Y)	t_{pLH}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
	t_{pHL}		6.0	-	11	18	-	22	
Propagation Delay Time (A, B, C - W)	t_{pLH}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
	t_{pHL}		6.0	-	22	35	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	75	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

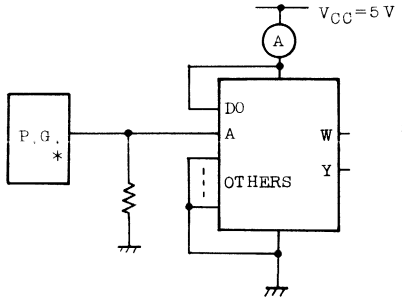
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM





$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC153P/F
TC74HC253P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC153P/F DUAL 4-CHANNEL MULTIPLEXER

TC74HC253P/F DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74HC153 and TC74HC253 are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C²MOS technology.

Both achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipations.

The designer has a choice of complementary output (HC153) and 3-state output (HC253).

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

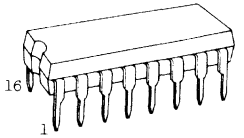
Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections.

The strobe input ($\overline{G}$) can be used to inhibit the data output; the output of HC153 is fixed in low level and the output of HC253 is disabled to be high impedance unconditionally, while the strobe input is held low.

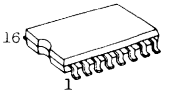
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS153/253.



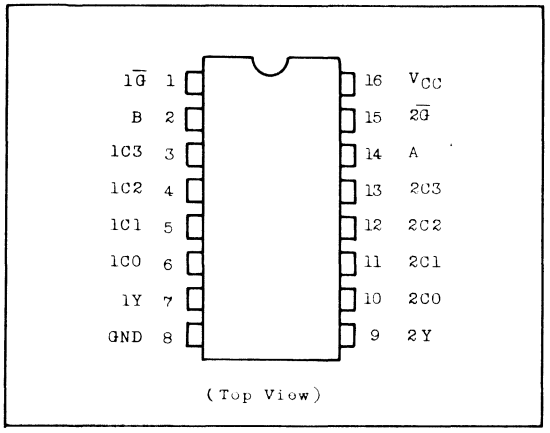
DIP16(3D16A-P)



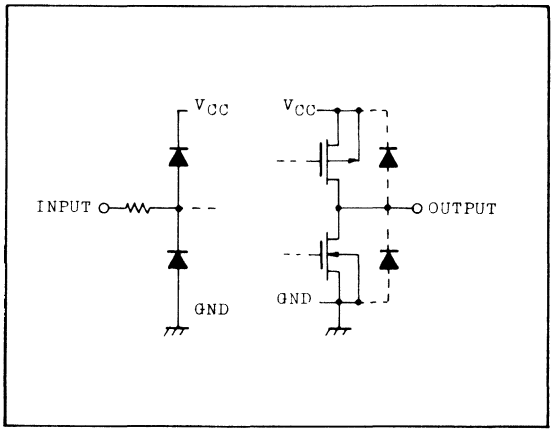
MFP16(F16GC-P)

TC74HC153P/F
TC74HC253P/F

PIN ASSIGNMENT



INPUT and OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

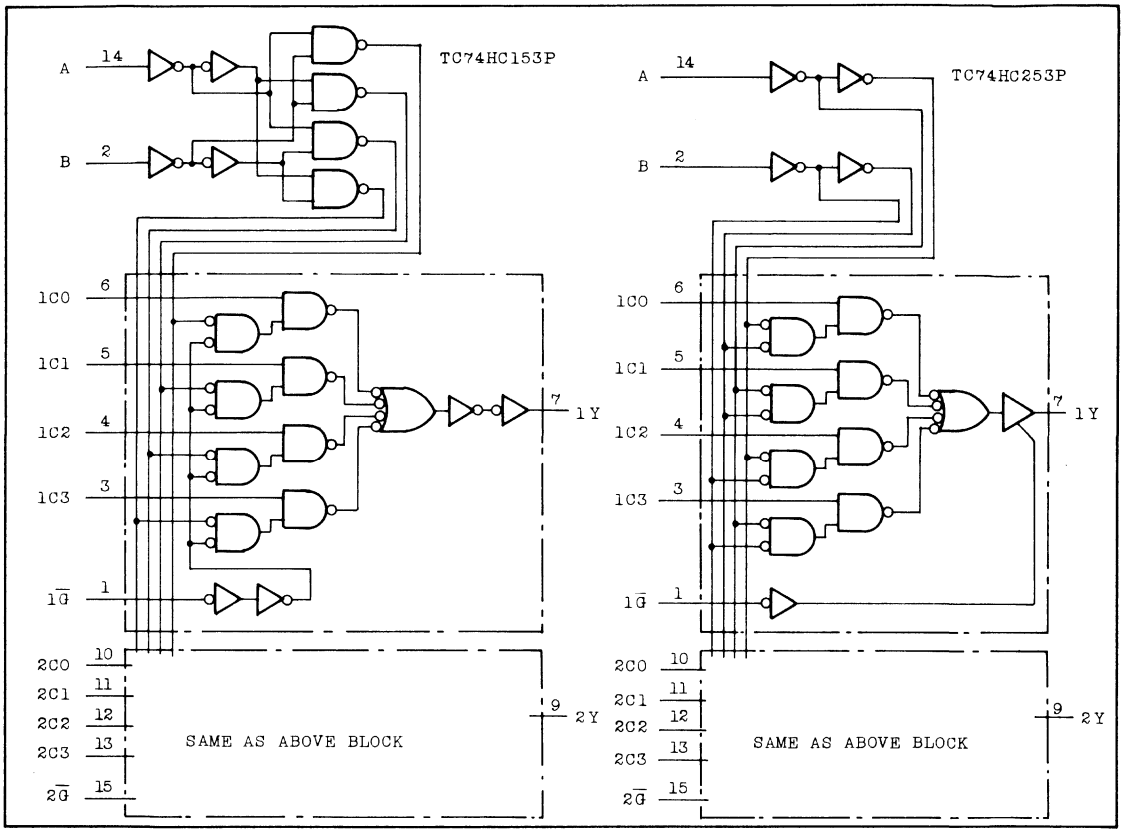
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC153	HC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X : Don't care

Z : High Impedance

TC74HC153P/F
TC74HC253P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}(1)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

Note (1) Applied only for TC74HC253P

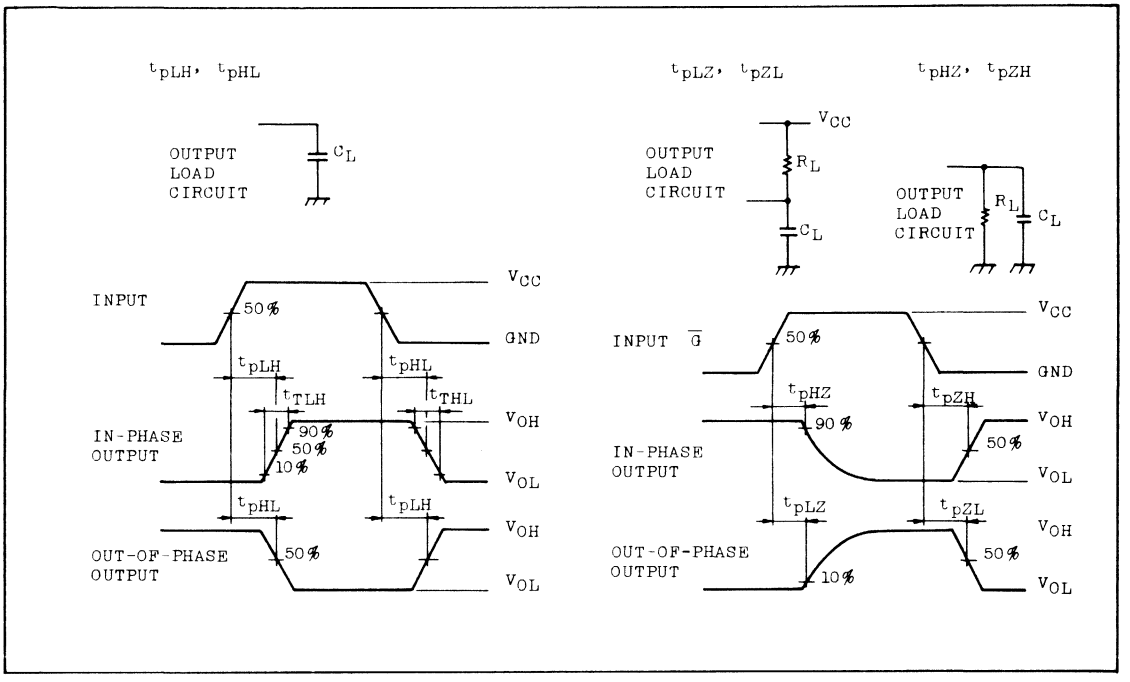
TC74HC153P/F
TC74HC253P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

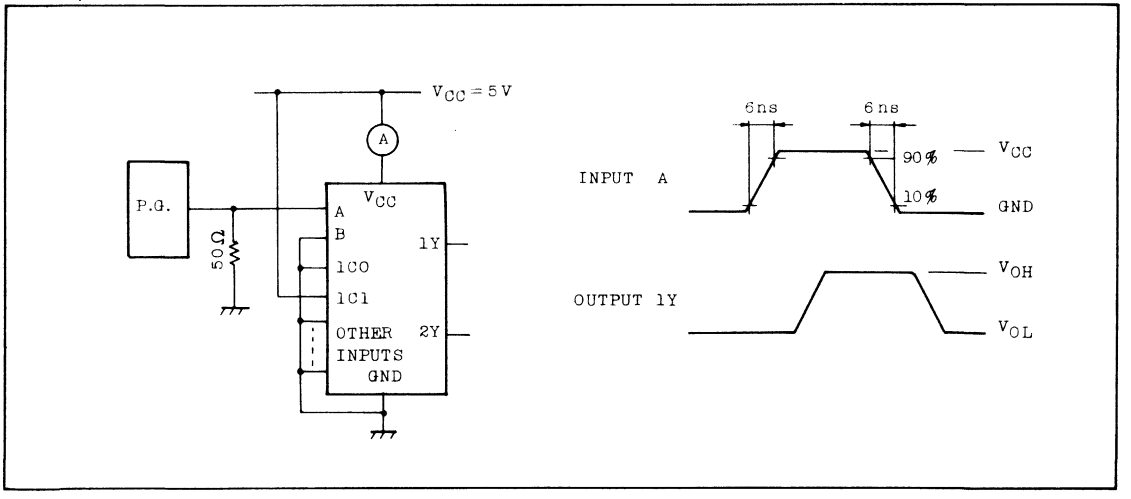
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	75	-	95	ns
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
TC74HC153/253 Propagation Delay Time C_n - Y	t_{pLH} t_{pHL}		2.0	-	68	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
TC74HC153/253 A,B - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC153 Propagation Delay Time $\overline{G}$ - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC253 Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	46	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
TC74HC253 Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	TC74HC253		-	7	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC153		-	56	-	-	-	
		TC74HC253		-	56	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Channel)

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC154P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC154P 4-LINE TO 16-LINE DECODER

The TC74HC154 is a high speed CMOS 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER fabricated with silicon gate CMOS technology.

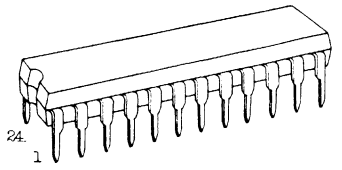
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A binary code applied to the four inputs (A thru D) provides a low level at the selected one of sixteen outputs excluding the other fifteen outputs, when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are held low.

When either strobe input is held high, the decording function is inhibited to keep all outputs high.

The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decording circuit in the memory control system.

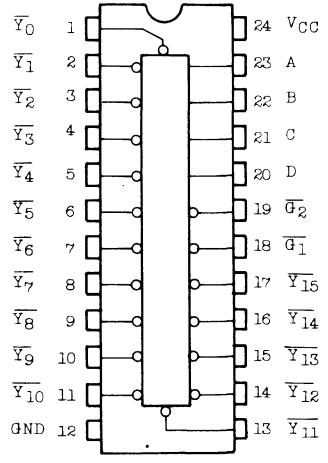
All inputs are equipped with protection circuit against static discharge or transient excess voltage.



DIP24-300A-P)

0.300 INCH (7.62) ROW SPACING

PIN ASSIGNMENT



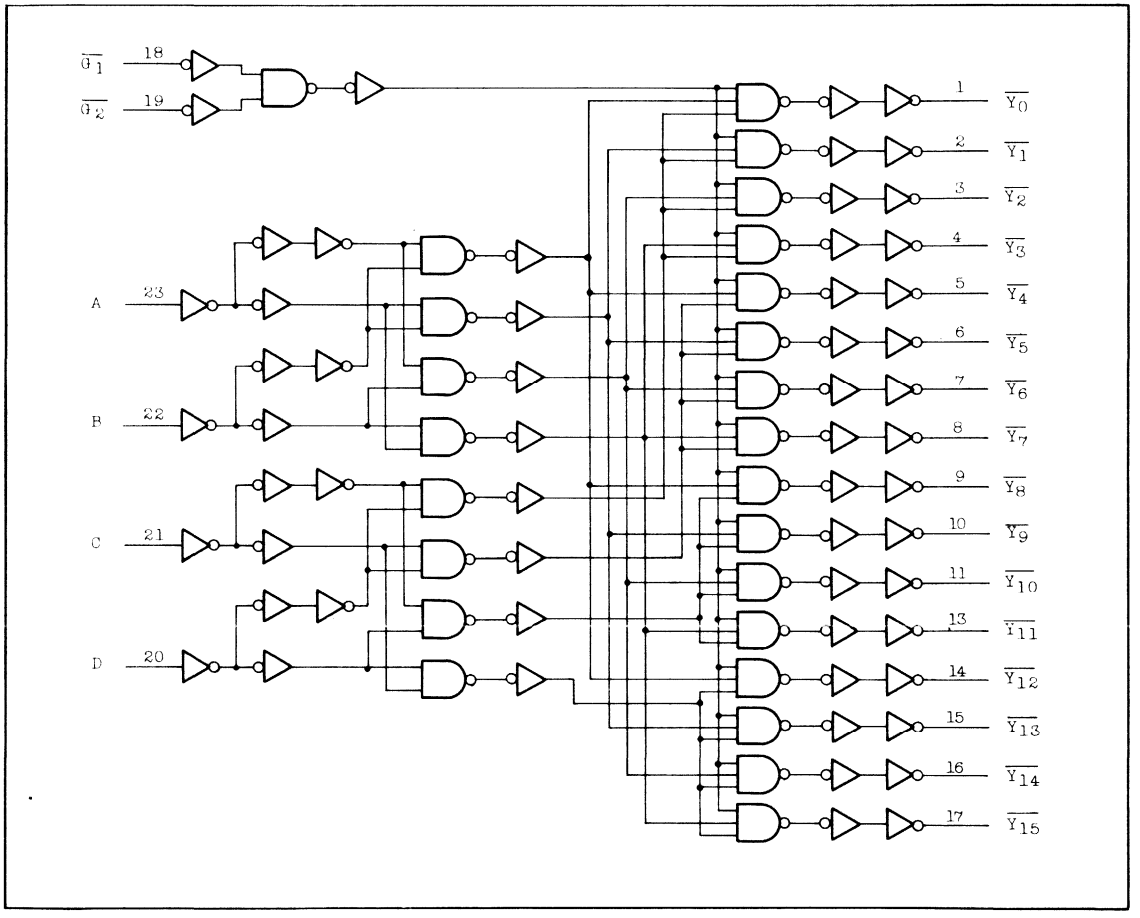
(Top View)

FEATURES:

- High Speed.....t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \doteqdot t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS154
- Small Package.....0.300(7.62) Row Spacing

TC74HC154P

LOGIC DIAGRAM



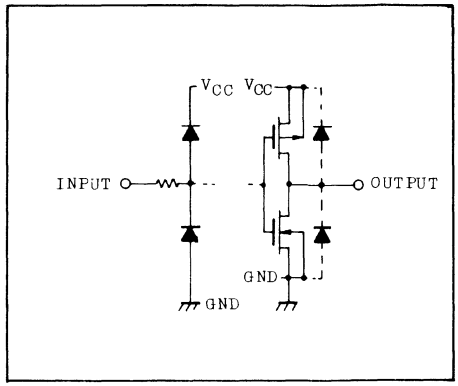
TC74HC154P

TRUTH TABLE

INPUTS						SELECTED OUTPUT (L)
$\overline{G}_1$	$\overline{G}_2$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y}_0$
L	L	L	L	L	H	$\overline{Y}_1$
L	L	L	L	H	L	$\overline{Y}_2$
L	L	L	L	H	H	$\overline{Y}_3$
L	L	L	H	L	L	$\overline{Y}_4$
L	L	L	H	L	H	$\overline{Y}_5$
L	L	L	H	H	L	$\overline{Y}_6$
L	L	L	H	H	H	$\overline{Y}_7$
L	L	H	L	L	L	$\overline{Y}_8$
L	L	H	L	L	H	$\overline{Y}_9$
L	L	H	L	H	L	$\overline{Y}_{10}$
L	L	H	L	H	H	$\overline{Y}_{11}$
L	L	H	H	L	L	$\overline{Y}_{12}$
L	L	H	H	L	H	$\overline{Y}_{13}$
L	L	H	H	H	L	$\overline{Y}_{14}$
L	L	H	H	H	H	$\overline{Y}_{15}$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC154P

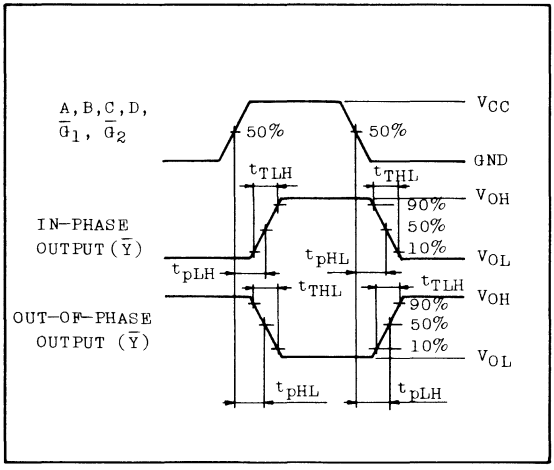
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	ns
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time ($\overline{G}_1$, $\overline{G}_2$ - Y)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	ns
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

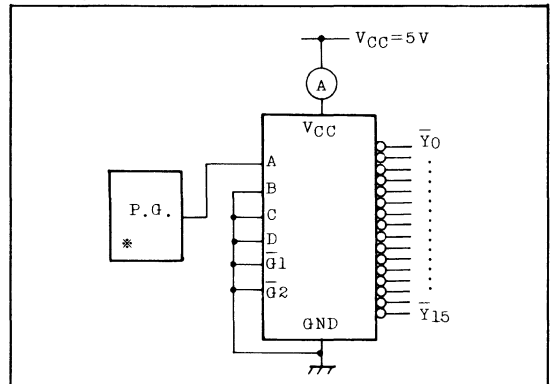
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC155P/F

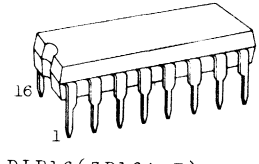
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC155P/F DUAL 2-TO-4 LINE DECODER/3-TO-8 LINE DECODER

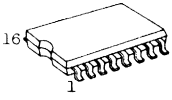
The TC74HC155 is a high speed CMOS 2-TO-4 LINE DECODER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It features dual 1-TO-4 line demultiplexers with individual strobe inputs (1G and $\overline{2G}$), individual data inputs (1C and $\overline{2C}$) and common binary address inputs (A and B). When both decoders are enabled by the strobes, the inverted output of 1C data and non-inverted output of $\overline{2C}$ data will be brought to the selected output pins of each sections. A 1-TO-8 line demultiplexer will be also easily built up by providing a data signal to both 1C and $\overline{2C}$ inputs; the output order from significance bit is $\overline{1Y3}$, $\overline{1Y2}$, $\overline{1Y1}$, $\overline{1Y0}$, $\overline{2Y3}$, $\overline{2Y2}$, $\overline{2Y1}$, $\overline{2Y0}$ (BOTTOM). This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and $\overline{2C}$ is held low. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS155



DIP16(3D16A-P)



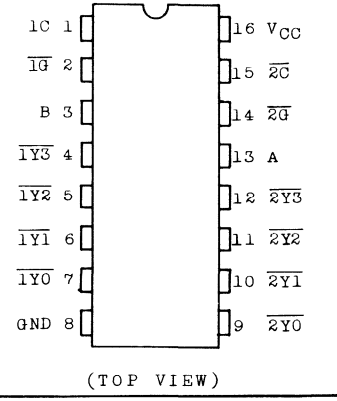
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC155P/F

TRUTH TABLE

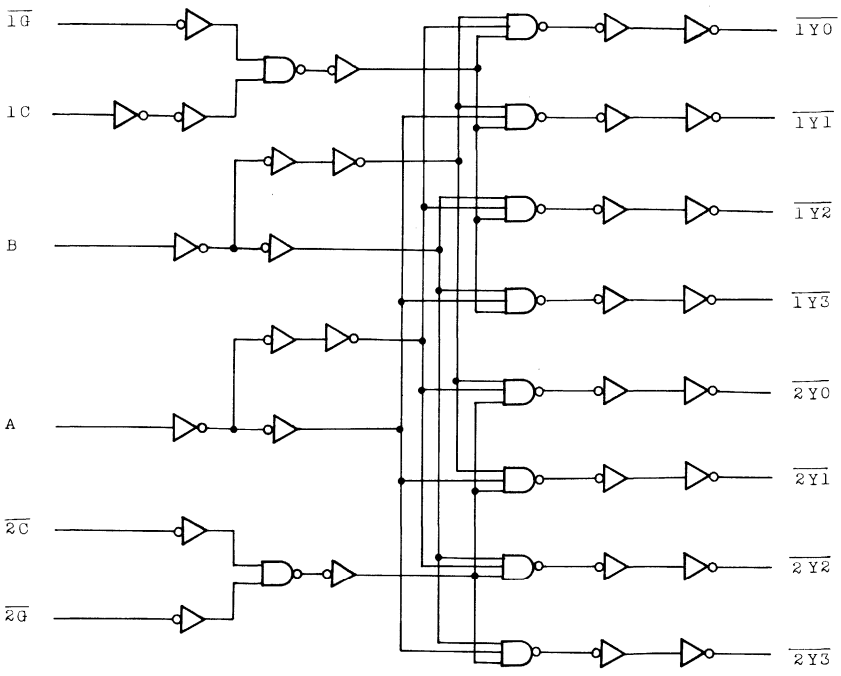
INPUTS				OUTPUTS			
B	A	$\overline{1G}$	1C	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X : DON'T CARE

INPUTS				OUTPUTS			
B	A	$\overline{2G}$	$\overline{2C}$	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y3}$	$\overline{2Y3}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

X : DON'T CARE

LOGIC DIAGRAM

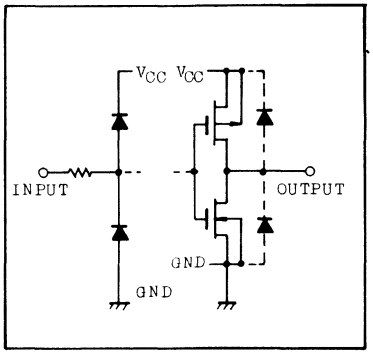


TC74HC155P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC155P/F

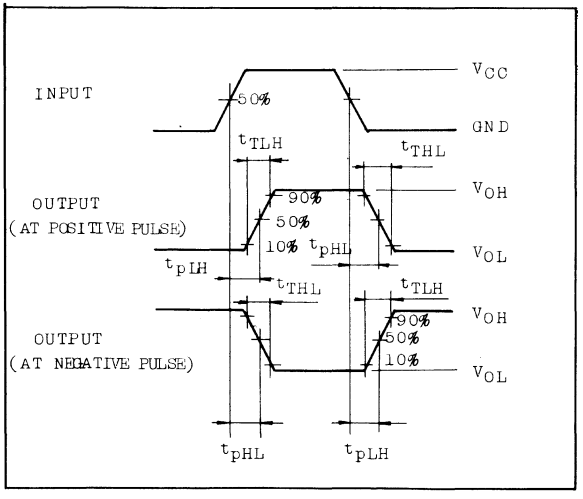
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	65	-	-	-	

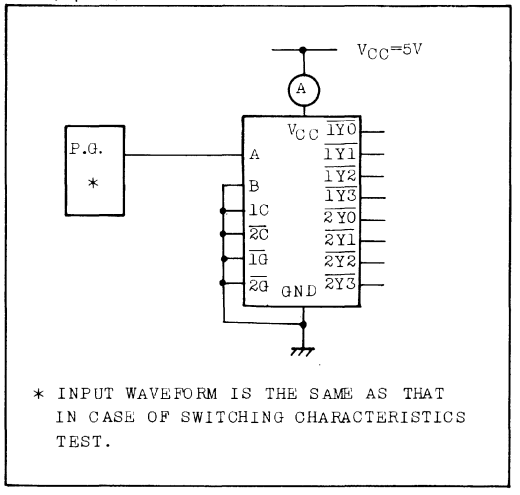
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC157P/F
TC74HC158P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

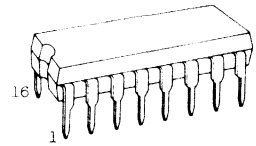
TC74HC157P/F QUAD 2-CHANNEL MULTIPLEXER

TC74HC158P/F QUAD 2-CHANNEL MULTIPLEXER (INVERTING)

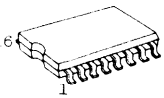
The TC74HC157 and the TC74HC158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low Power dissipation.
These devices consist of four 2-input digital multiplexers with common select and strobe inputs.
The TC74HC158 is an inverting multiplexer while the TC74HC157 is a non-inverting multiplexer.
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level in case of 157 and all the outputs become "H" level in case of 158.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS157/158.



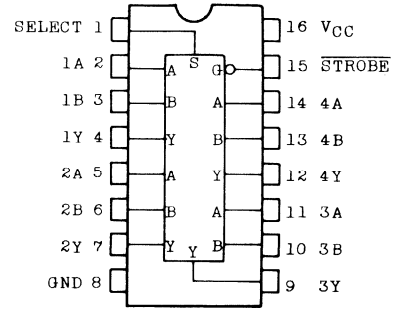
DIP16(SD16A-P)



MFP16(F16GC-P)

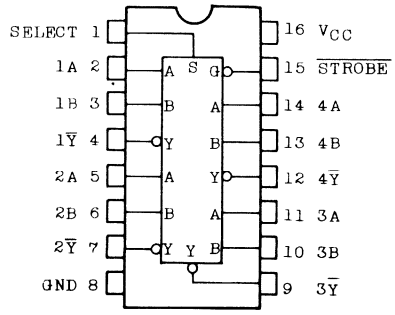
PIN ASSIGNMENT

TC74HC157



(TOP VIEW)

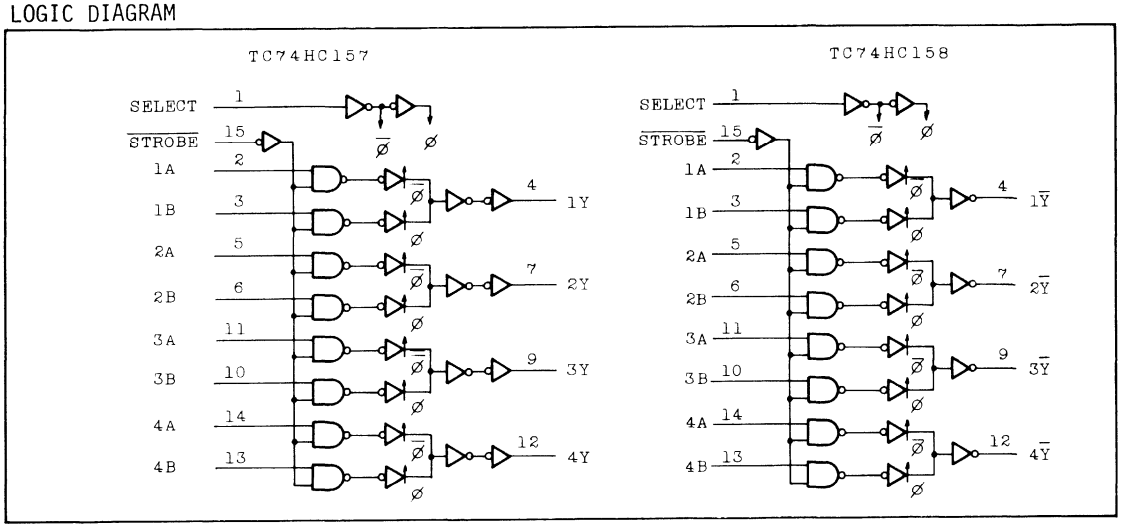
TC74HC158



(TOP VIEW)

TC74HC157P/F
TC74HC158P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{\text{STROBE}}$	SELECT	A	B	Y (157)	$\overline{\text{Y}}$ (158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

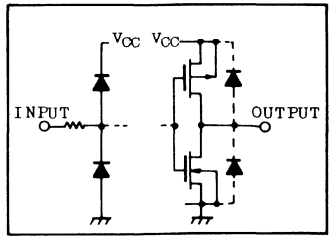
* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC157P/F
TC74HC158P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC157P/F
TC74HC158P/F

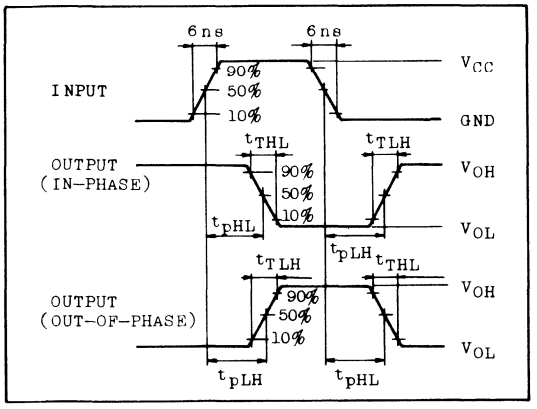
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
TC74HC157 Propagation Delay Time A,B -Y	t_{pLH} t_{pHL}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
SELECT - Y	t_{pLH} t_{pHL}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
$\overline{\text{STROBE}}$ - Y	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
TC74HC158 Propagation Delay Time A,B - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	46	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
SELECT - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
$\overline{\text{STROBE}}$ - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Input Capacitance	C_{IN}			-	6	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC157		-	53	-	-	-	
		TC74HC257		-	51	-	-	-	

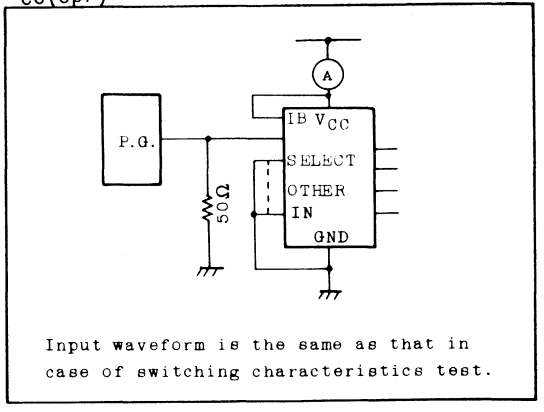
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Channel)

TC74HC157P/F
TC74HC158P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC160P/F·TC74HC161P/F
TC74HC162P ·TC74HC163P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

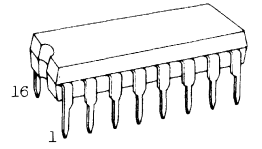
SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

TC74HC160P/F DECADE, ASYNCHRONOUS CLEAR
TC74HC161P/F BINARY, ASYNCHRONOUS CLEAR
TC74HC162P DECADE, SYNCHRONOUS CLEAR
TC74HC163P/F BINARY, SYNCHRONOUS CLEAR

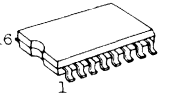
The TC74HC160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC160/162 are BCD decode counters and the TC74HC161/163 are 4 bit binary counters.
The CLOCK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ inputs are active on "L" level.
Presetting of all four IC's is synchronous to the rising edge of CLOCK.
Clear function on the TC74HC162/163 is synchronous to CLOCK, while the TC74HC160/161 counters are cleared asynchronously.
Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilitates easy implementation of N-bit counters without using external gate.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=50MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS160~163.

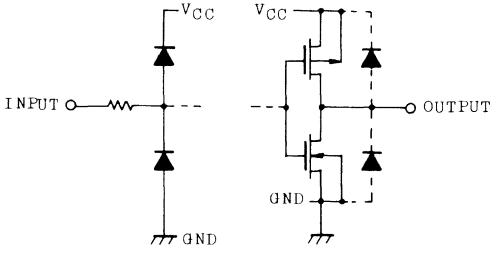


DIP16(3D16A-P)

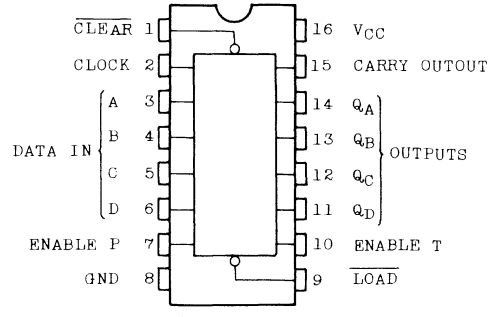


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGNMENT



(TOP VIEW)

TC74HC160P/F·TC74HC161P/F TC74HC162P ·TC74HC163P/F

TRUTH TABLE

TC74HC160/161					TC74HC162/163					OUTPUTS				FUNCTION
INPUTS					INPUTS									
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↓	L	L	L	L	RESET TO "0"
H	L	X	X	↓	H	L	X	X	↓	A	B	C	D	PRESET DATA
H	H	X	L	↓	H	H	X	L	↓	NO CHANGE				NO COUNT
H	H	L	X	↓	H	H	L	X	↓	NO CHANGE				NO COUNT
H	H	H	H	↓	H	H	H	H	↓	COUNT UP				COUNT
H	X	X	X	↑	X	X	X	X	↑	NO CHANGE				NO COUNT

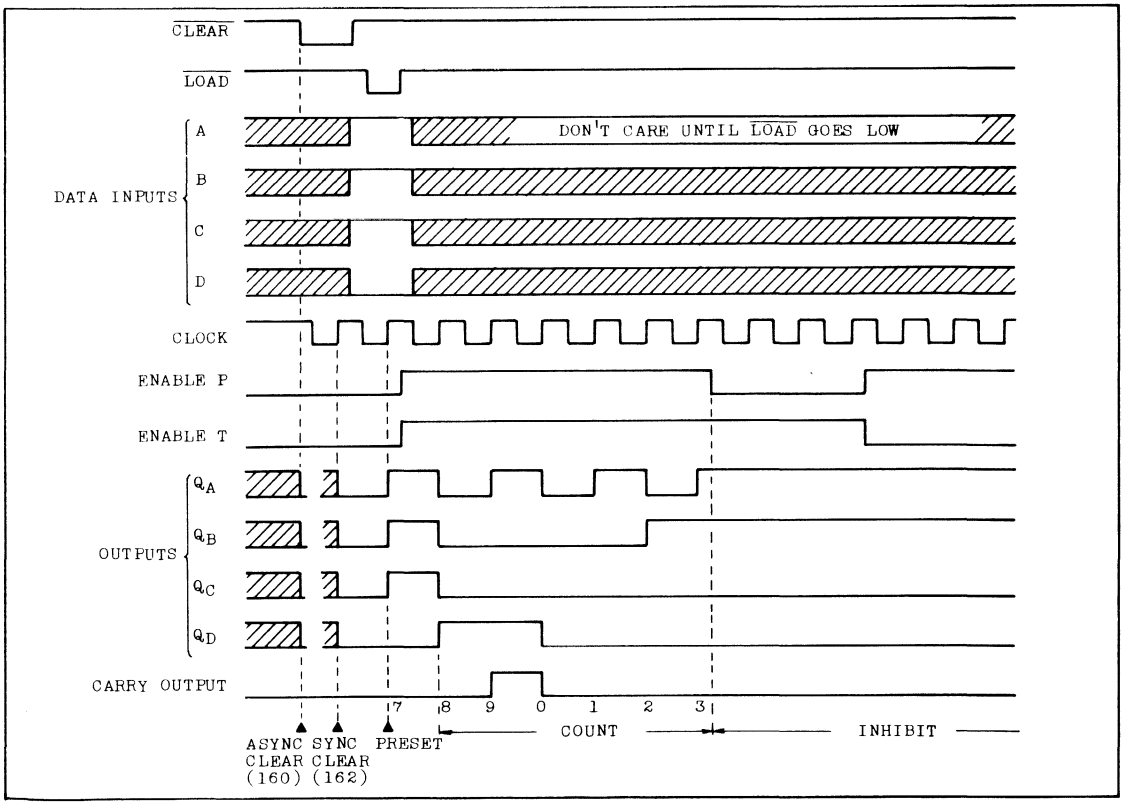
Note X ; Don't Care

A, B, C, D ; Logic level of data inputs

Carry ; CARRY = $TE \cdot Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot Q_D$ ····· (TC74HC160/162)

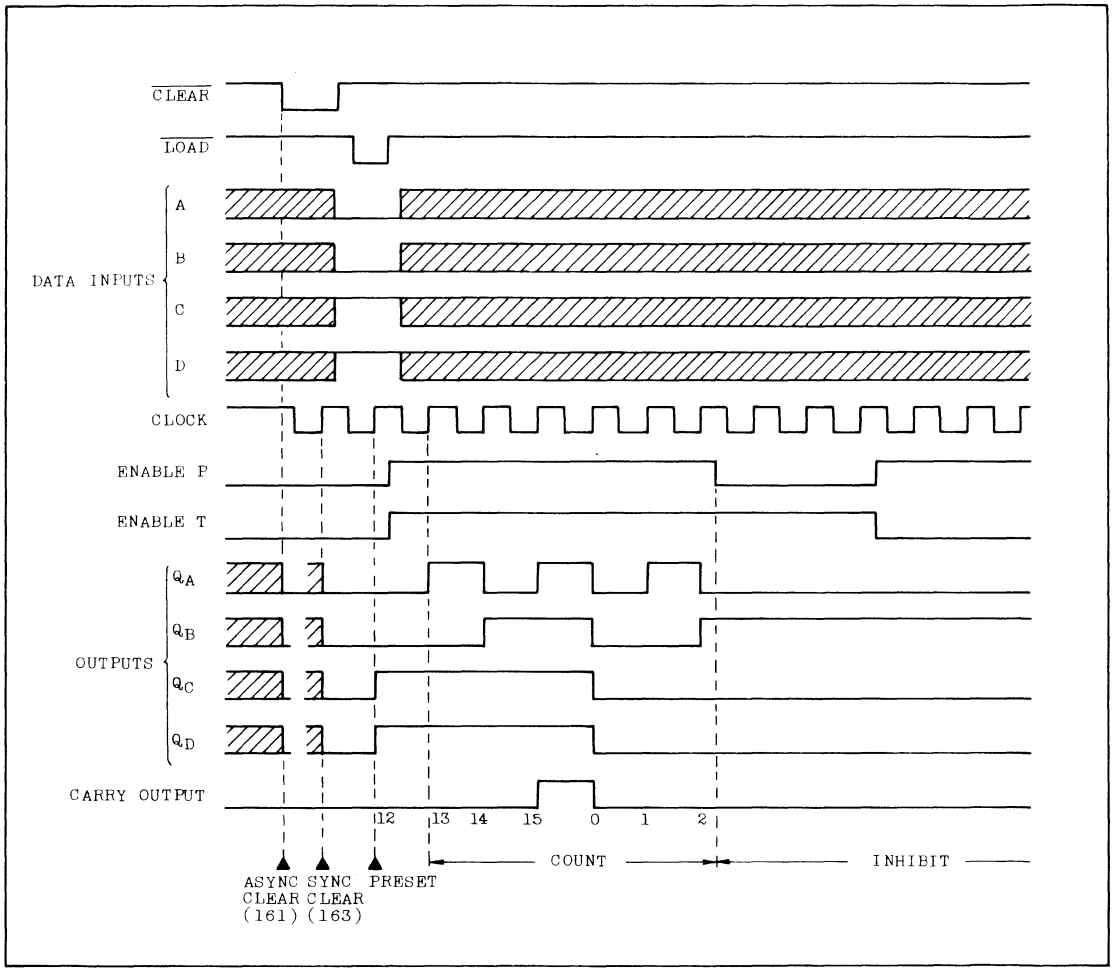
CARRY = $TE \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$ ····· (TC74HC161/163)

TIMING CHART (TC74HC160/162 : DECADE COUNTER)



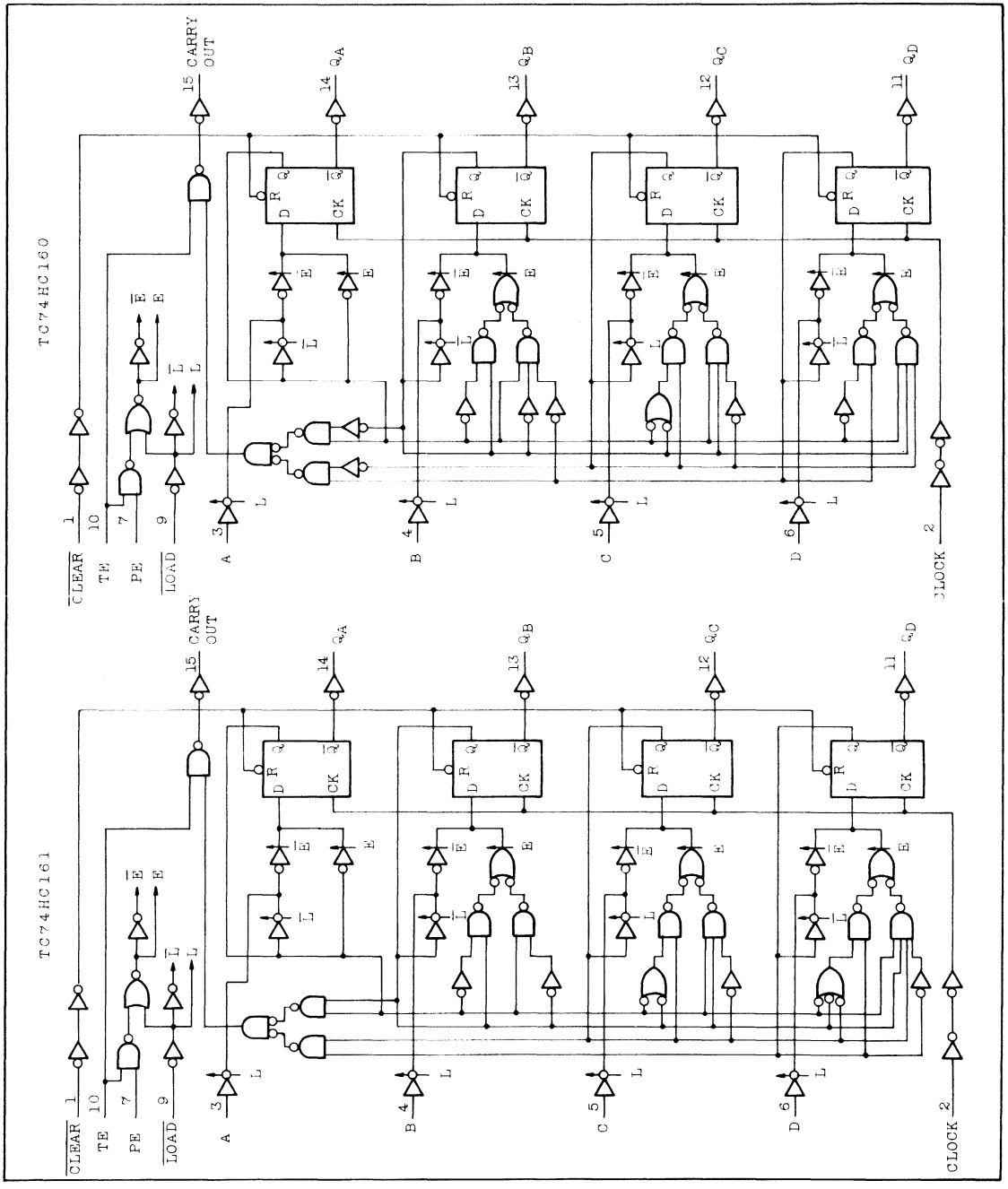
TC74HC160P/F • TC74HC161P/F
TC74HC162P • TC74HC163P/F

TIMING CHART (TC74HC161/163 : BINARY COUNTER)



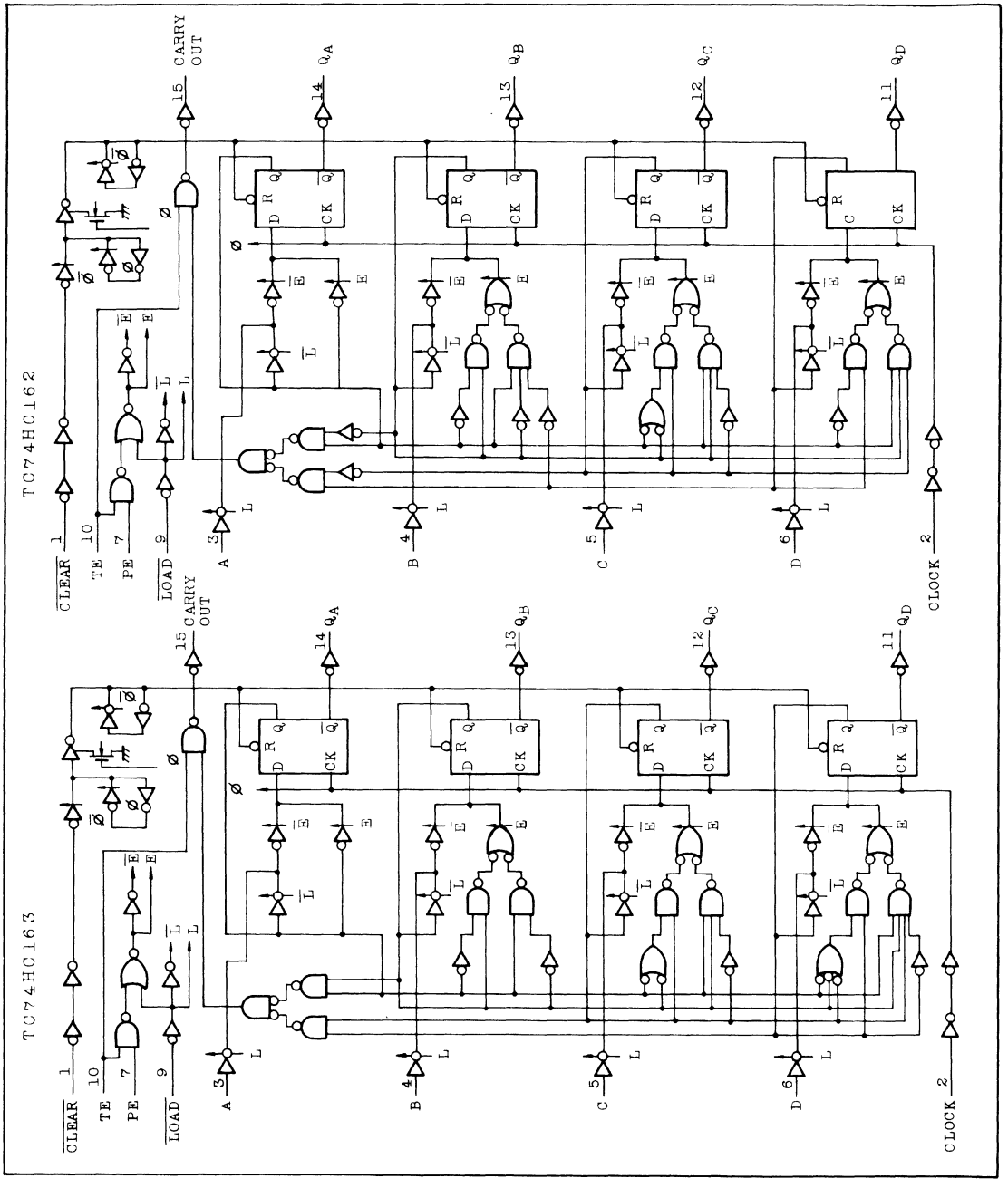
TC74HC160P/F・TC74HC161P/F
TC74HC162P ・TC74HC163P/F

LOGIC DIAGRAM



TC74HC160P/F • TC74HC161P/F
TC74HC162P • TC74HC163P/F

LOGIC DIAGRAM



TC74HC160P/F·TC74HC161P/F TC74HC162P ·TC74HC163P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC160P/F • TC74HC161P/F
TC74HC162P • TC74HC163P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	88	165	-	205	
			4.5	-	22	33	-	41	
			6.0	-	19	28	-	35	
CLOCK - CARRY	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
TE - CARRY	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
$\overline{CLEAR}$ - Q*	t_{pHL}		2.0	-	100	185	-	230	
			4.5	-	25	37	-	46	
			6.0	-	21	31	-	39	
$\overline{CLEAR}$ - CARRY*	t_{pHL}		2.0	-	112	210	-	265	
			4.5	-	28	42	-	53	
			6.0	-	24	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	45	-	22	-	
			6.0	32	53	-	26	-	

TC74HC160P/F·TC74HC161P/F TC74HC162P ·TC74HC163P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
$\overline{CLEAR}$ *	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time $\overline{LOAD}$, PE, TE	t_s		2.0	-	50	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
A, B, C, D	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
$\overline{CLEAR}$ **	t_s		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{CLEAR}$ *	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Input Capacitance	C_{IN}			-	5	7.5	-	7.5	pF
Power Dissipation Capacitance	C_{PD}(1)			-	57	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

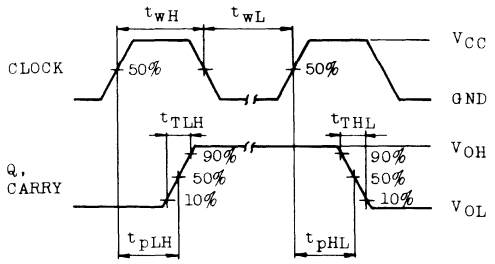
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

(2) * for TC74HC160/161 only
** for TC74HC162/163 only

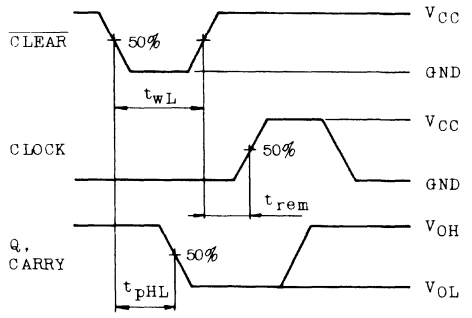
TC74HC160P/F·TC74HC161P/F
TC74HC162P ·TC74HC163P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

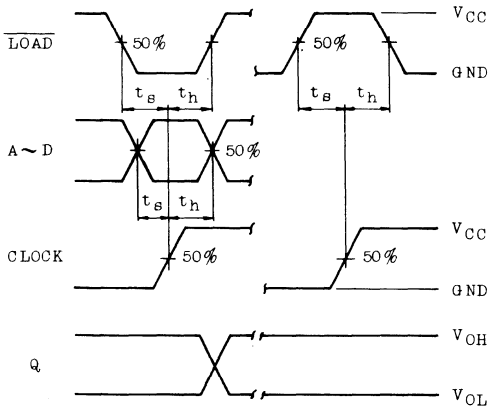
COUNT MODE



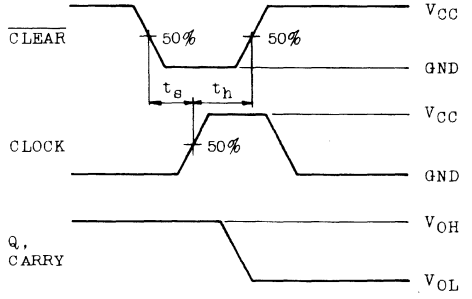
CLEAR MODE (TC74HC160P/161P)



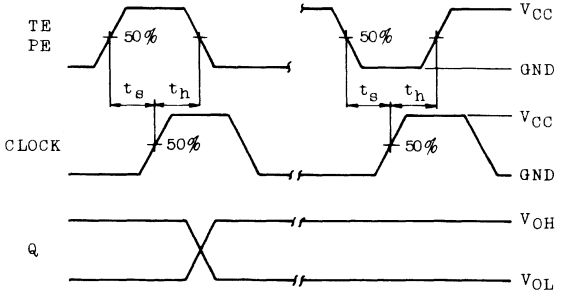
PRESET MODE



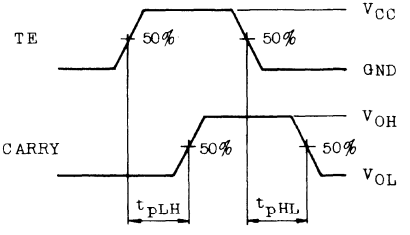
CLEAR MODE (TC74HC162P/163P)



COUNT ENABLE MODE

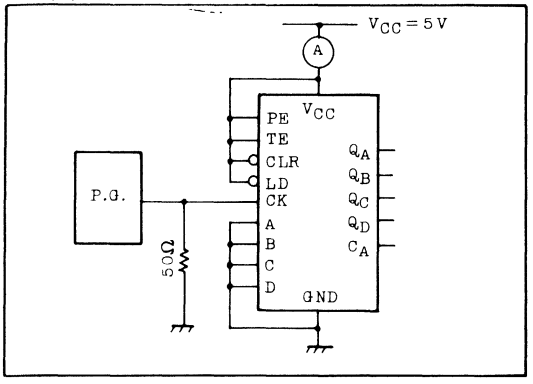


CASCADE MODE
(Fix Maximum Count)



TC74HC160P/F·TC74HC161P/F
TC74HC162P ·TC74HC163P/F

$I_{CC(opr)}$ TEST CIRCUIT



OPERATING CURRENT CONSUMPTION WITH LOAD CAPACITANCE

When the outputs drive capacitive load, total current consumption is to be a sum of the value calculated from C_{PD} and ΔI_{CC} obtained from the following formula.

In case of TC74HC160/162

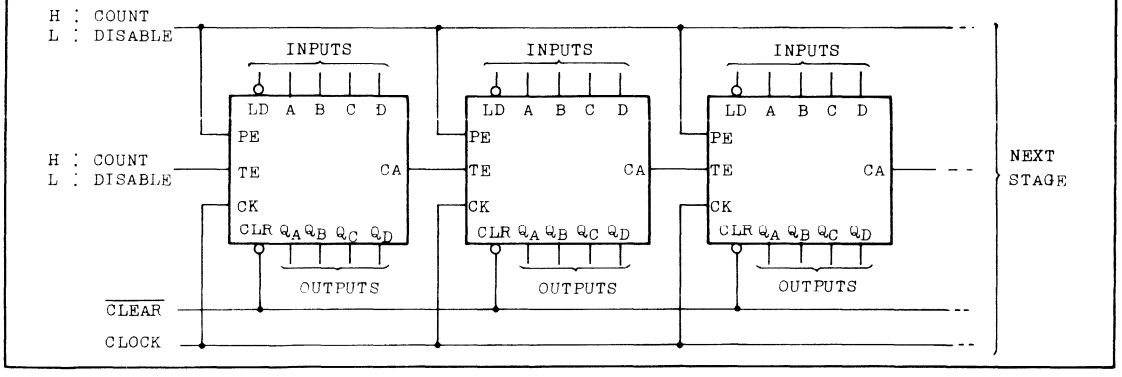
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

In case of TC74HC161/163

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

$C_a \sim C_{ca}$ are the capacitance at $Q_A \sim$ CARRY output.

TYPICAL APPLICATION



TC74HC164P/F

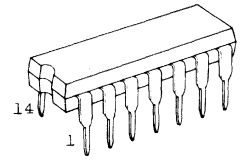
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC164P/F 8-BIT SHIFT REGISTER (S-IN, P-OUT)

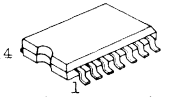
The TC74HC164 is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of serial-in, parallel-out 8-bit shift register with a clock inputs and an overriding clear input. Two serial data inputs (A, B) are provided so that one input may be used as a data enable.
Data is shifted serially through the shift register on the positive going transition of the clock input.
A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=50MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS164



DIP14(3D14A-P)



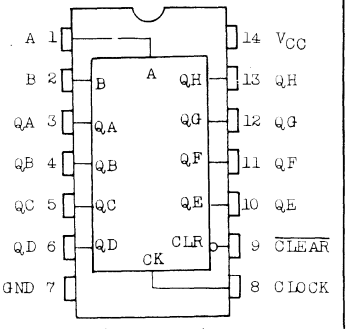
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC164P/F

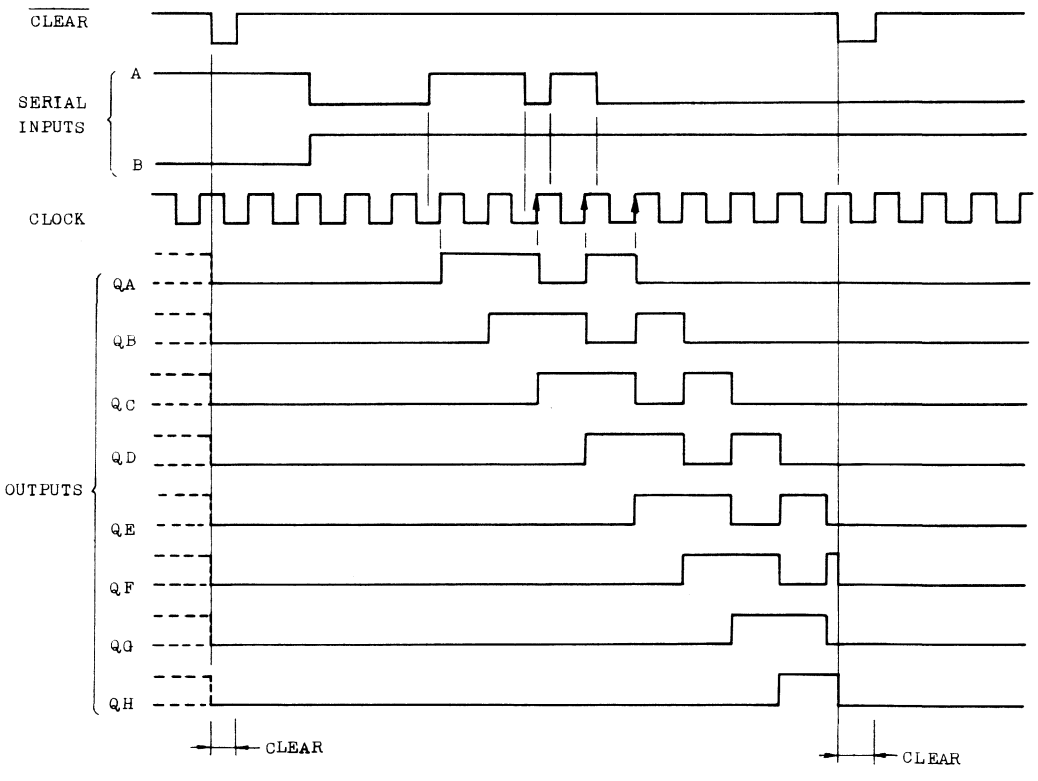
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLEAR}$	CLOCK	SERIAL IN		QA	QB	·····	QH
		A	B				
L	X	X	X	L	L	·····	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	·····	QGn
H	↑	X	L	L	QAn	·····	QGn
H	↑	H	H	H	QAn	·····	QGn

X : DON'T CARE

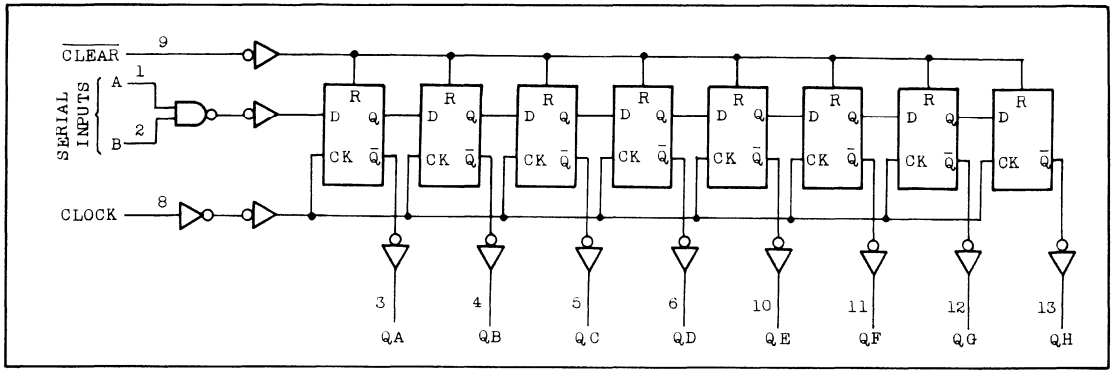
QAn~QGn : THE LEVEL OF QA~QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

TIMING CHART



TC74HC164P/F

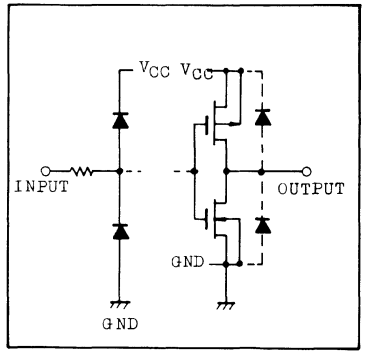
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn)	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	
Propagation Delay Time ($\overline{CLEAR}$ - Qn)	t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	46	-	22	-	
			6.0	32	54	-	26	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	96	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Set-up Time (A, B)	t_s		2.0	-	25	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	

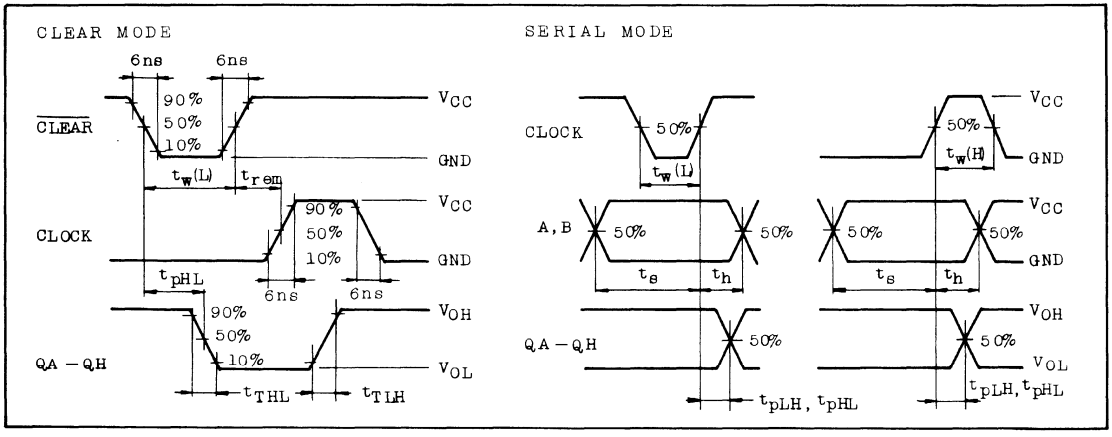
TC74HC164P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

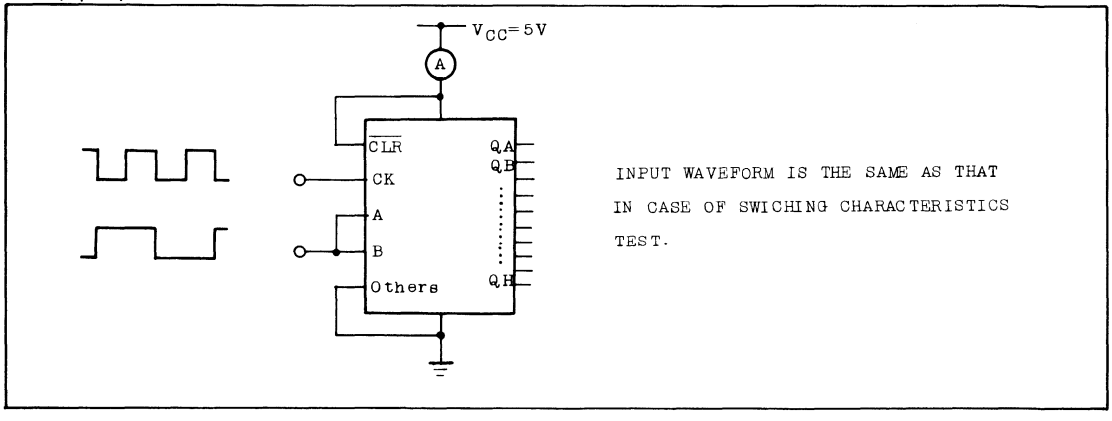
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Hold Time (A, B)	t_h		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	112	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWICHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

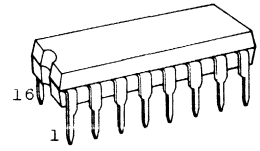
TC74HC165P/F

TC74HC165P/F 8-BIT SHIFT REGISTER (P-IN, S-OUT)

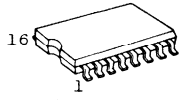
The TC74HC165 is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock input.
When the SHIFT/$\overline{LOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.
When the SHIFT/$\overline{LOAD}$ input is held low, the parallel data is loaded asychronously into the register.
Clocking is accomplished on the positive going transition of the clock pulse.
The CLOCK-INHIBIT input should be changed to the high level only while the CLOCK input is held high.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=48MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delay ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS165



DIP16(3D16A-P)



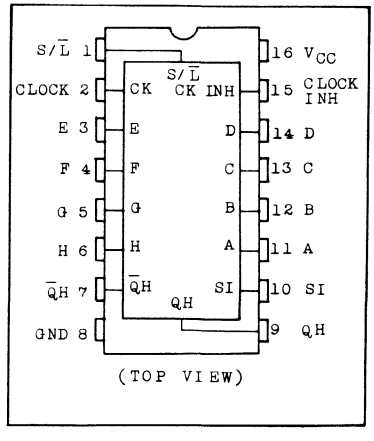
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC165P/F

TRUTH TABLE

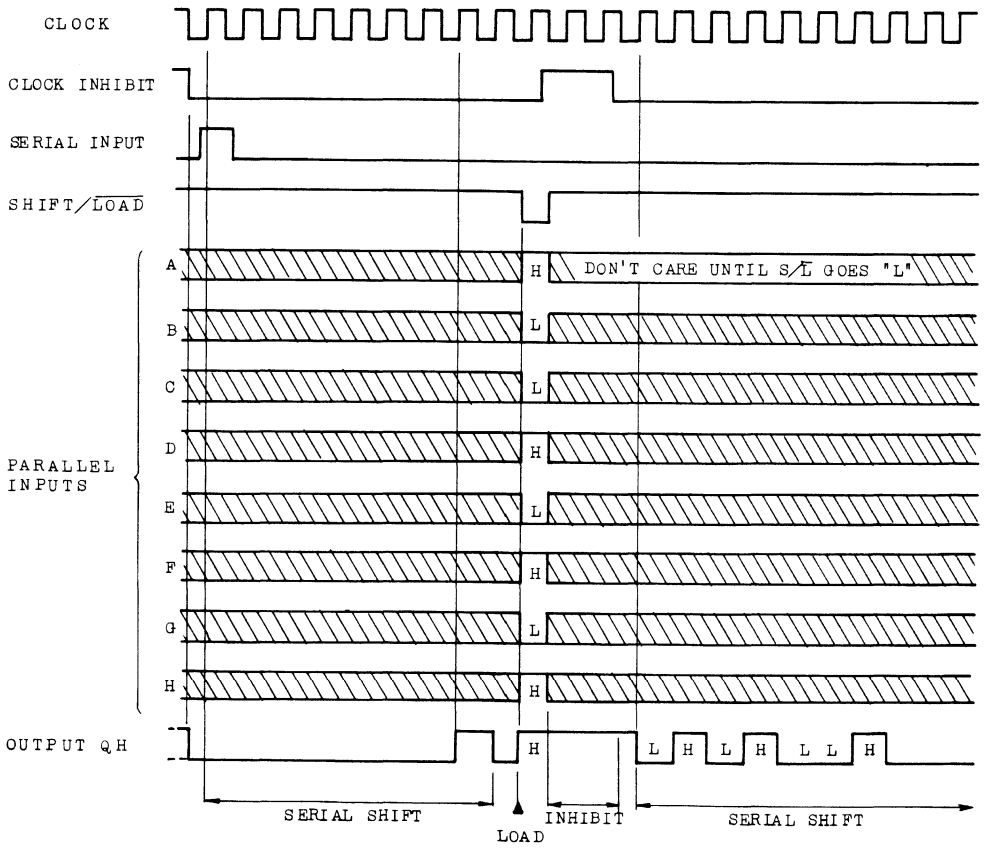
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/$\overline{\text{LOAD}}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A ····· H	Q_A	Q_B	Q_H
L	X	X	X	a ····· h	a	b	h
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	L	H	X	H	Q_{An}	Q_{Gn}
H	↑	L	L	X	L	Q_{An}	Q_{Gn}
H	X	H	X	X	No change		
H	H	X	X	X	No change		

X : DON'T CARE

a ····· h : THE LEVEL OF STEADY INPUT VOLTAGE AT INPUTS A THROUGH H RESPECTIVELY

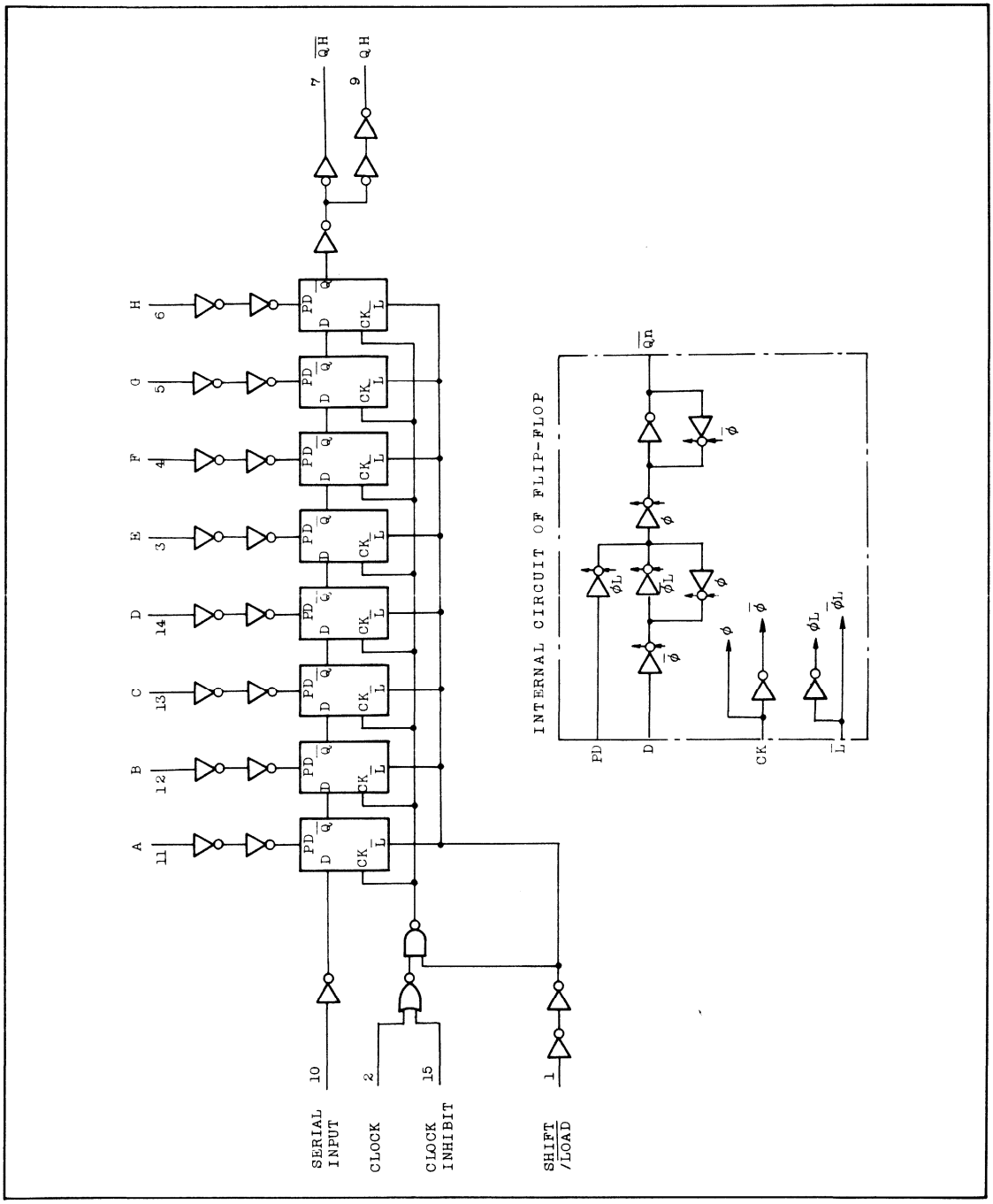
Q_{An} ··· Q_{Gn} : THE LEVEL OF Q_A~Q_G, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

TIMING CHART



TC74HC165P/F

LOGIC DIAGRAM

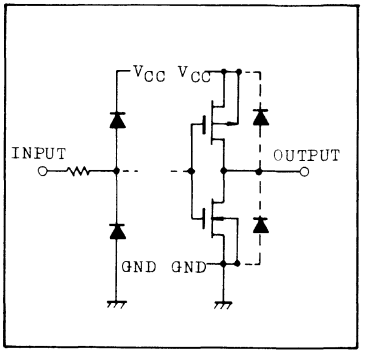


TC74HC165P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT tr=tf=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (CK, CK INH - QH, $\overline{Q}$H)	t_{pLH}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
	t_{pHL}		6.0	-	20	32	-	41	
Propagation Delay Time (S/$\overline{L}$ - QH, $\overline{Q}$H)	t_{pLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
	t_{pHL}		6.0	-	22	34	-	43	
Propagation Delay Time (H - QH, $\overline{Q}$H)	t_{pLH}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
	t_{pHL}		6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	25	44	-	20	-	
			6.0	29	52	-	24	-	
Minimum Pulse Width (CK, CK INH)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width (S/$\overline{L}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (PI-S/$\overline{L}$)	t_s		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (SI-CK, CK INH)	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Set-up Time (S/L-CK, CK INH)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (PI - S/$\overline{L}$) (SI - CK, CK INH)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (S/$\overline{L}$ - CK, CK INH)	t_h		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time (CK INH - CK) (CK - CK INH)	t_{rem}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	95	-	-	-	

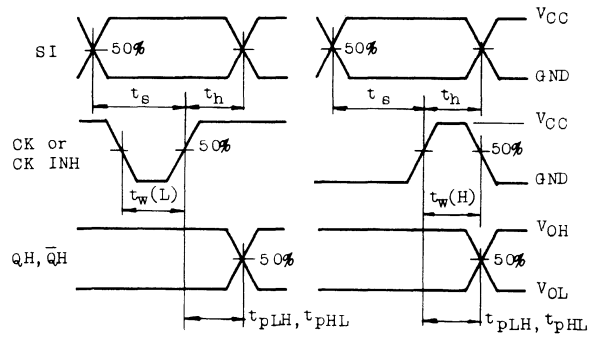
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

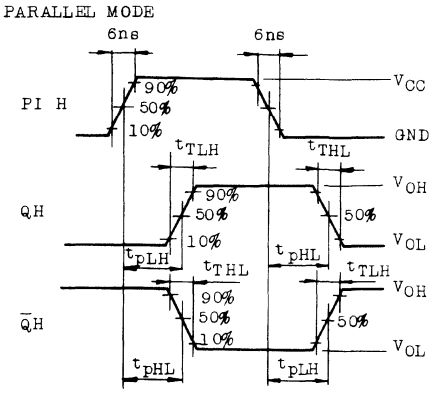
TC74HC165P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

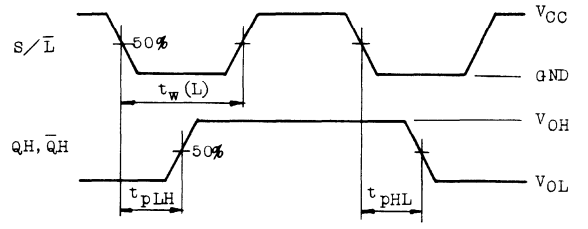
SERIAL MODE



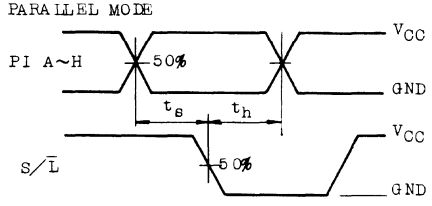
PARALLEL MODE



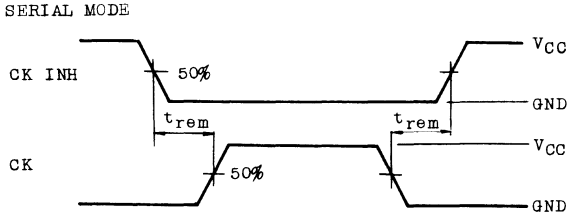
PARALLEL MODE



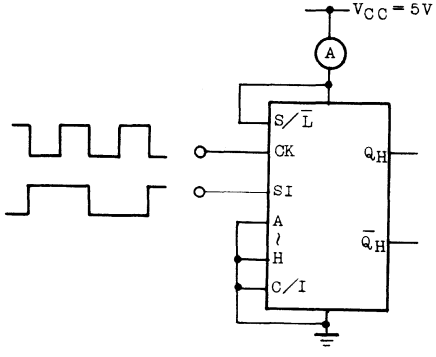
PARALLEL MODE



SERIAL MODE



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

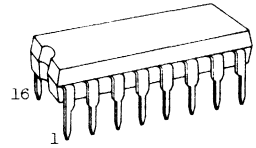
TC74HC166P/F

TC74HC166P/F 8-BIT SHIFT REGISTER (P-IN, S-OUT)

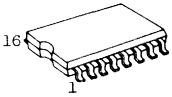
The TC74HC166 is a high speed CMOS 8 BIT PARALLEL/SERIAL-IN SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When held low, the parallel data inputs are enabled and synclonous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse. The CLOCK-INHIBIT input should be changed to the high level only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flop to zero. The detail about the function is shown at the truth table and the timing chart. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delay ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V∿6V
- Pin and Function Compatible with 74LS166



DIP16(3D16A-P)



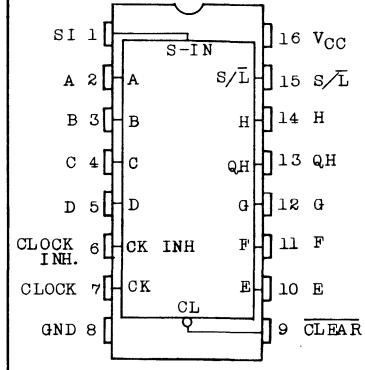
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

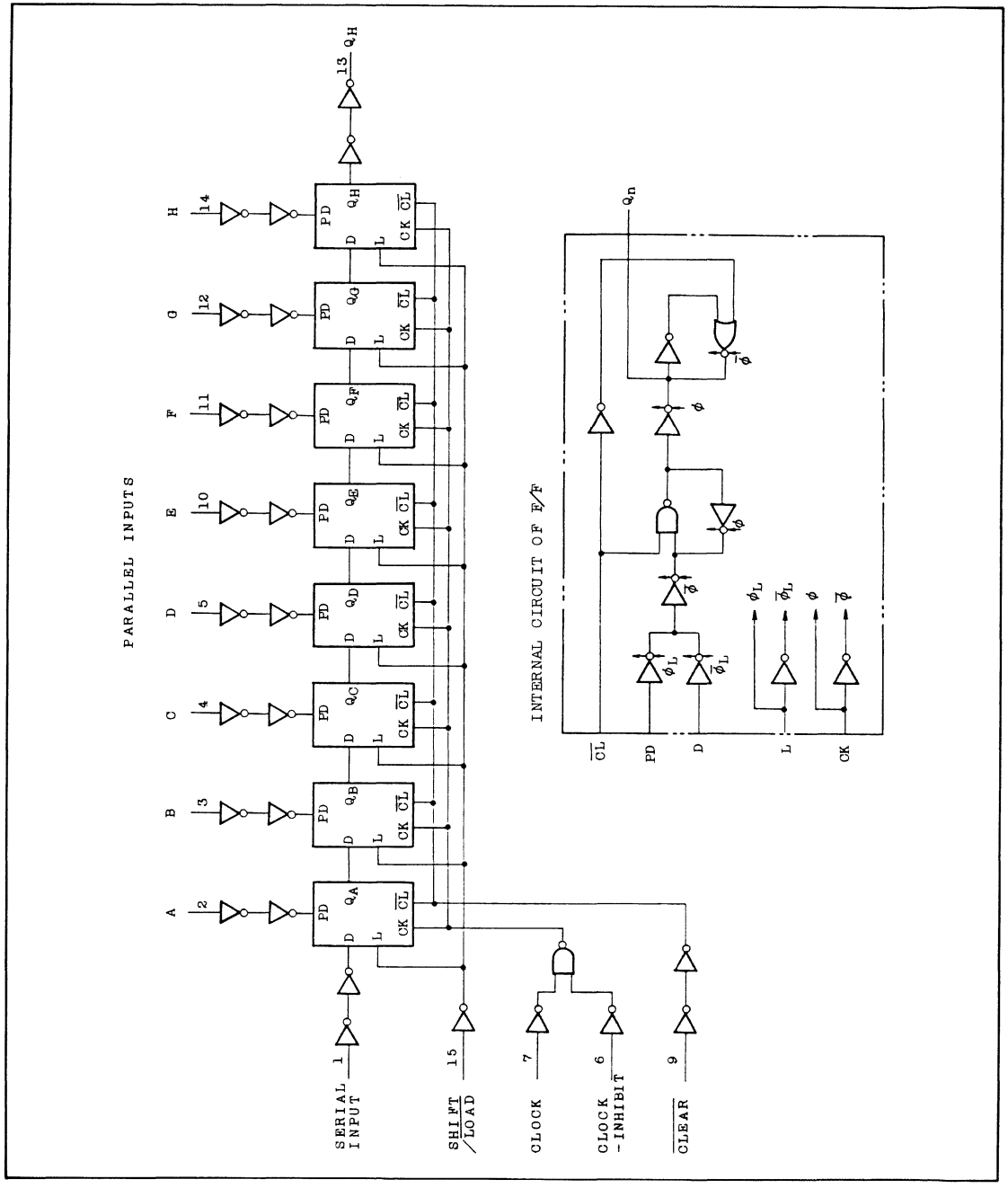
PIN ASSIGNMENT



(TOP VIEW)

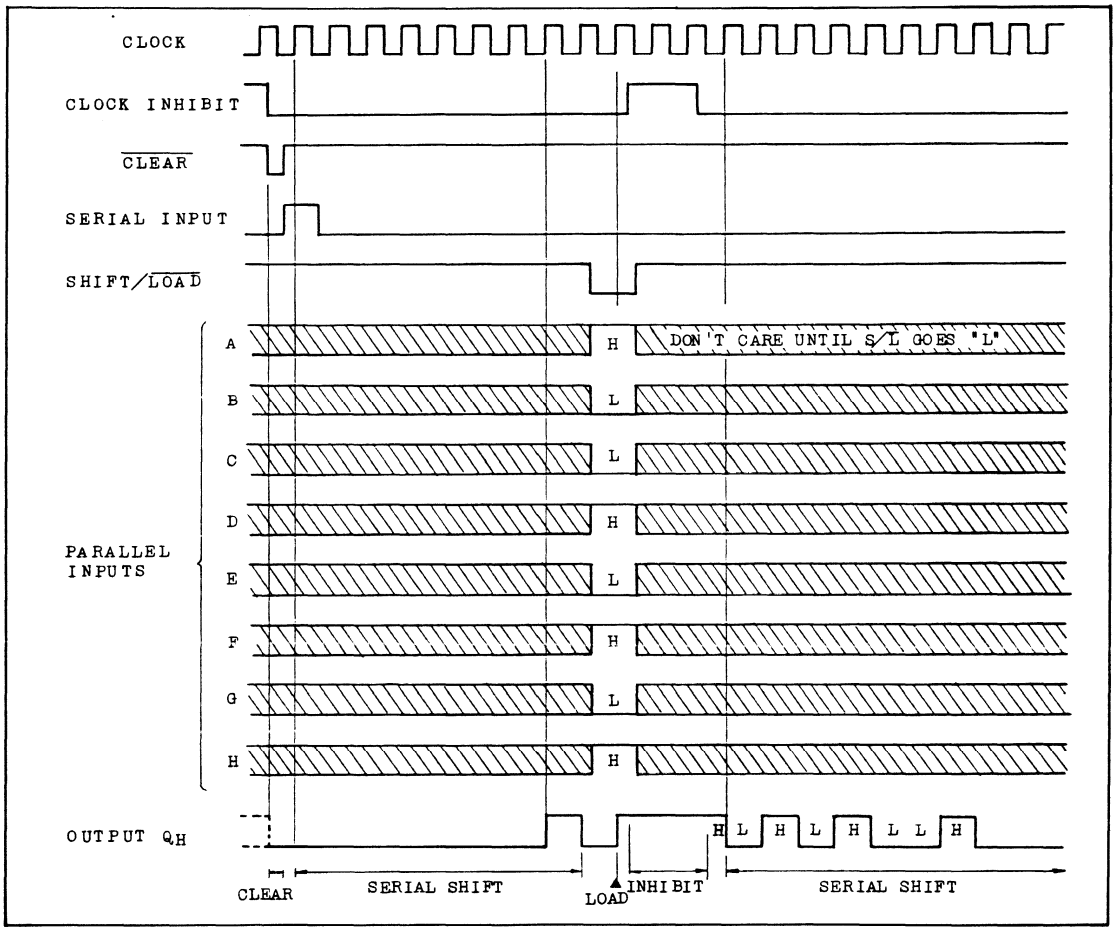
TC74HC166P/F

LOGIC DIAGRAM



TC74HC166P/F

TIMING CHART



TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
CLEAR	SHIFT/LOAD	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A ····· H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↓	X	X	No change	
H	L	L	↑	X	a ····· h	a b	h
H	H	L	↑	H	X	H QAn	QGn
H	H	L	↑	L	X	L QAn	QGn
H	X	H	X	X	X	No change	

x: Don't Care

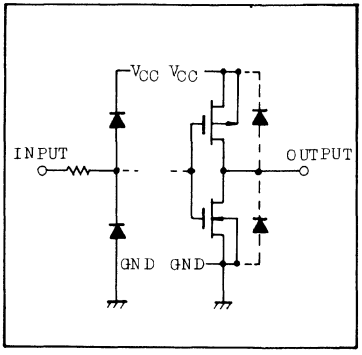
a ····· h: The level of steady state input voltage at inputs A through H respectively

TC74HC166P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

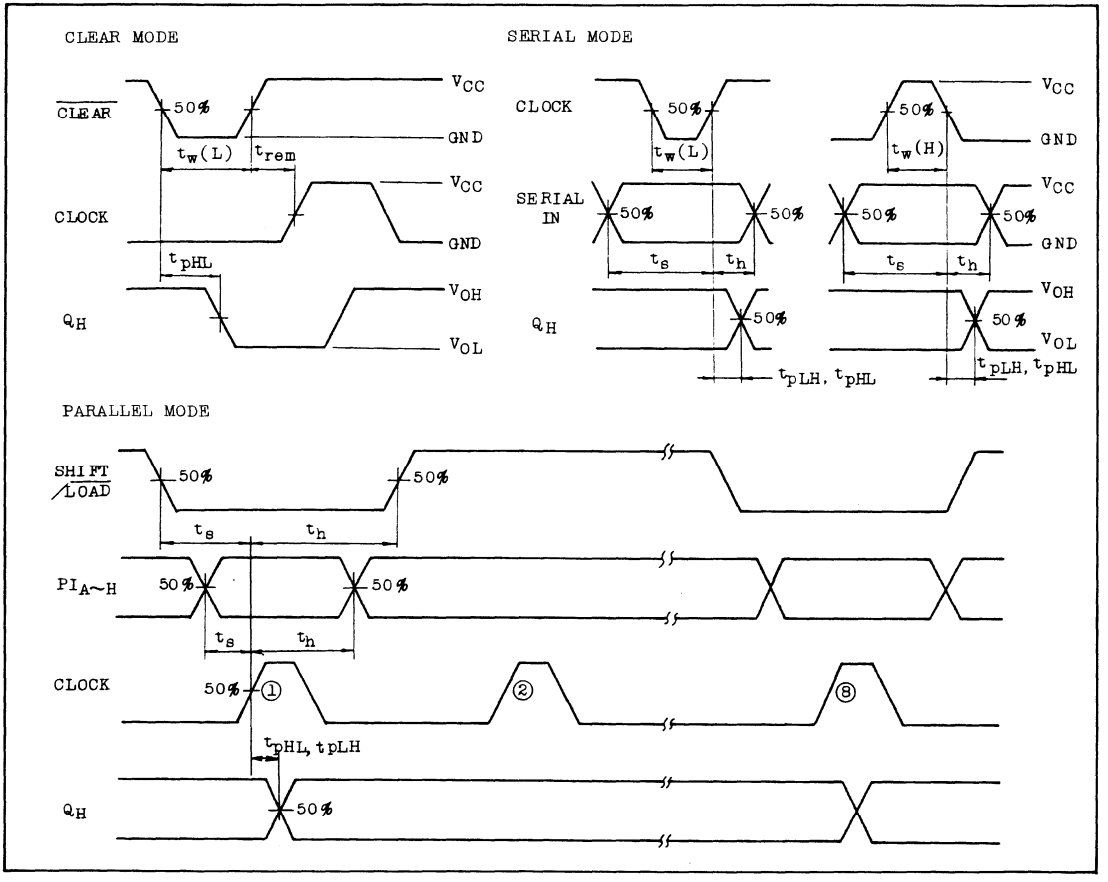
PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{TLH}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - QH)	t_{pLH}		2.0	-	80	150	-	190	
			4.5	-	20	30	-	38	
	t_{pHL}		6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{CLEAR}$ - QH)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0		0	
			6.0	-	-	0	-	0	
Minimum Set-up Time (SI, PI)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (S/$\overline{L}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (SI, PI)	t_h		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Minimum Hold Time (S/$\overline{L}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD} (1)			-	58	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

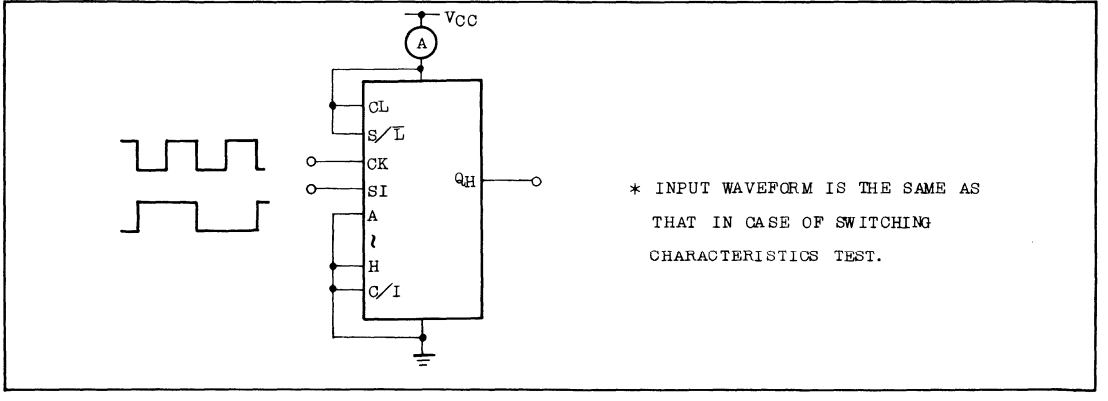
$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC166P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



ICC(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

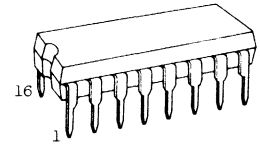
TC74HC173P/F

TC74HC173P/F QUAD D-TYPE REGISTER (3-STATE)

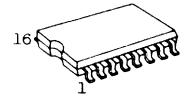
The TC74HC173 is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device is composed of four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs ($D_1 - D_4$) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low. The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, and otherwise the outputs are in a high-impedance state. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS173



DIP16(3D16A-P)



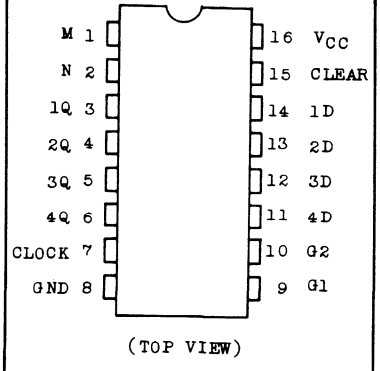
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC173P/F

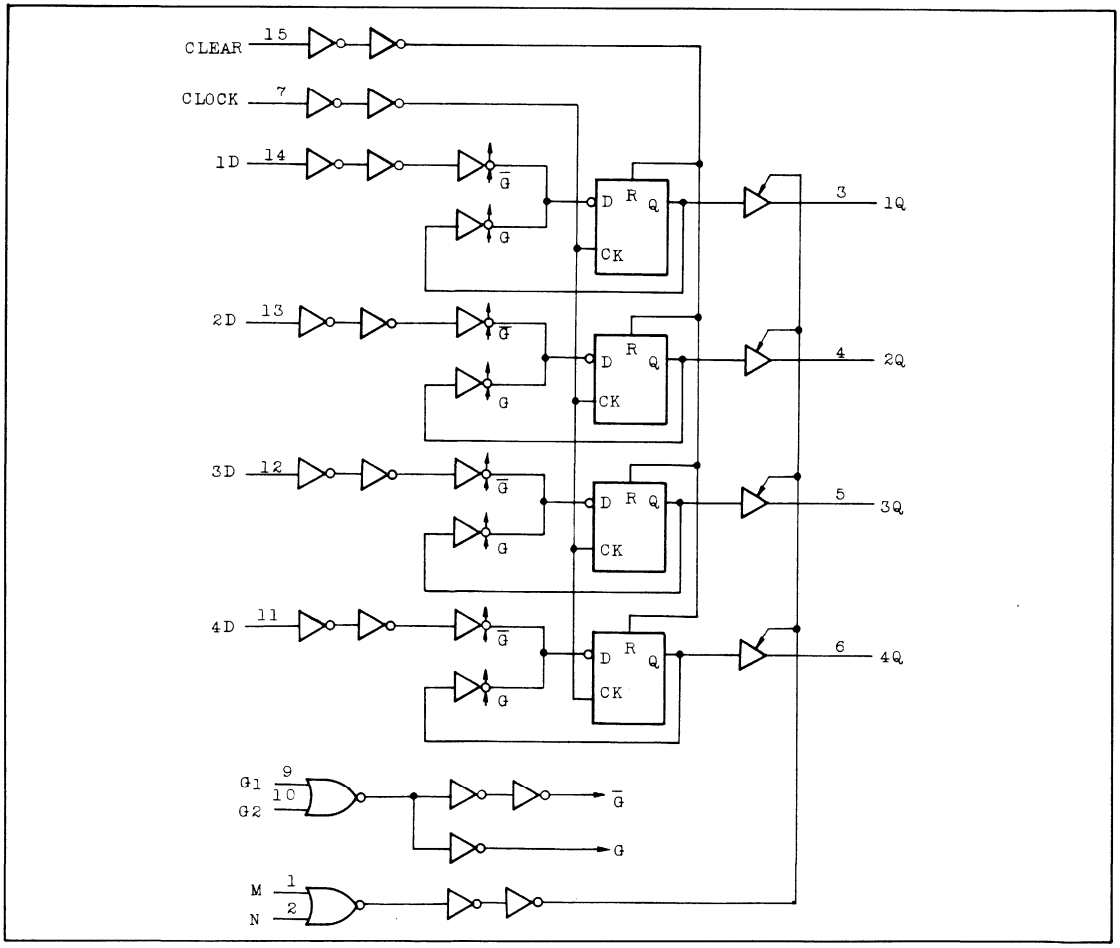
TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	Dn	OUTPUT CONTROL M	OUTPUT CONTROL N	Qn
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↓	X	X	X	L	L	Q0
L	↑	H	X	X	L	L	Q0
L	↑	X	H	X	L	L	Q0
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L

X : DON'T CARE

Z : HIGH IMPEDANCE

LOGIC DIAGRAM

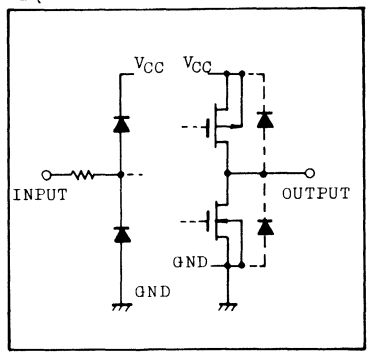


TC74HC173P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC173P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CLOCK - Q)	t_{PLH} t_{PHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (CLEAR - Q)	t_{PLH} t_{PHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time (G_1, G_2)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time (D)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (G_1, G_2, D)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

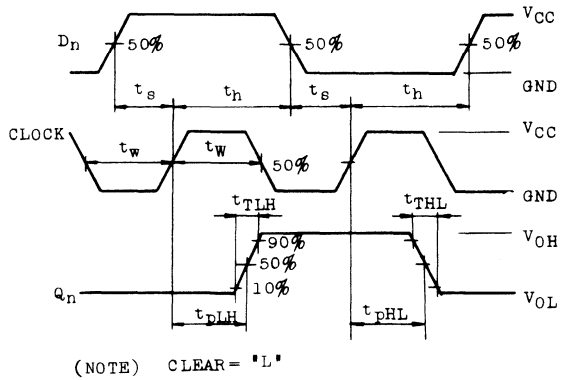
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per 1 Circuit)}$$

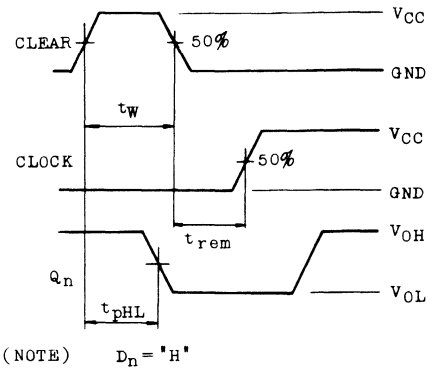
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD(total)}=14 + 16 \cdot n$$

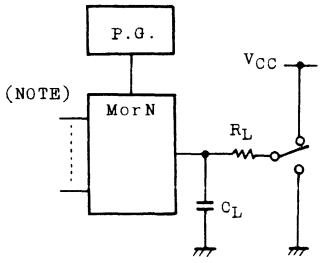
SWITCHING CHARACTERISTICS TEST WAVEFORM



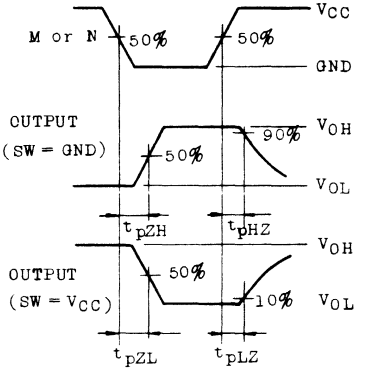
(NOTE) CLEAR = "L"



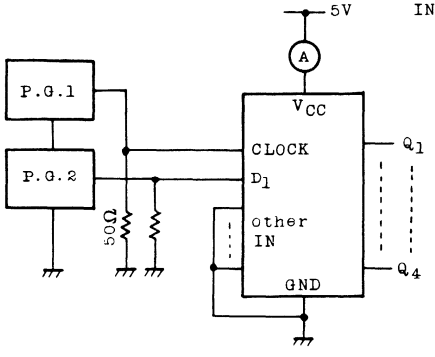
(NOTE) D_n = "H"



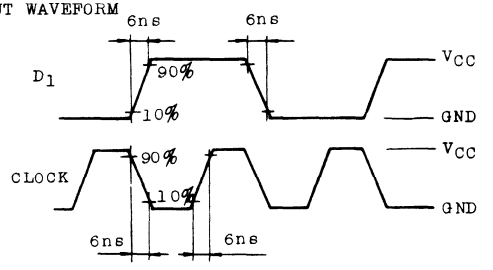
(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM



TC74HC174P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC174P/F HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74HC174 is a high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

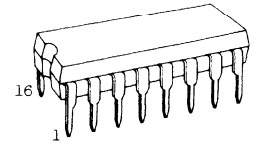
Information signals applied to D inputs are transfered to the Q output on the positive-going edge of the clock pulse.

When the $\overline{\text{CLEAR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

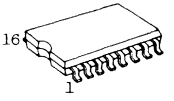
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=43MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS174

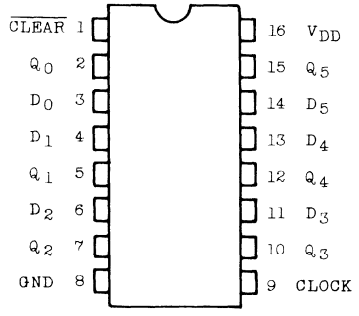


DIP16(3D16A-P)



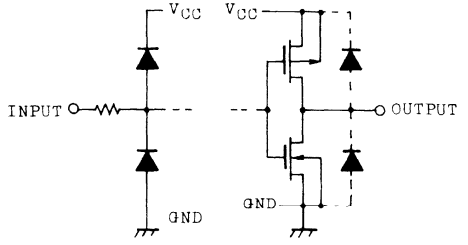
MFP16(F16GC-P)

PIN ASSIGNEMENT



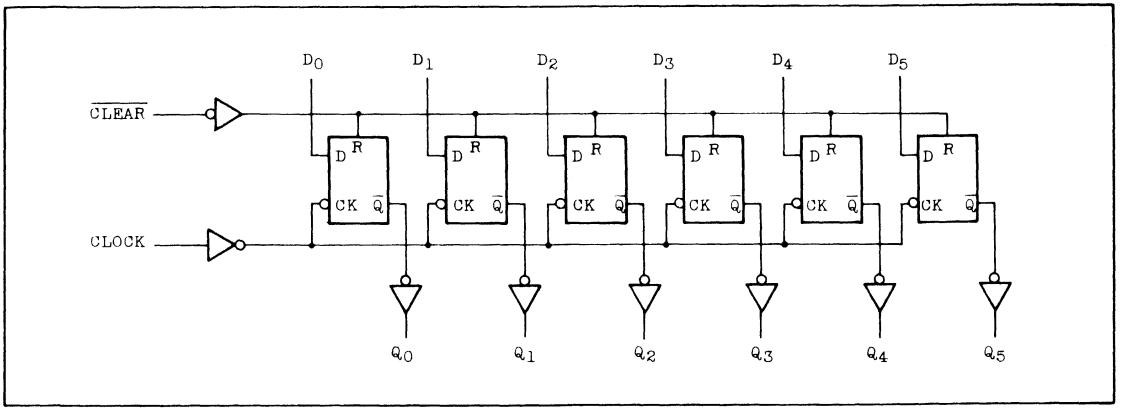
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC174P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	-
H	H	↑	H	-
H	X	↓	Q_n	No change

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

※ 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC174P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time $\overline{\text{CLEAR}}$ - Q	t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	44	-	22	-	
			6.0	32	52	-	26	-	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width $\overline{\text{CLEAR}}$	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{\text{CLEAR}}$	t_{rem}		2.0	-	15	75	-	95	
			4.5	-	4	15	-	19	
			6.0	-	3	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	53	-	-	-	

TC74HC174P/F

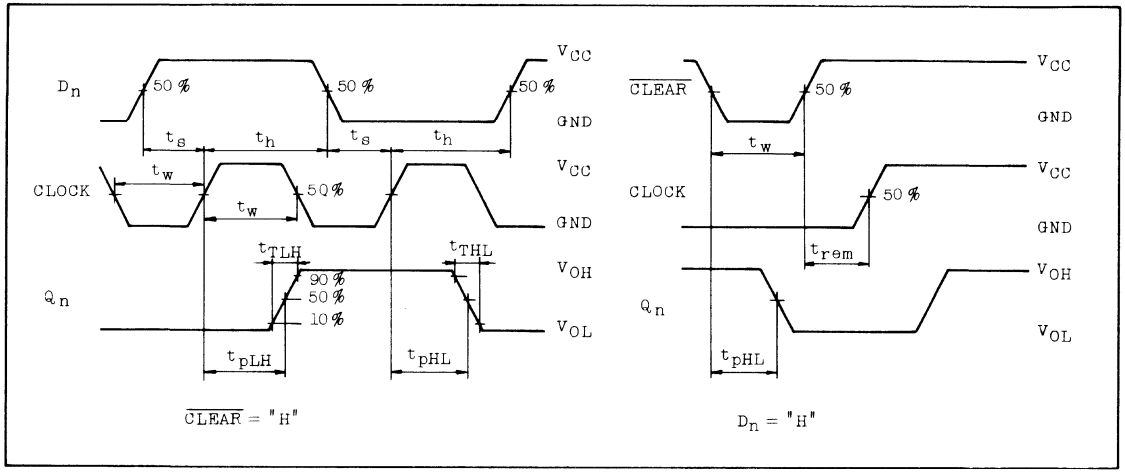
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Flip Flop)}$$

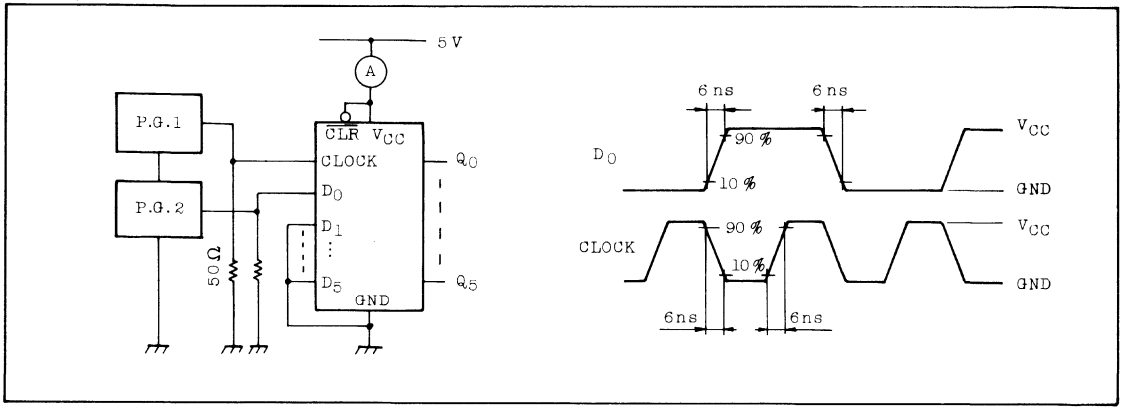
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD(total)} = 38 + 15 \cdot n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC175P/F

TC74HC175P/F QUAD D-TYPE FLIP-FLOP WITH CLEAR

The TC74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

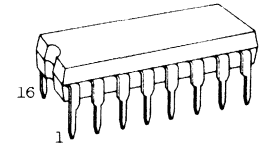
These four flip-flops are controled by a clock input (CLOCK) and a clear input (CLEAR). The infomation data applied to the D inputs (1D thru 4D) are transfered to the outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$) on the positive-going edge of the clock pulse.

Reset function is accomplished when the clear input is taken low, and all Q outputs are kept in low level regardless of other input conditions.

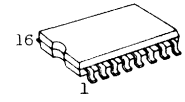
All input are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS175

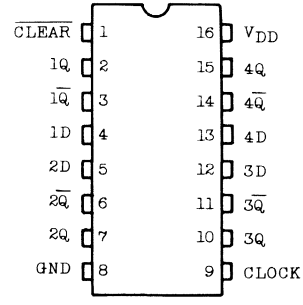


DIP16(3D16A-P)



MFP16(F16GC-P)

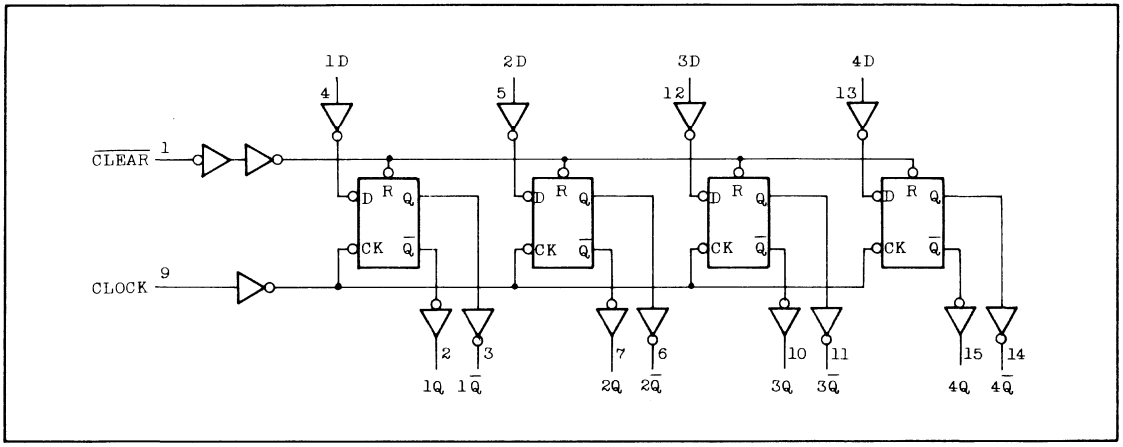
PIN ASSIGNMENT



(Top View)

TC74HC175P/F

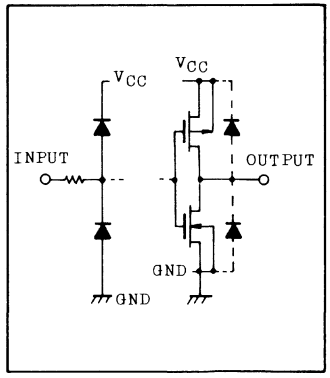
LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	Clear
H	L	↑	L	H	-
H	H	↑	H	L	-
H	X	↓	Q_n	$\overline{Q}_n$	No change
X : Don't care					

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC175P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	105	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	115	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	48	-	24	-	
			6.0	35	56	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	0	75	-	95	
			4.5	-	0	15	-	19	
			6.0	-	0	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	71	-	-	-	

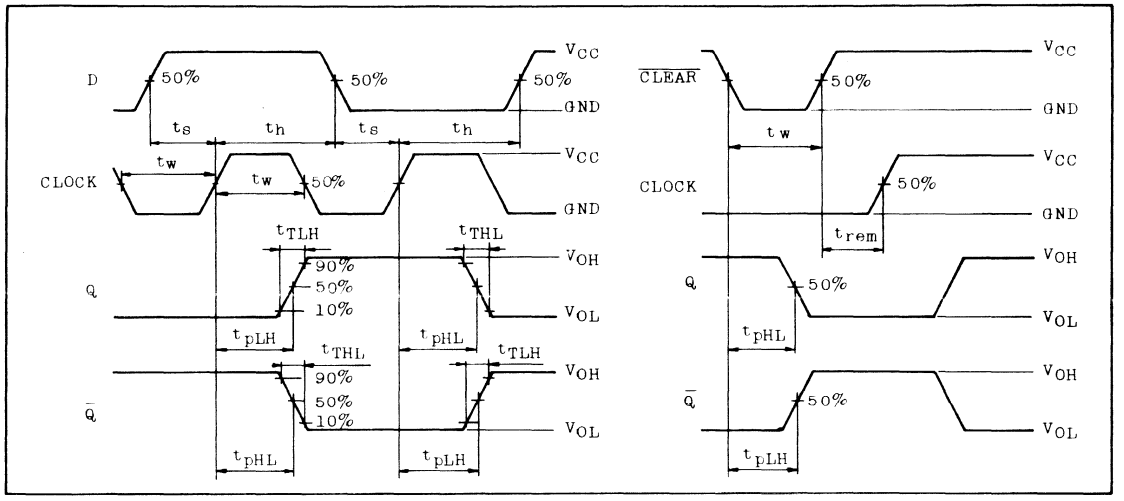
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Flip-Flop)}$$

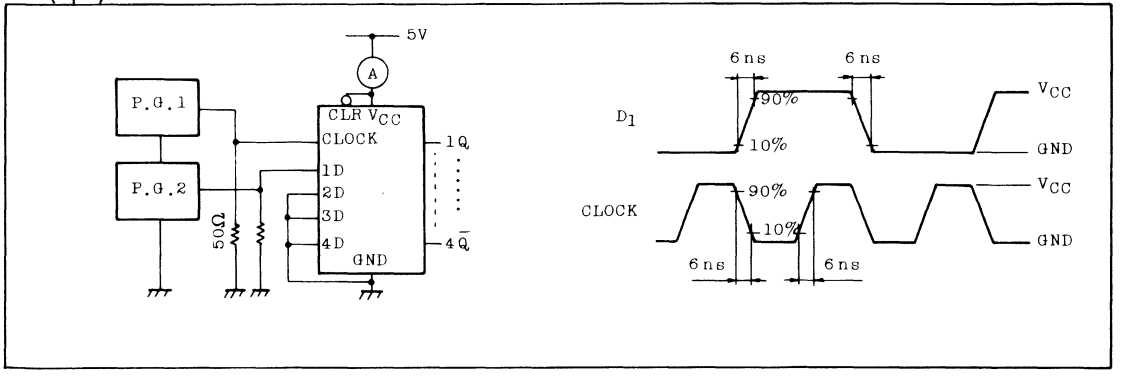
And the total C_{PD} at the time when n pcs of Flip-Flop operate can be gained by the following equation.

$$C_{PD}(\text{total}) = 43 + 28 \times n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC181P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC181P ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The TC74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT(ALU)/FUNCTION GENERATORS fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This circuit perform 16 binary arithmetic operations on two 4-bit word as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

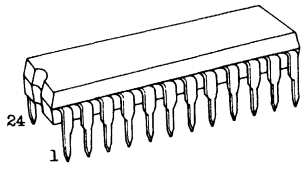
When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look ahead scheme is made available in these devices for fast, simultaneous carry generation be means of two cascade-outputs (pins 15 and 17) for the four bits in the package.

When used in conjunction with the TC74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

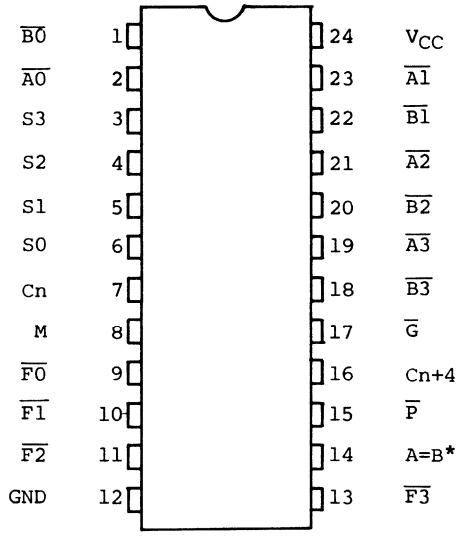
FEATURES:

- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS181



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

*: Open drain Output Structure

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A=B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

TC74HC181P

FUNCTIONAL DESCRIPTION

The HC181 will accomodate active-high or active-low data, if the pin designations are interpreted as show below.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn+4	$\overline{P}$	$\overline{G}$
Active-high data(Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{Cn}$	$\overline{Cn+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to produce A-B.

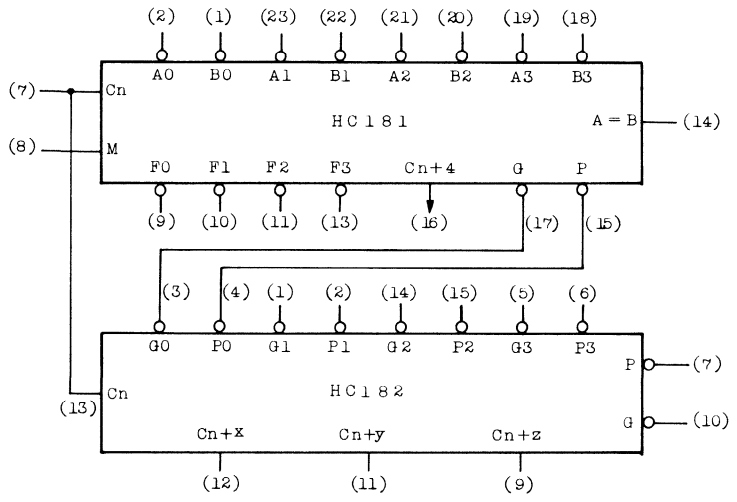
The HC181 also be utilized as a comparator. The A=B output is internally decoder from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with Cn=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output Cn+4	Active-low data (Figure 1)	Active-high data (Figure 2)
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

TC74HC181P



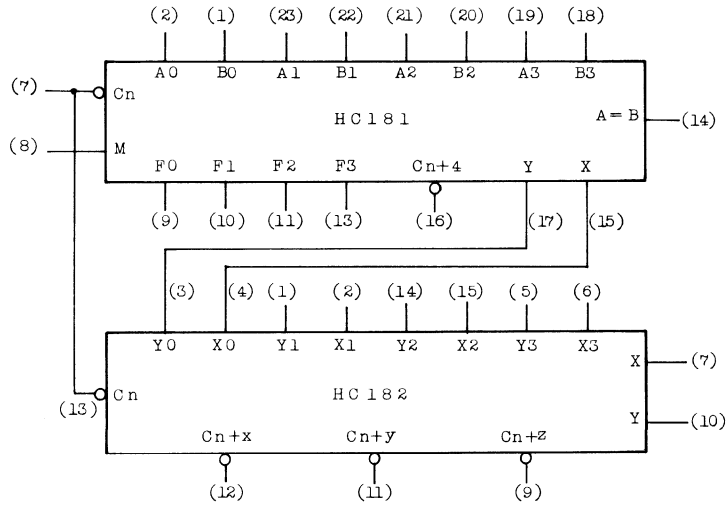
(Figure 1)

Table 1

Selection				Active Low Data		
				M=H	M=L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	$F = \bar{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \bar{A} + B$	F = $A\bar{B}$ Minus 1	F = ($A\bar{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus (A + $\bar{B}$)	F = A Plus(A + $\bar{B}$) Plus 1
L	H	L	H	$F = \bar{B}$	F = AB Puls (A + B)	F = AB Plus(A + $\bar{B}$) Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \bar{B}$	$F = A + \bar{B}$	F = (A + $\bar{B}$) Plus 1
H	L	L	L	$F = \bar{A}B$	F = A Plus (A + B)	F = A Plus(A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\bar{B}$ Plus (A + B)	F = $A\bar{B}$ Plus(A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\bar{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\bar{B}$ Plus A	F = $A\bar{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

TC74HC181P



(Figure 2)

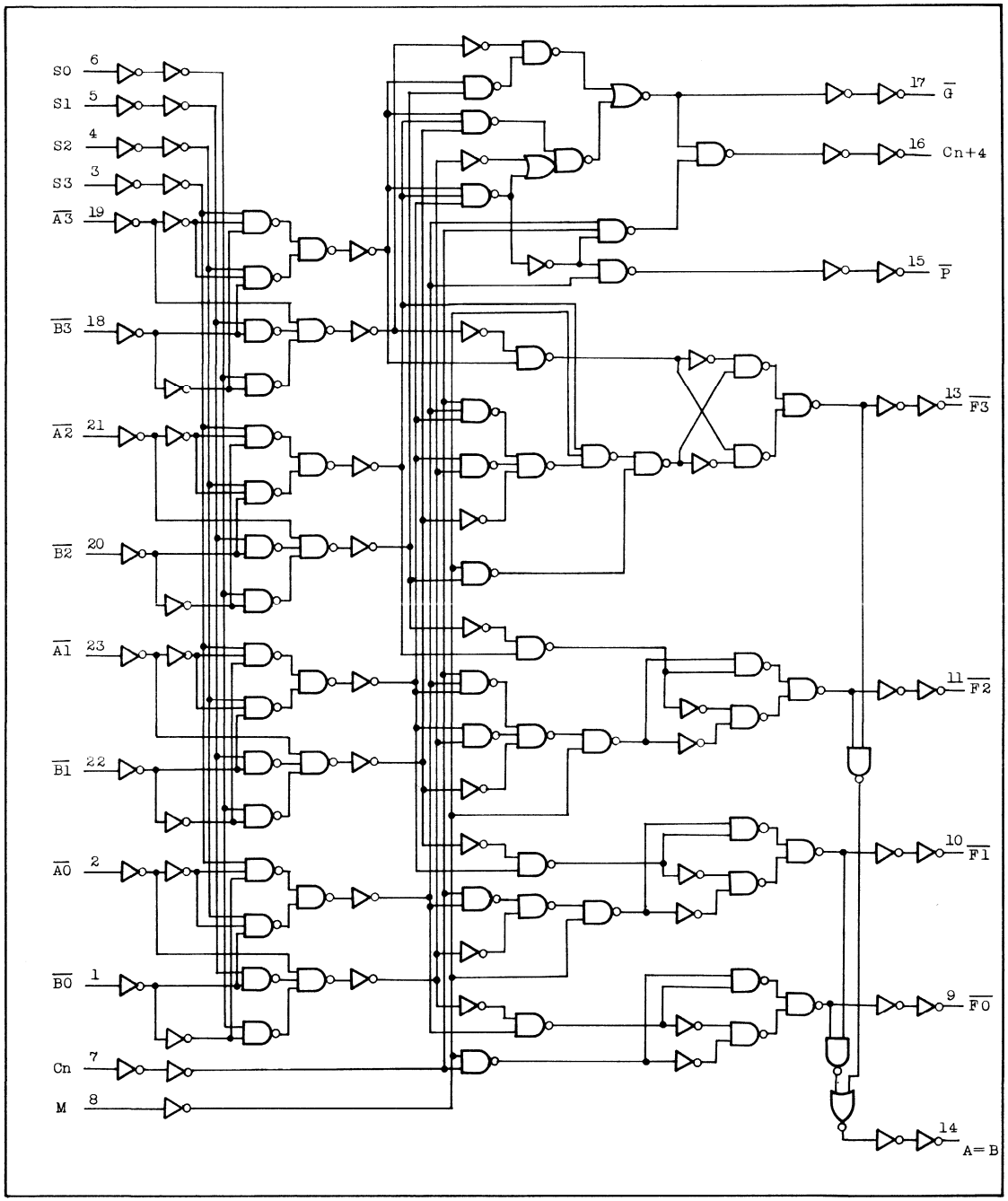
Table 2

Selection S3 S2 S1 S0	Active High Data: M=H Logic Functions	M=L: Arithmetic Operations: C_n=H (no carry)	M=L: Arithmetic Operations: C_n=L (with carry)
L L L L	$F = \overline{A}$	F = A	F = A Plus 1
L L L H	$F = \overline{A+B}$	F = A + B	F = (A + B) Plus 1
L L H L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
L L H H	F = 0	F = Minus 1(2's Compl)	F = Zero
L H L L	$F = \overline{AB}$	$F = A$ Plus $A\overline{B}$	$F = A$ Plus $A\overline{B}$ Plus 1
L H L H	$F = \overline{B}$	$F = (A + B)$ Plus $A\overline{B}$	$F = (A + B)$ Plus $A\overline{B}$ Plus 1
L H H L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L H H H	$F = A\overline{B}$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
H L L L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H L L H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	$F = (A + \overline{B})$ Plus AB	$F = (A + \overline{B})$ Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	$F = A + \overline{B}$	$F = (A + B)$ Plus A	$F = (A + B)$ Plus A Plus 1
H H H L	F = A + B	$F = (A + \overline{B})$ Plus A	$F = (A + \overline{B})$ Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

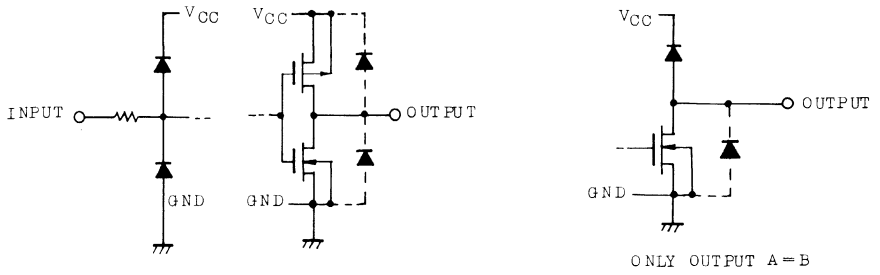
TC74HC181P

LOGIC DIAGRAM



TC74HC181P

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

TC74HC181P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Any output except A=B	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.00	0.1	-	0.1	V
				4.5	-	0.00	0.1	-	0.1	
				6.0	-	0.00	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	$V_{IN}=V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

TC74HC181P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (1)	t_{pLH}		2.0	-	68	135	-	170	
	t_{pHL}		4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time (2)	t_{pLH}		2.0	-	124	240	-	300	
	t_{pHL}		4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (3)	t_{pLH}		2.0	-	120	235	-	295	
	t_{pHL}		4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (4)	t_{pLH}		2.0	-	112	215	-	270	
	t_{pHL}		4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
Propagation Delay Time (5)	t_{pLH}		2.0	-	116	225	-	280	
	t_{pHL}		4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (6)	t_{pLH}		2.0	-	116	220	-	275	
	t_{pHL}		4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Propagation Delay Time (7)	t_{pLH}		2.0	-	108	210	-	265	
	t_{pHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (8)	t_{pLH}		2.0	-	108	210	-	265	
	t_{pHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (9)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (10)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (11)	t_{pLH}		2.0	-	112	215	-	270	
	t_{pHL}		4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
3-State Output Enable Time (12)	t_{pZL}	R_L=1kΩ	2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
3-State Output Disable Time (12)	t_{pLZ}	R_L=1kΩ	2.0	-	140	260	-	325	
			4.5	-	35	52	-	65	
			6.0	-	30	44	-	55	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	216	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

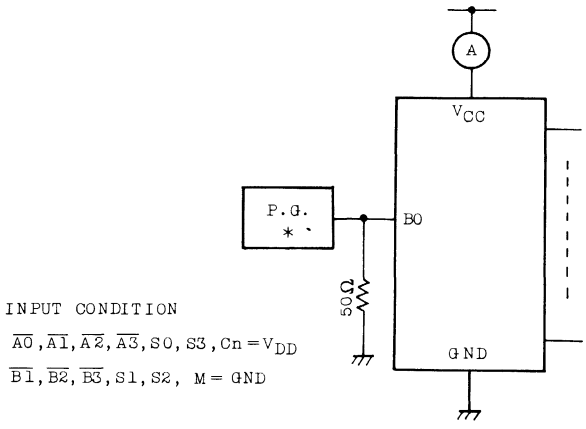
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

PROPAGATION DELAY TIME TEST CONDITIONS

TEST NO.	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M=GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=VCC, S1=S2=GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A=B	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)

TC74HC181P

$I_{CC(opr.)}$ TEST CIRCUIT



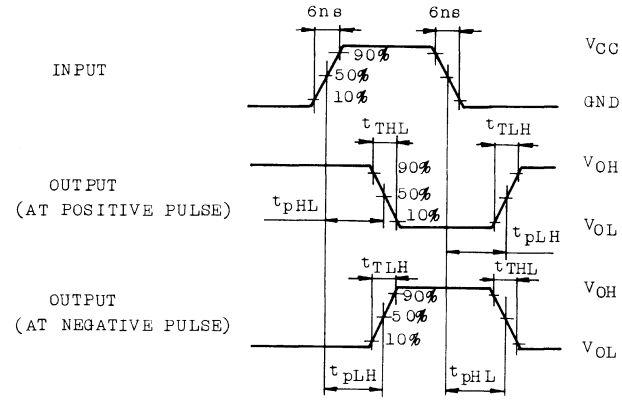
INPUT CONDITION

$\overline{A0}, \overline{A1}, \overline{A2}, \overline{A3}, S0, S3, Cn = V_{DD}$

$\overline{B1}, \overline{B2}, \overline{B3}, S1, S2, M = GND$

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC182P/F

TC74HC182P/F LOOK AHEAD CARRY LOGIC

The TC74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated with silicon gate C^2MOS technology.

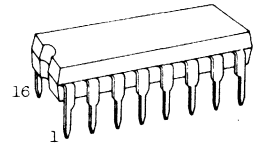
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

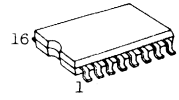
When used in conjunction with the HC181 arithmetic logic unit, these generators provide hihg-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate(P) and carry generate(G) are in negated form; therefore, the carry functions (inputs, output, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-1)

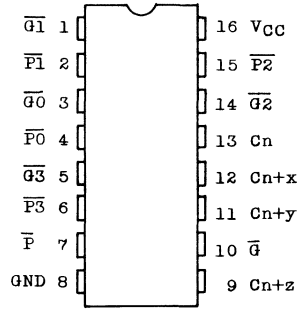


MFP16(F16GC-P)

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS182

PIN ASSIGNMENT



(TOP VIEW)

TC74HC182P/F

TRUTH TABLE

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
All other combinations			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

X: Don't care

$Cn+x = G0 + P0Cn$

$Cn+y = G1 + P1G0 + P1P0Cn$

$Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$

$\overline{G} = \overline{G3+P3G2+P3P2G1+P3P2P1G0}$

$\overline{P} = \overline{P3P2P1P0}$

or

$\overline{Cn+x} = \overline{Y0(X0+Cn)}$

$\overline{Cn+y} = \overline{Y1[X1+Y0(X0+Cn)]}$

$\overline{Cn+z} = \overline{Y2\{X2+Y1[X1+Y0(X0+Cn)]\}}$

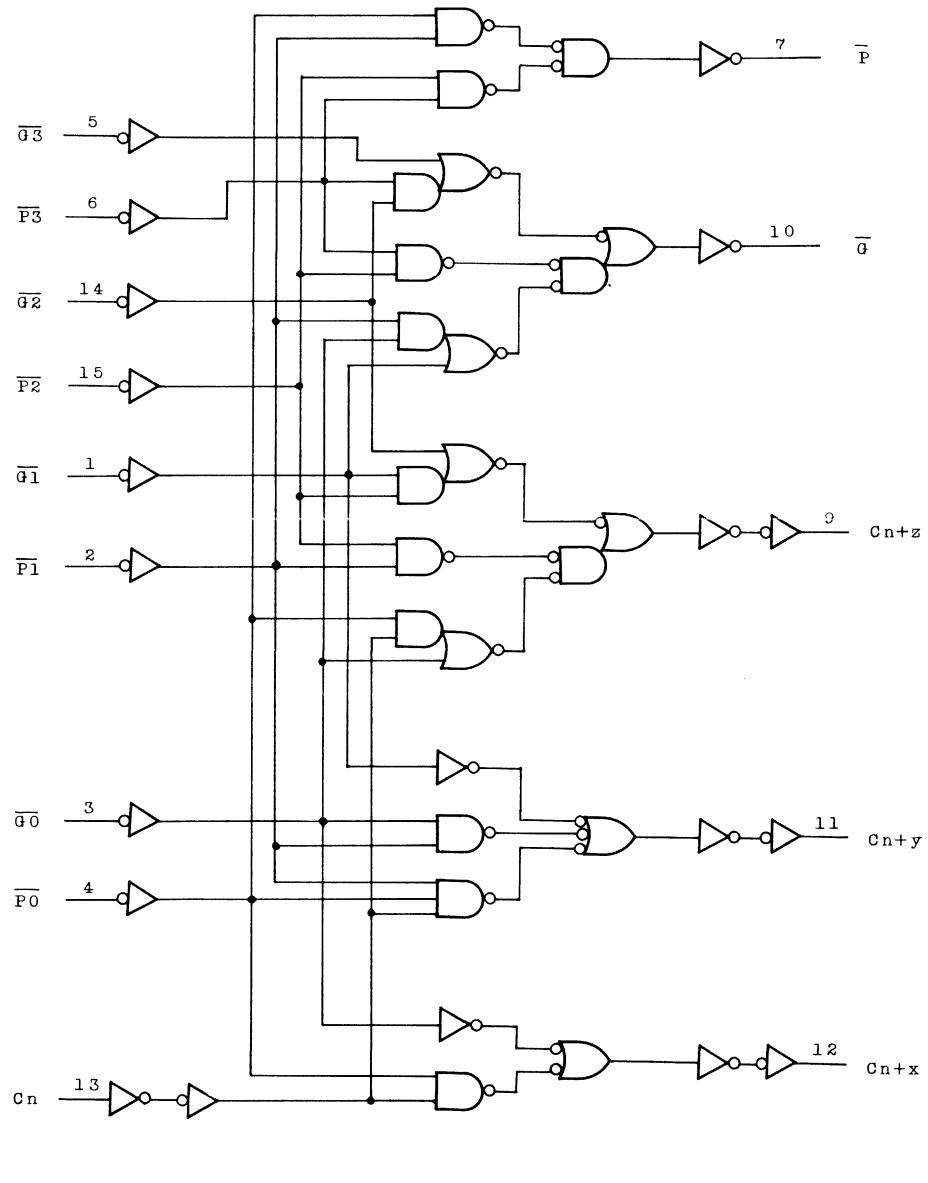
$Y = Y3(X3+Y2)(X3+X2+Y1)(X3+X2+X1+Y0)$

$X = X3+X2+X1+X0$

Pin Designation

Active "L"	Active "H"	Pin No.	Function
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	G0, G1, G2, G3	3, 1, 14, 5	Carry Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	P0, P1, P2, P3	4, 2, 15, 6	Carry Propagate Inputs
Cn	$\overline{Cn}$	13	Carry Input
Cn+z, Cn+y Cn+z	$\overline{Cn}$+x, $\overline{Cn}$+y $\overline{Cn}$+z	12, 11, 9	Carry Outputs
$\overline{G}$	Y	10	Carry Generate Output
$\overline{P}$	X	7	Carry Propagate Output
VCC		16	Supply Voltage
GND		8	Ground

LOGIC DIAGRAM



TC74HC182P/F

ABSOLUTE MAXIMUM RATINGS

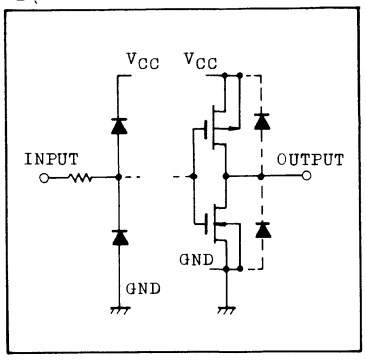
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC182P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

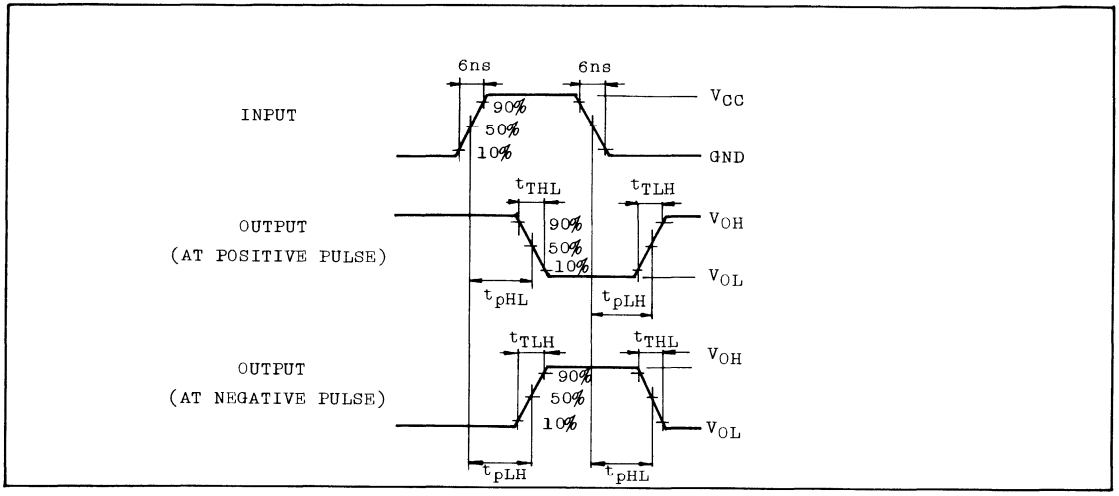
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$ - Cn+x, Cn+y; $\overline{P0},\overline{P1},\overline{P2}$ - Cn+z)	t_{pLH}		2.0	-	72	145	-	180	
	t_{pHL}		4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$ - $\overline{G}$; $\overline{P1},\overline{P2},\overline{P3}$ - $\overline{G}$)	t_{pLH}		2.0	-	84	165	-	205	
	t_{pHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)	t_{pLH}		2.0	-	80	155	-	195	
	t_{pHL}		4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time (Cn - Cn+x, Cn+y, Cn+z)	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	88	-	-	-	pF

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

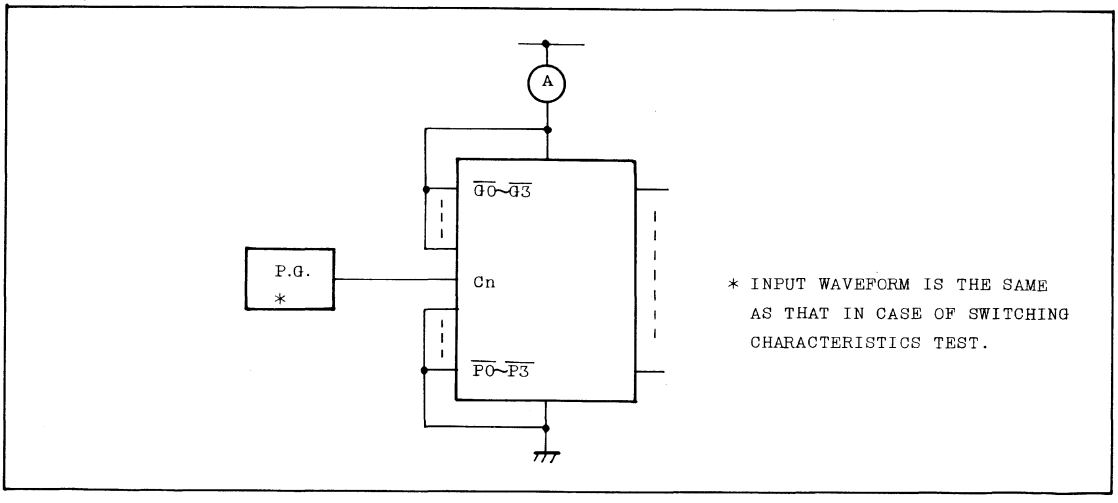
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC182P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



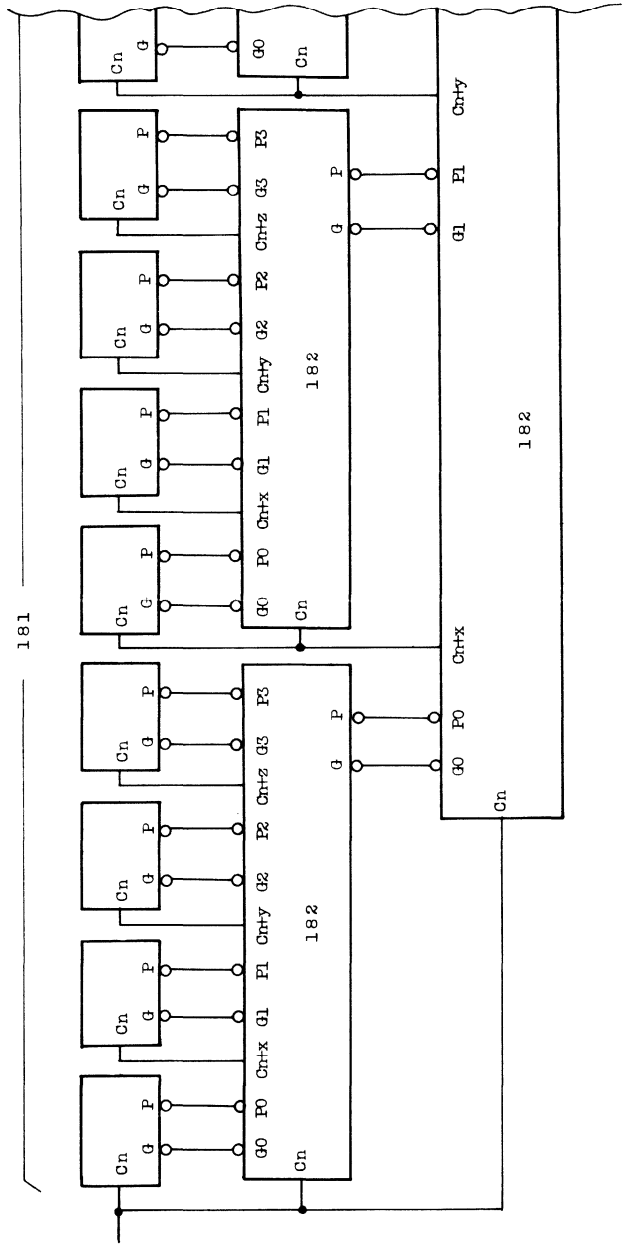
$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC182P/F

TYPICAL APPLICATION



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

TC74HC190P/F
TC74HC191P/F

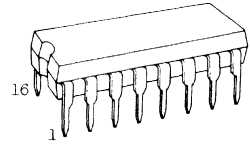
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC190P/F BCD UP/DOWN COUNTER
TC74HC191P/F 4-BIT BINARY UP/DOWN COUNTER

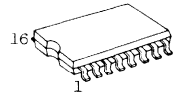
The TC74HC190 and TC74HC191 are high speed CMOS 4-BIT UP/DOWN COUNTERS fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC190 is BCD up/down counter and the TC74HC191 is 4-bit binary up/down counter.
These devices have asynchronous inputs LOAD ($\overline{LOAD}$). $\overline{LOAD}$ is active low and Load the load data.
The direction of the count is determined by the level of the DOWN/$\overline{UP}$ input. When low, the counter counts up and when high, it counts down. These counter change on the positive transition of the clock input.
Enable input ($\overline{ENABLE}$) and two CARRY output ($\overline{RIPPLE\ CLOCK\ OUT}$, MAX/MIN) are provided to enable easy cascading of counters, which facilitates easy implementation of N-bit counters without using external gate.
All inputs are equipped with protection circuits against static discahrge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- High Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS190/191



DIP16(3D16A-P)



MFP16(F160C-P)

TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	Preset Data
H	L	L	↑	Up Count				Up count
H	L	H	↑	Down Count				Down Count
H	H	X	↑	No Change				No Count
H	X	X	↓	No Change				No Count

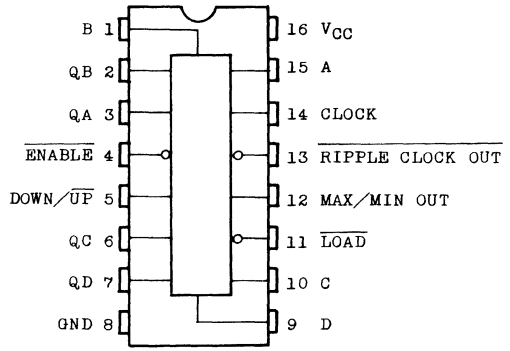
Note X: Don't care

a ∿ d: The level of steady state inputs at inputs A through D respectively.

TC74HC190P/F
TC74HC191P/F

PIN ASSIGMENT

TC74HC190/191



ABSOLUTE MAXIMUM RATINGS

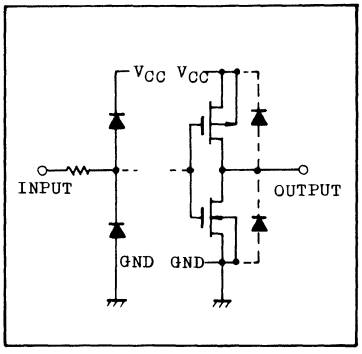
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

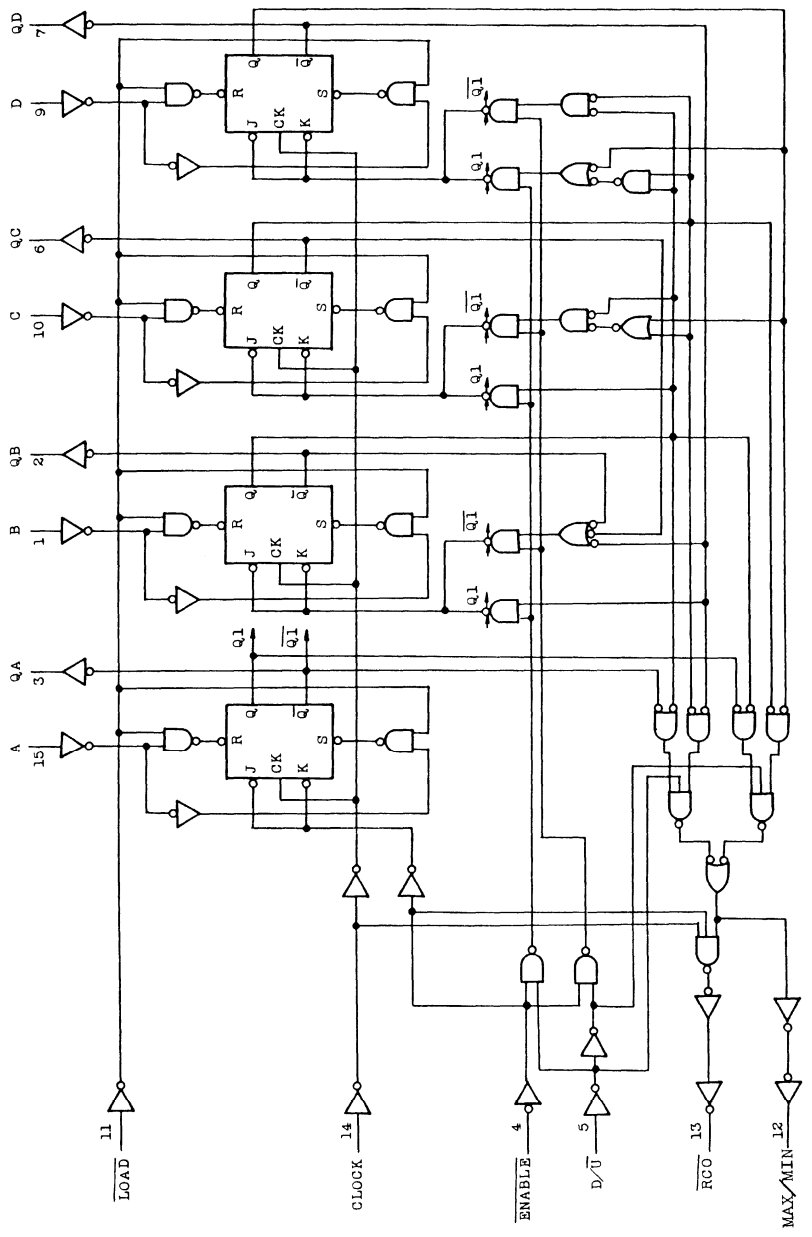
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC190P/F
TC74HC191P/F

LOGIC DIAGRAM - 1

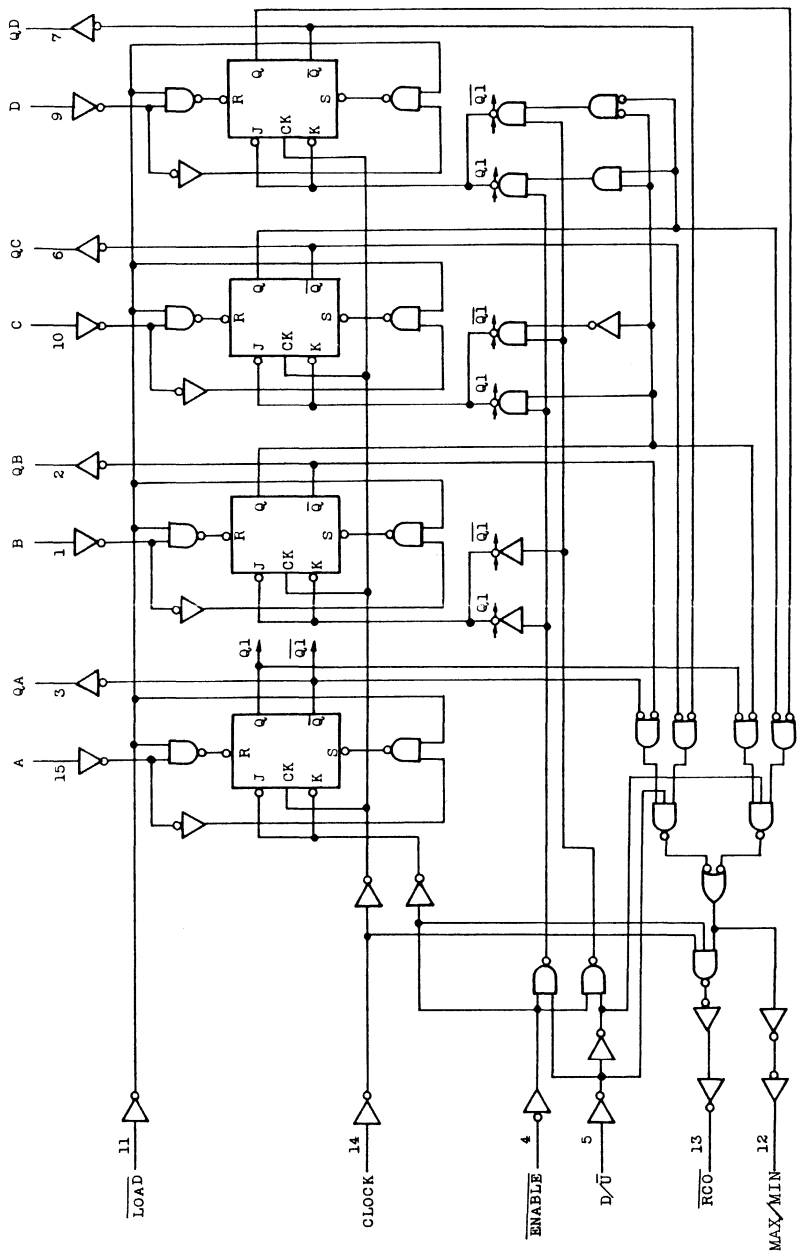
TC74HC190



TC74HC190P/F
TC74HC191P/F

LOGIC DIAGRAM - 2

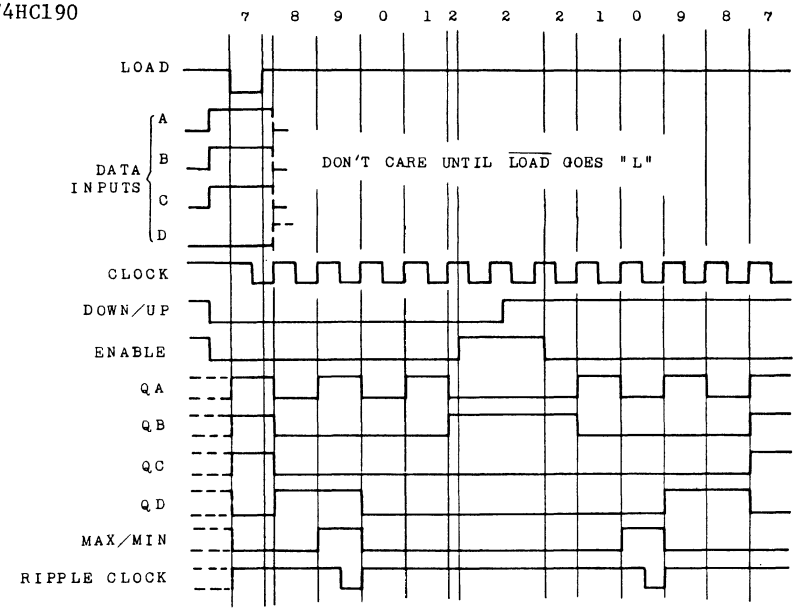
TC74HC191



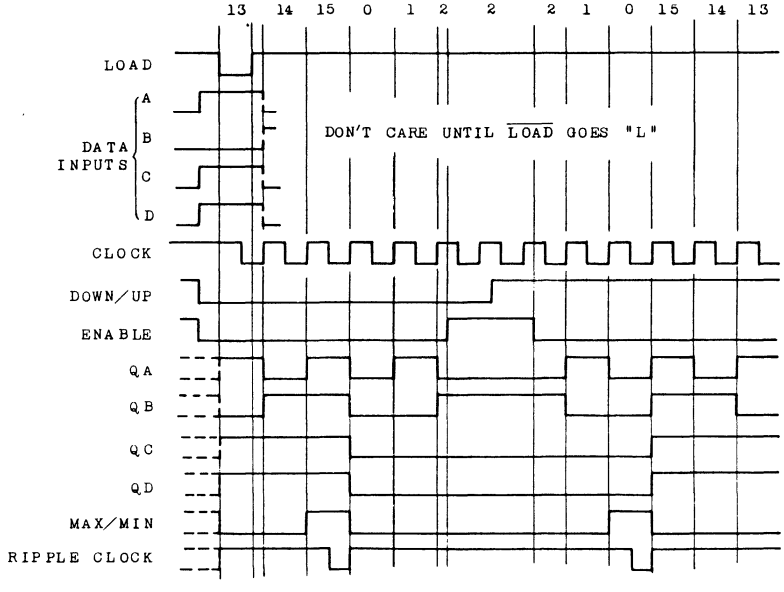
TC74HC190P/F
TC74HC191P/F

TIMING CHART

TC74HC190



TC74HC191



TC74HC190P/F
TC74HC191P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagrtion Dealy Time (CLOCK - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	

TC74HC190P/F
TC74HC191P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{pLH} t_{pHL}		2.0	-	104	205	-	255	ns
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Propagation Dalay Time (DATA -Q)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time ($\overline{ENABLE}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (D/$\overline{U}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (D/$\overline{U}$ - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	25	42	-	20	-	
			6.0	29	49	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	45	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Set-up Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_s		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	

AC ELECTRICAL CHARACTERISTICS (Continued)

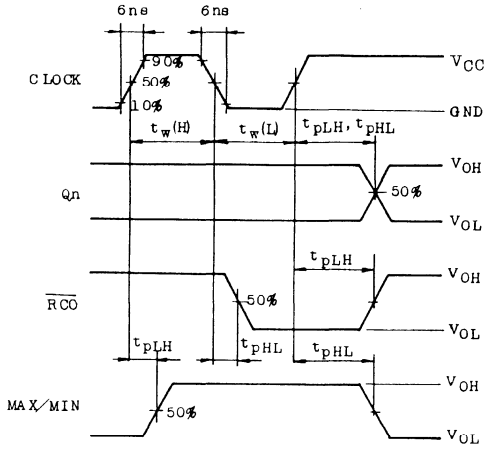
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	5	-	5	ns
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}				5	10		10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	124	-	-	-	

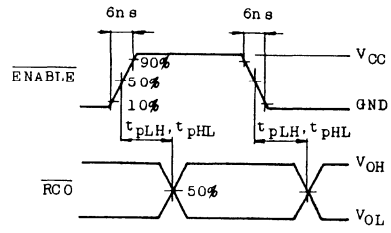
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

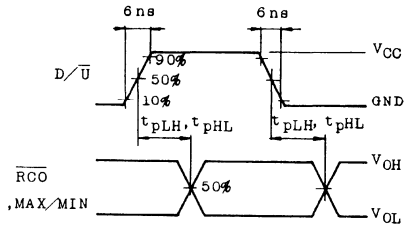
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

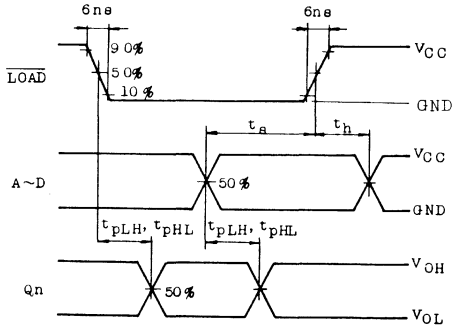
TC74HC190P/F
TC74HC191P/F

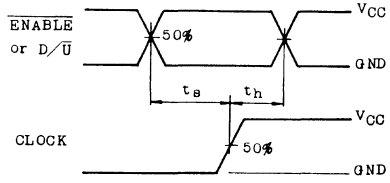
SWITCHING CHARACTERISTICS TEST WAVEFORM

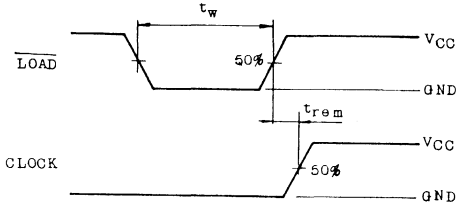




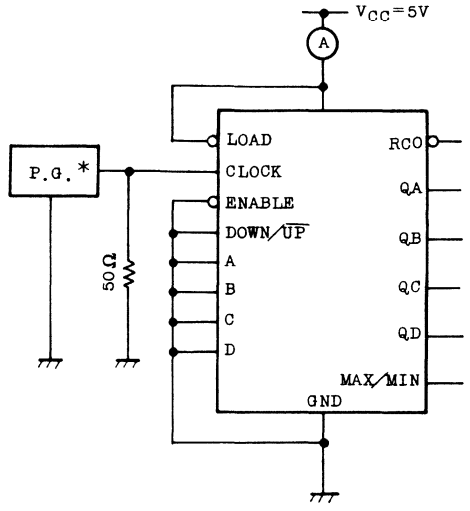








I_{CC}(Opr.) TEST WAVEFORM



* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC192P/F
TC74HC193P/F

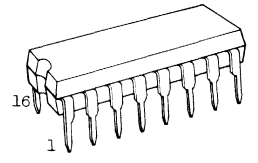
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC192P/F SYNCHRONOUS UP/DOWN DECADE COUNTER
TC74HC193P/F SYNCHRONOUS UP/DOWN BINARY COUNTER

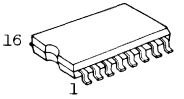
The TC74HC192 and TC74HC193 are high speed CMOS SYNCRONOUS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C²MOS technology. They achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipaiton. These counters have a clear input(CLEAR), a load input($\overline{LOAD}$), load data inputs(A - D), two clock inputs(COUNT UP/COUNT DOWN), four count data outputs(Q_A - Q_D) and carry and borrow outputs. CLEAR is active high and forces Q_A thru Q_D outputs low independently of the other inputs. $\overline{LOAD}$ is active low and load the load data when CLEAR input is held low. COUNT UP input pulse and COUNT DOWN input pulse independently bring a up-counting or down at the positive going transition of each clock pulse. CARRY and BORROW outputs are provided in order to make a cascade connection without external circuitry. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=32MHZ(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS192/193



DIP16(3D16A-P)



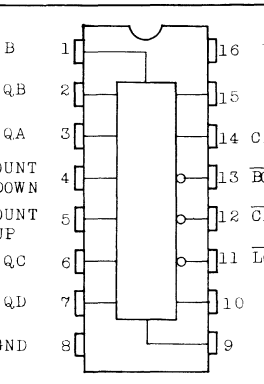
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

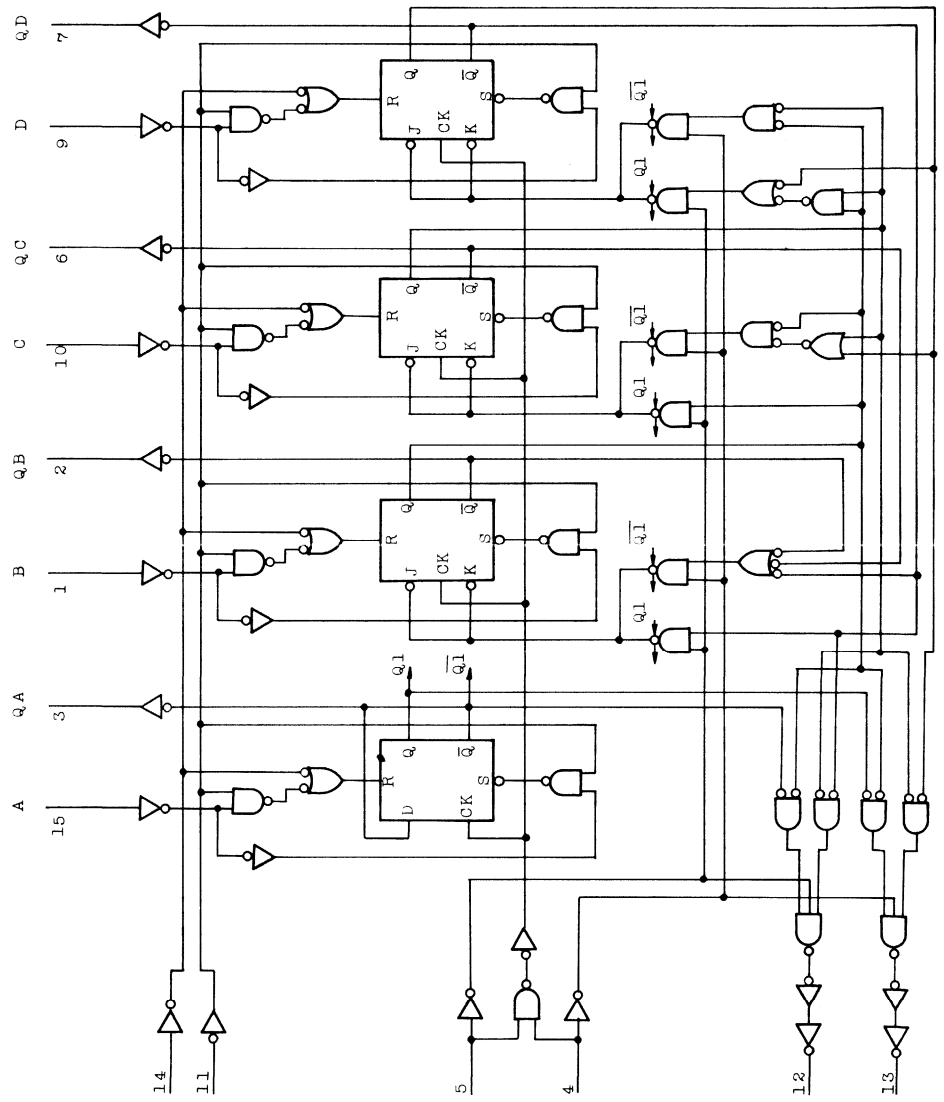


(TOP VIEW)

TC74HC192P/F
TC74HC193P/F

CIRCUIT DIAGRAM

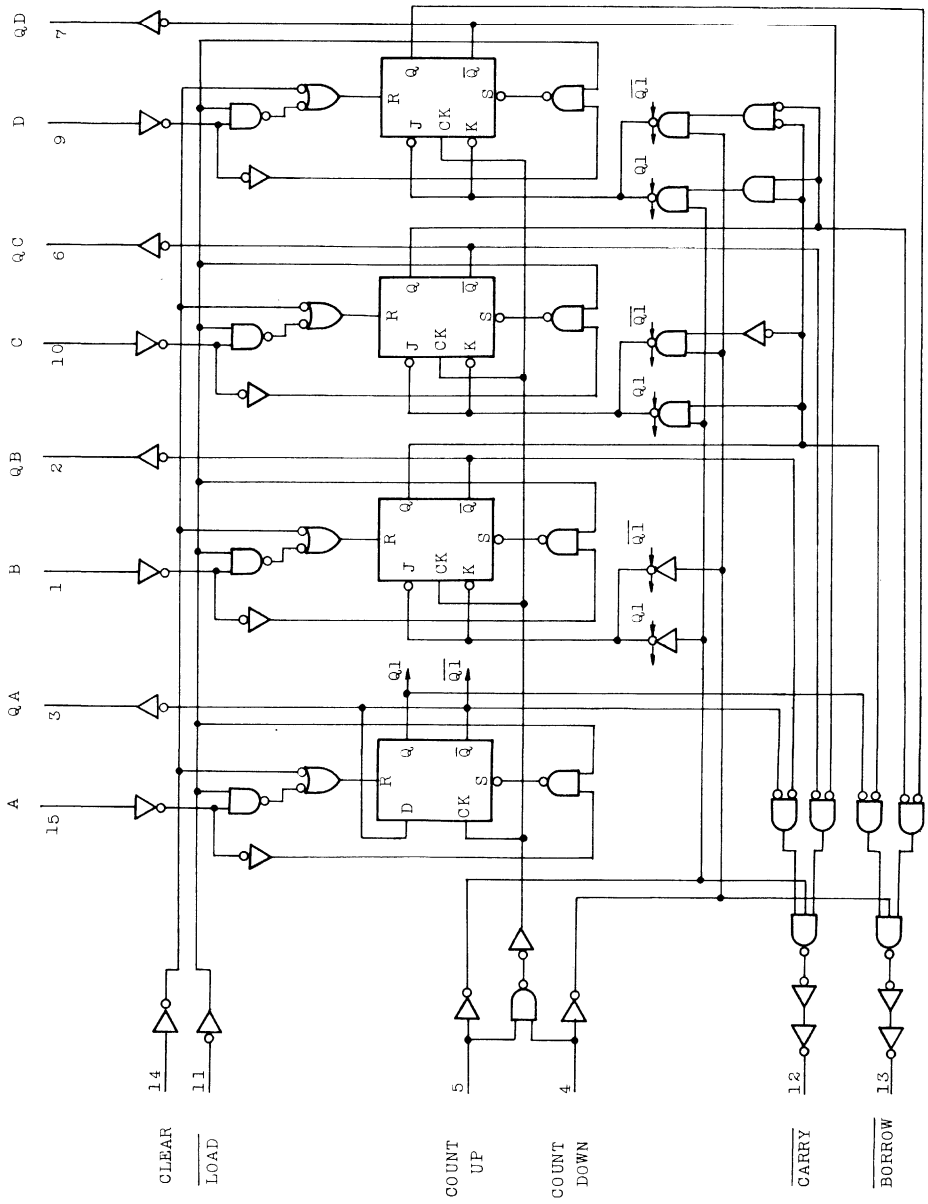
TC74HC192



TC74HC192P/F
TC74HC193P/F

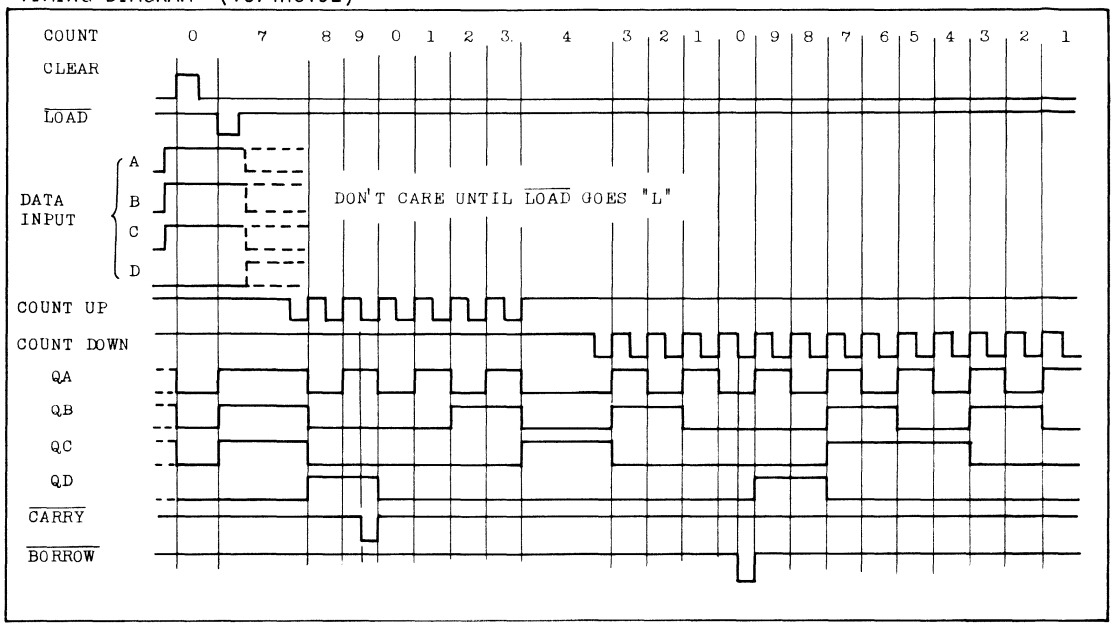
CIRCUIT DIAGRAM

TC74HC193

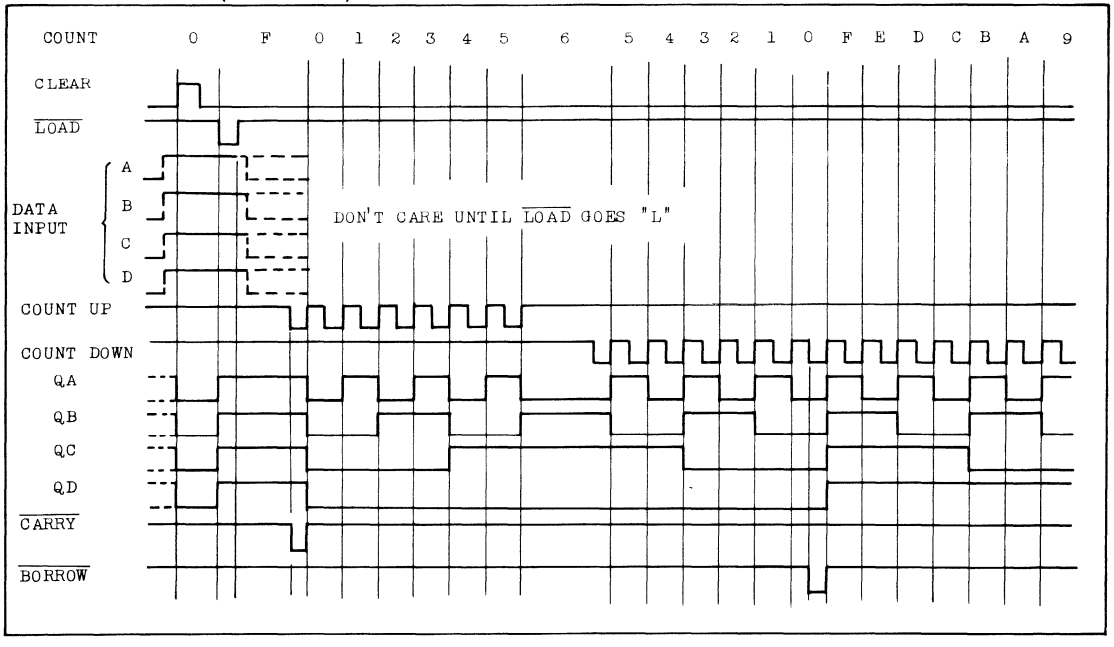


TC74HC192P/F
TC74HC193P/F

TIMING DIAGRAM (TC74HC192)



TIMING DIAGRAM (TC74HC193)



TC74HC192P/F
TC74HC193P/F

TRUTH TABLE

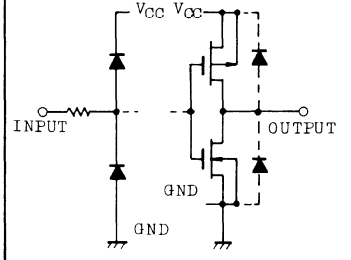
COUNT UP	COUNT DOWN	$\overline{\text{LOAD}}$	CLEAR	FUNCTION
⎍	H	H	L	COUNT UP
⎍	H	H	L	NO COUNT
H	⎍	H	L	COUNT DOWN
H	⎍	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (UP, DOWN - Q)	t_{PLH}		2.0	-	96	190	-	240	
	t_{PHL}		4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Propagation Delay Time (UP - $\overline{CARRY}$)	t_{PLH}		2.0	-	76	140	-	175	
	t_{PHL}		4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time (DOWN - $\overline{BORROW}$)	t_{PLH}		2.0	-	76	140	-	175	
	t_{PHL}		4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{PLH}		2.0	-	128	250	-	315	
	t_{PHL}		4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{CARRY}$)	t_{PLH}		2.0	-	160	310	-	390	
	t_{PHL}		4.5	-	40	62	-	78	
			6.0	-	34	53	-	66	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{BORROW}$)	t_{PLH}		2.0	-	144	280	-	350	
	t_{PHL}		4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	

TC74HC192P/F
TC74HC193P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (JAM IN - Q)	t_{PLH} t_{PHL}		2.0	-	116	230	-	290	ns
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Propagation Delay Time (JAM IN - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	172	330	-	415	
			4.5	-	43	66	-	83	
			6.0	-	37	56	-	71	
Propagation Delay Time (JAM IN - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	144	265	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (CLEAR - Q)	t_{PHL}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (CLEAR - $\overline{CARRY}$)	t_{PLH}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CLEAR - $\overline{BORROW}$)	t_{PHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Frequency (CLOCK)	f_{MAX}		2.0	3	7	-	2.5	-	MHz
			4.5	16	29	-	13	-	
			6.0	19	34	-	15	-	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	-	70	150	-	190	ns
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	32	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(H)}$		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$		2.0	-	45	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	

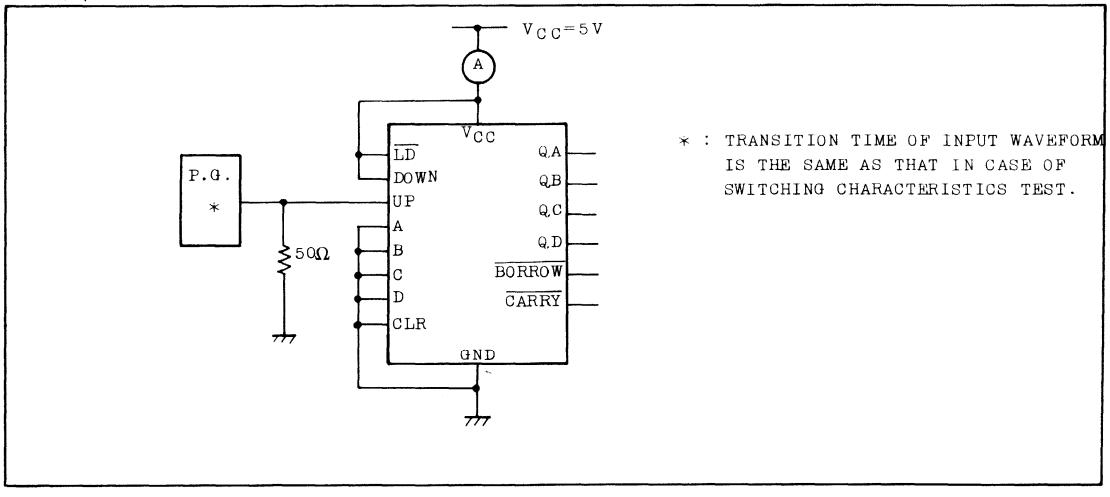
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_s		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	66	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{DD(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

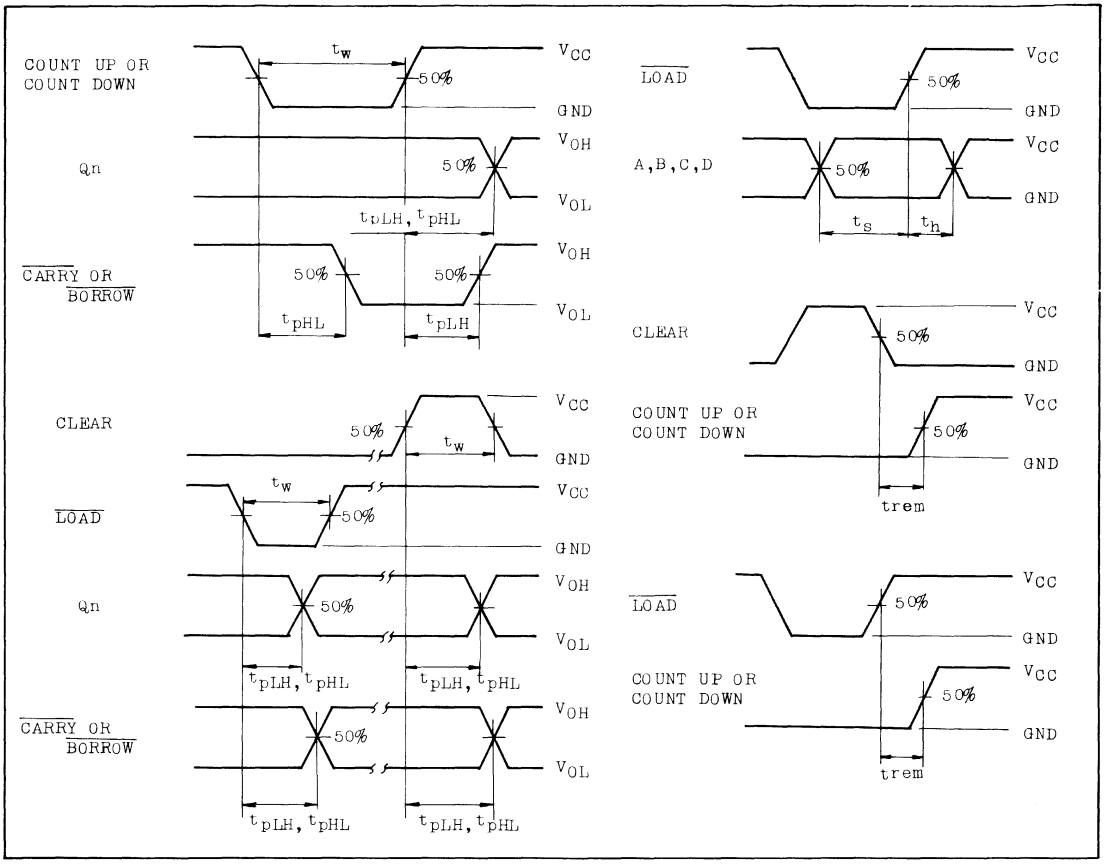
$I_{CC(opr.)}$ TEST WAVERORM



* : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC192P/F
TC74HC193P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

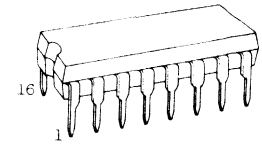
TC74HC194P/F

TC74HC194P/F 4-BIT PIPO SHIFT REGISTER

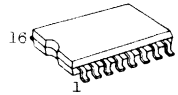
The TC74HC194 a high speed CMOS 4-BIT BIDIRECTIONAL SHIFT REGISTER fabricated with silicon C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of parallel in, parallel out, 4 ibt register with shift right and shift left input. In parallel mode, data of D0 ∿ D3 are stored into the internal flip-flops at the low-to-high level transition of the clock pulse. Shift right and shift left inputs are inhibited during parallel operating mode. In shift right and shift left modes, data from shift right and shift left inputs are shifted to the right and to the left by 1 bit, respectively, synchronously with the low-to-high level edge of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS194



DIP16(3D16A-P)



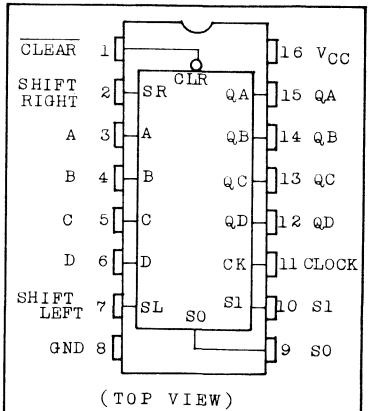
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC194P/F

TRUTH TABLE

INPUTS										OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SL	SR	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

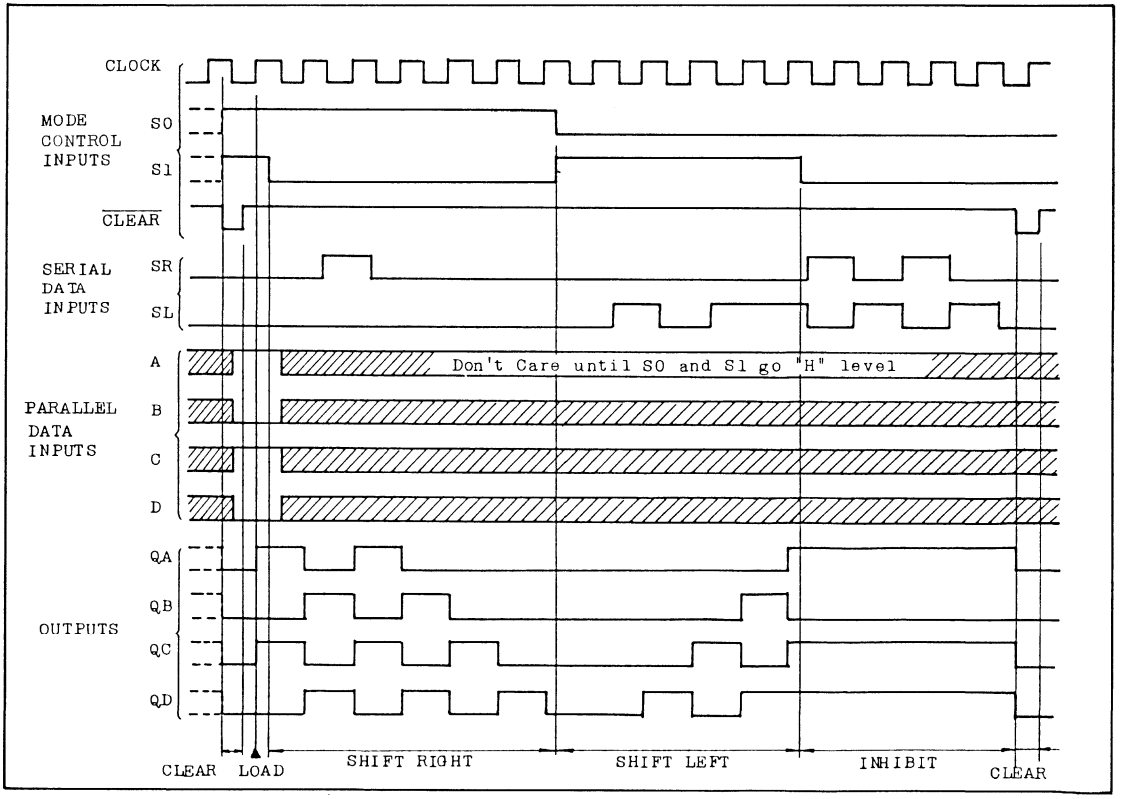
X: Don't care

a ∿ d: The level of steady state input voltage at input A ∿ D respectively

QA0 ∿ QD0: No change

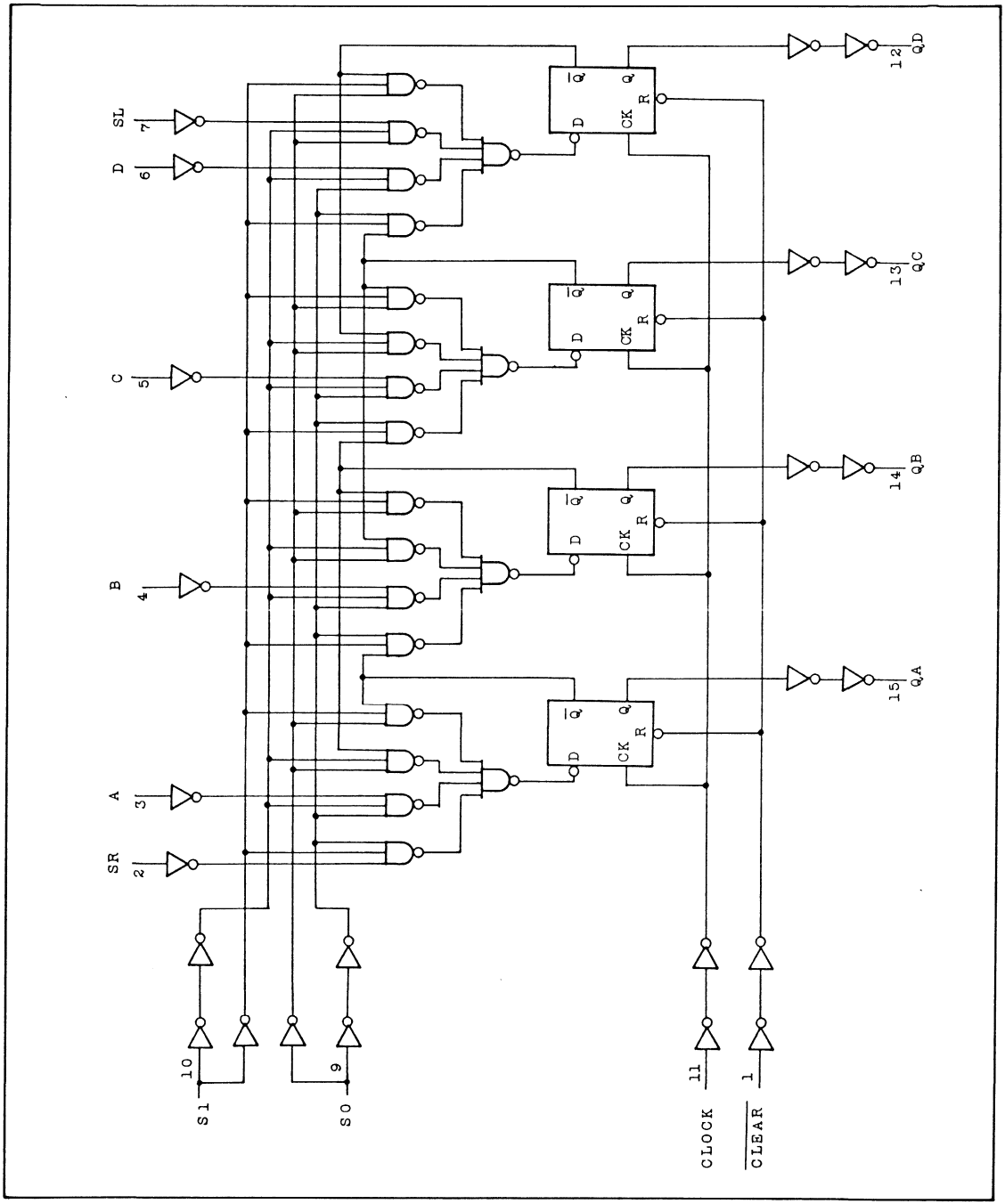
QAn ∿ QDn: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

TIMING CHART



TC74HC194P/F

LOGIC DIAGRAM

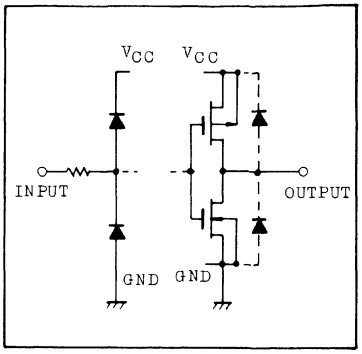


TC74HC194P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

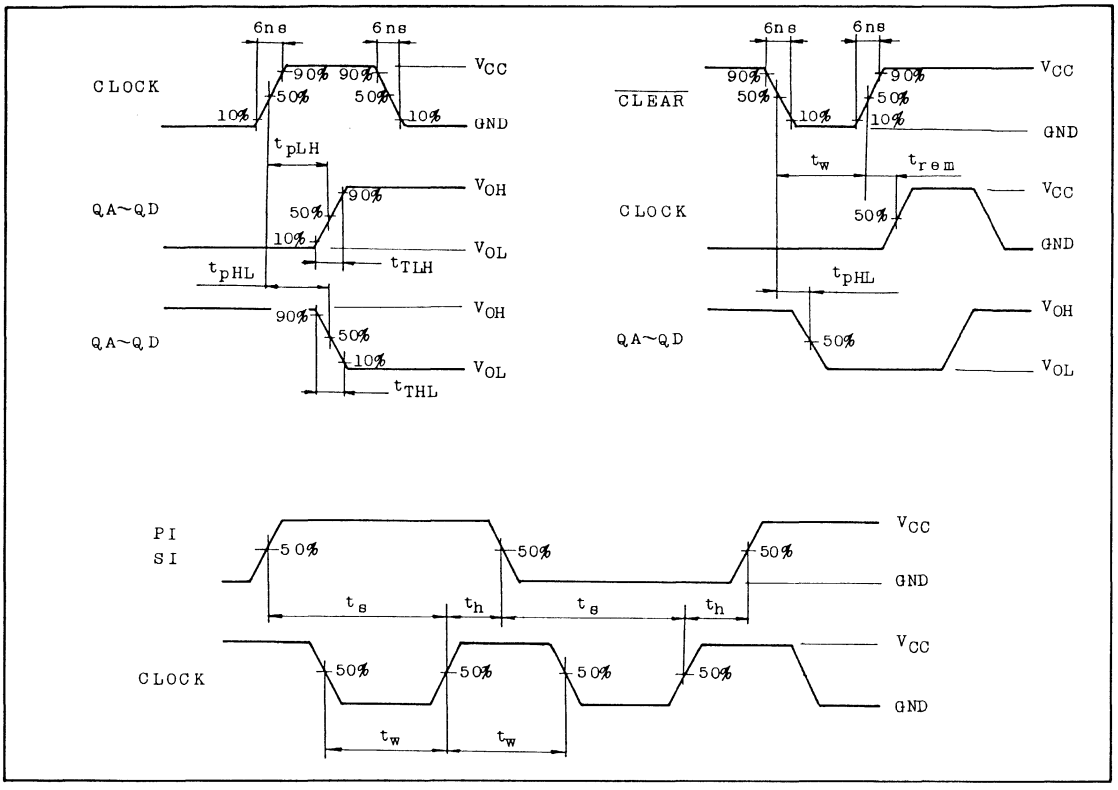
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S_{IN}, P_{IN})	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S0, S1)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	103	-	-	-	

Note (1): C_{PD} is defined as the vlaue of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit.) Average operating current can be obtained by the equation hereunder.

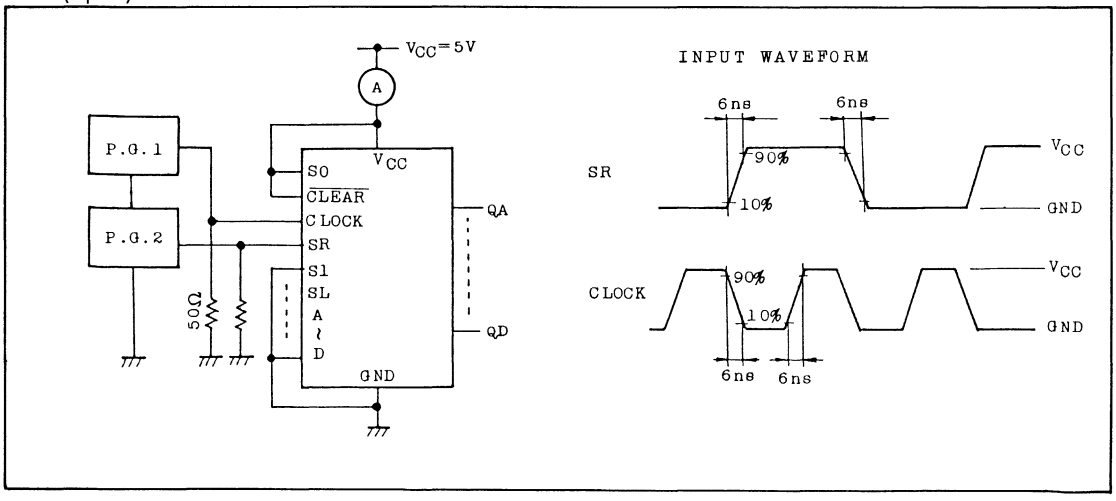
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC194P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

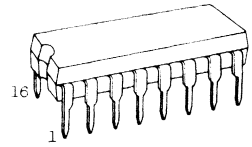
TC74HC195P/F

TC74HC195P/F 4-BIT PARALLEL SHIFT REGISTER

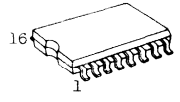
The TC74HC195 is a high speed CMOS 4-BIT SHIFT REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This register features parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{LOAD}$ input. When the SHIFT/$\overline{LOAD}$ input is held low, the parallel mode operation is designated. The data of A ∿ D inputs is loaded into the internal register and appears at the outputs after the positive transition of the clock. When the SHIFT/$\overline{LOAD}$ input is held high, the serial mode operation having J, $\overline{K}$ logical inputs is designated and four flip-flops perform shifting at the positive transition of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS195



DIP16(3D16A-P)



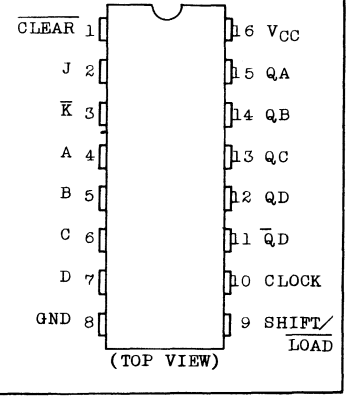
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TC74HC195P/F

TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{Q}$D
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{Q}$D0
H	H	↑	L	H	X	X	X	X	QAn	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	L	X	X	X	X	$\overline{Q}$An	QAn	QBn	QCn	$\overline{Q}$Cn

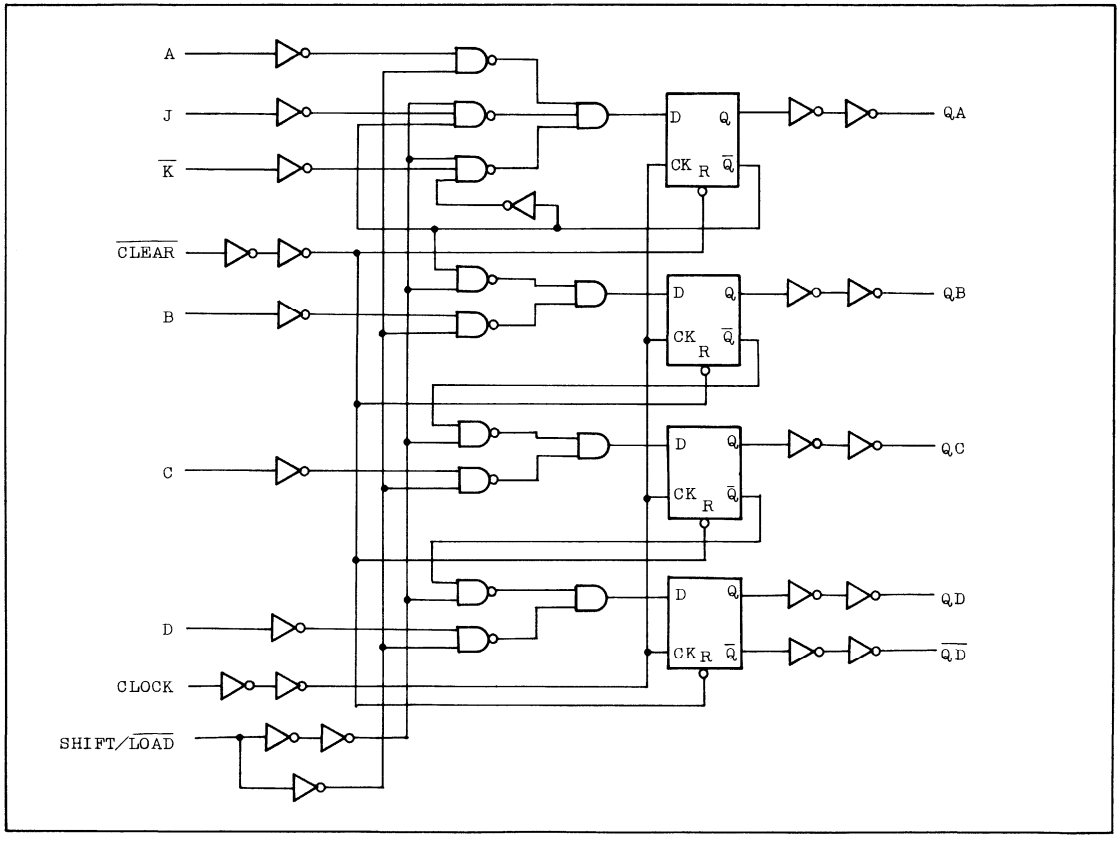
X: Don't care

QA0 ∿ AD0: No change

QAn ∿ QDn: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

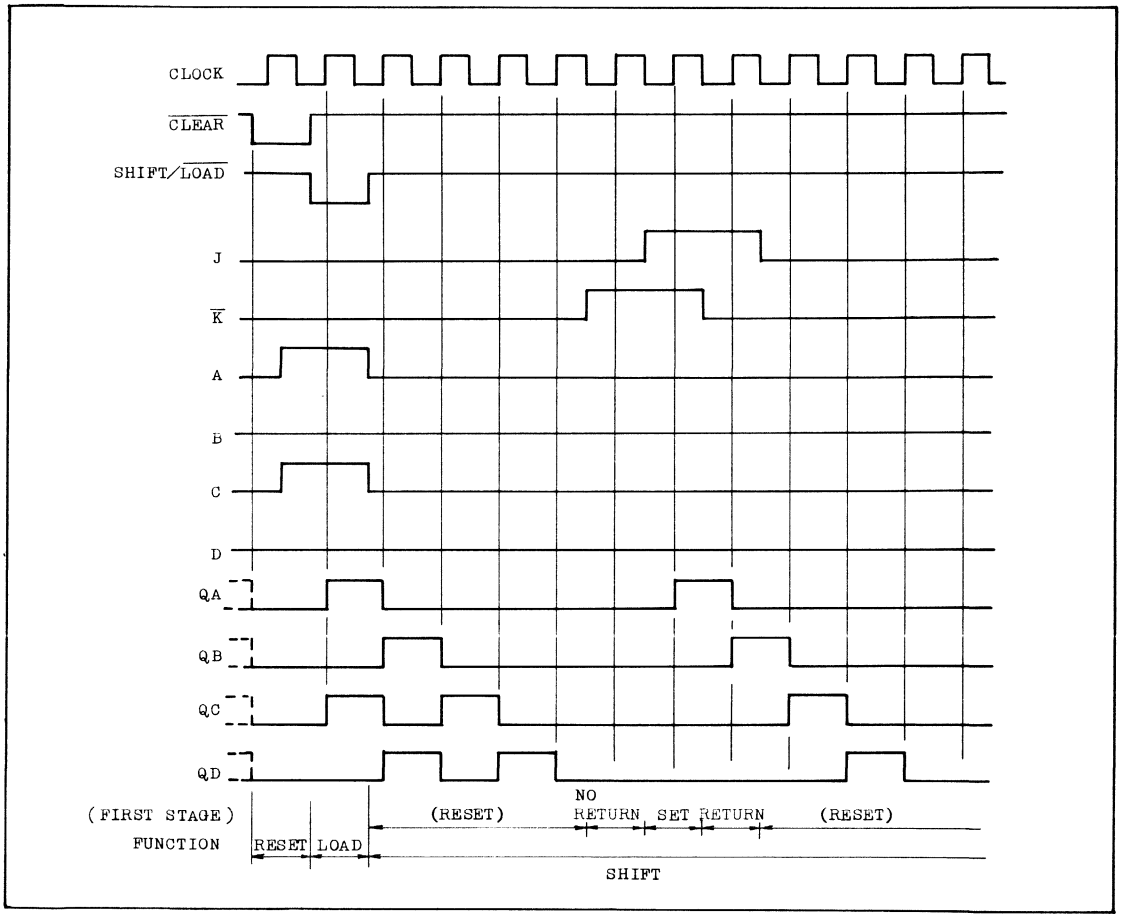
a ...d, $\overline{d}$: The level of steady state input voltage at inputs A ∿ D respectively.

LOGIC DIAGRAM



TC74HC195P/F

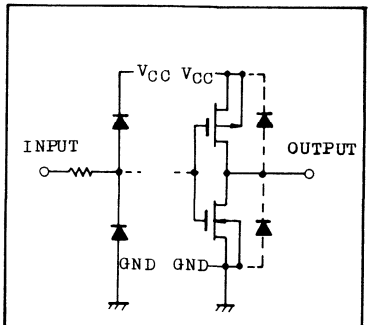
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC195P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Propagation Delay Time ($\overline{CLR}$ - Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	32	51	-	27	-	
			6.0	38	60	-	32	-	

AC ELECTRICAL CHARACTERISTICS (Continued)

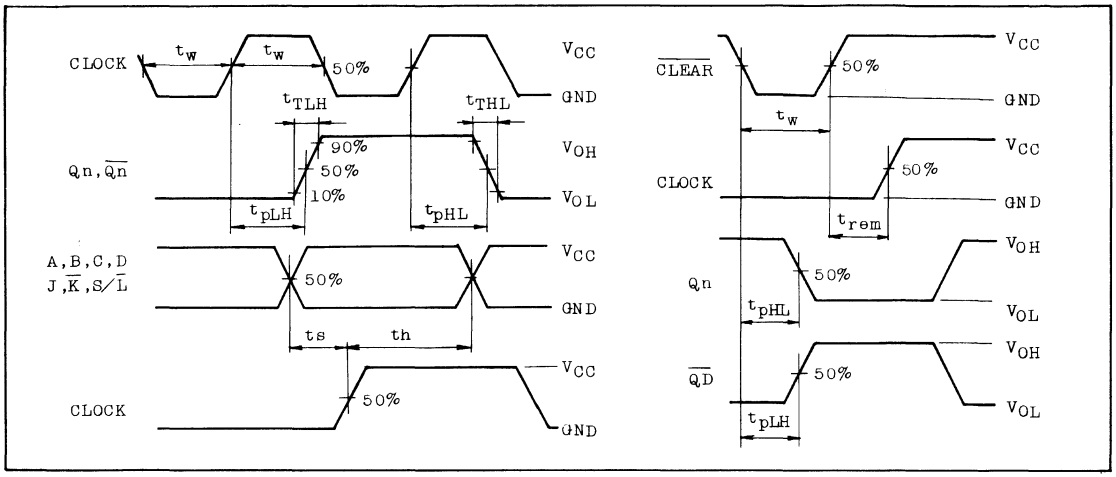
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (PI)	t_s		2.0	-	15	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set Up Time (J, $\overline{K}$, S/$\overline{L}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	1	5	-	6	
			6.0	-	1	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	115	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

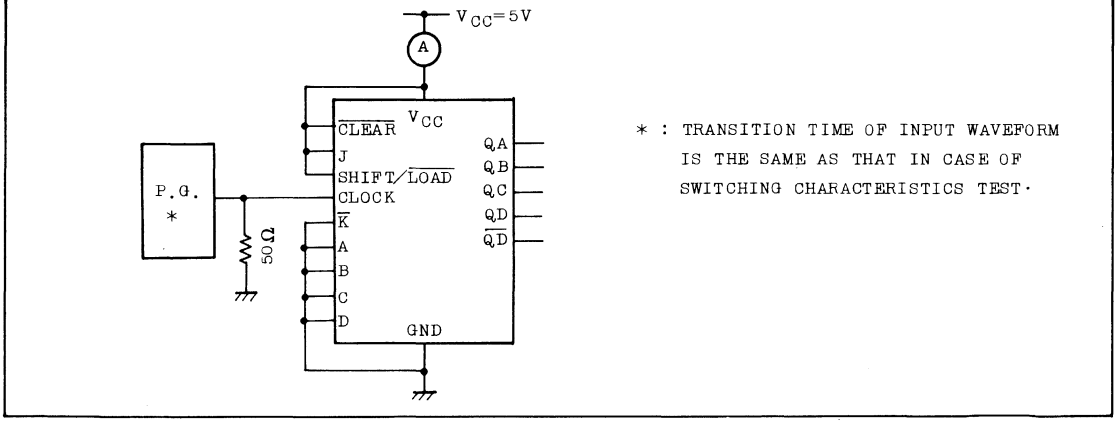
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC195P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC221P/F

TC74HC221P/F DUAL MONOSTABLE MULTIVIBRATOR

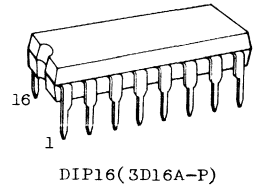
The TC74HC221 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaing the CMOS low power dissipation.
There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CLR}$ INPUT (Positive-edge input). After triggering, Output keeps MONOSTABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CLR}$ input breaks this STABLE STATE. Next coming new trigger in MONOSTABLE period is not effected. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5kΩ to 1MΩ
$V_{CC}\geq$3.0V from 1kΩ to 1MΩ

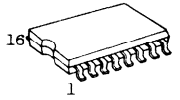
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=32ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at VCC=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range .... t_w(OUT)=150ns ∿ 60s over at V_{CC}=4.5V
- Pin and Function Compatible with LS221



DIP16(3D16A-P)



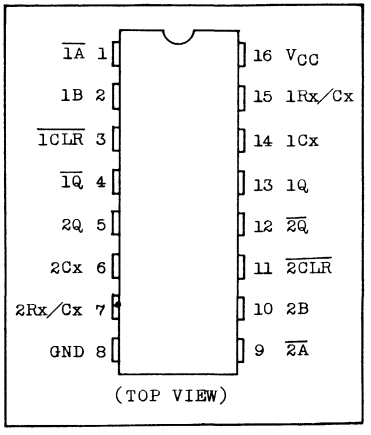
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP) * 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TC74HC221P/F

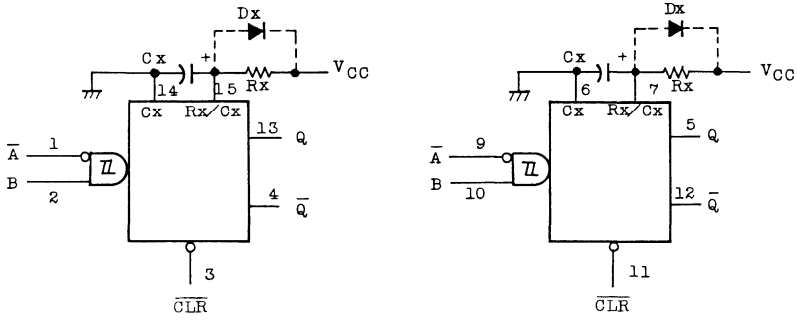
TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L△	H△	INHIBIT
H	X	H	L△	H△	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
L	H	↑	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:DON'T CARE

△:EXCEPT FOR MONOSTABLE PERIOD

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls dowen rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

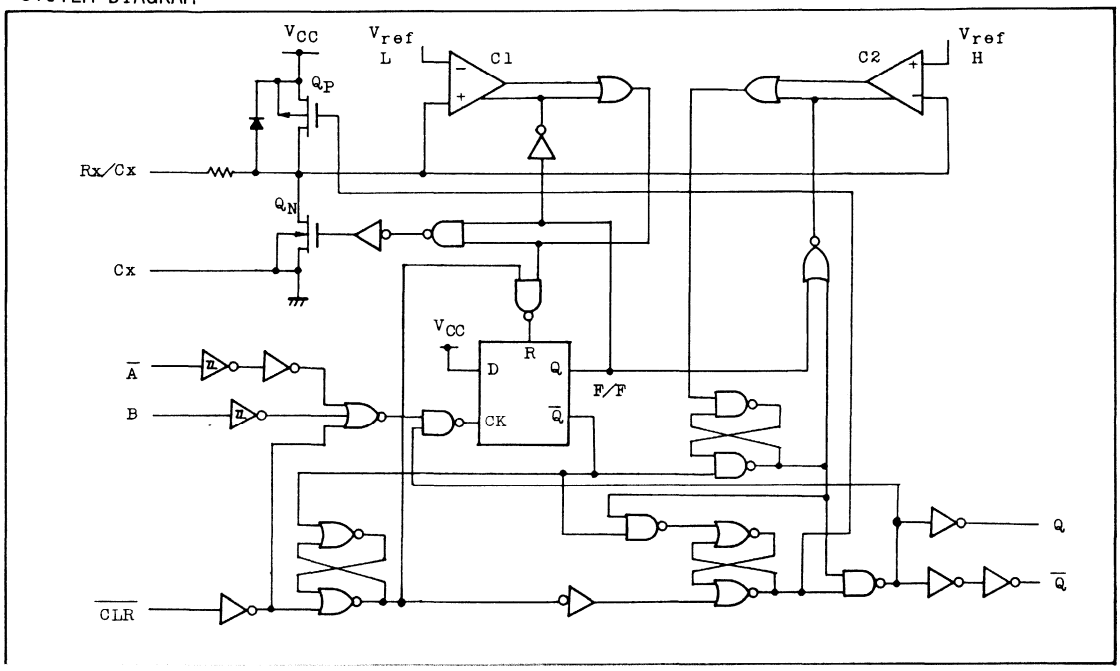
$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

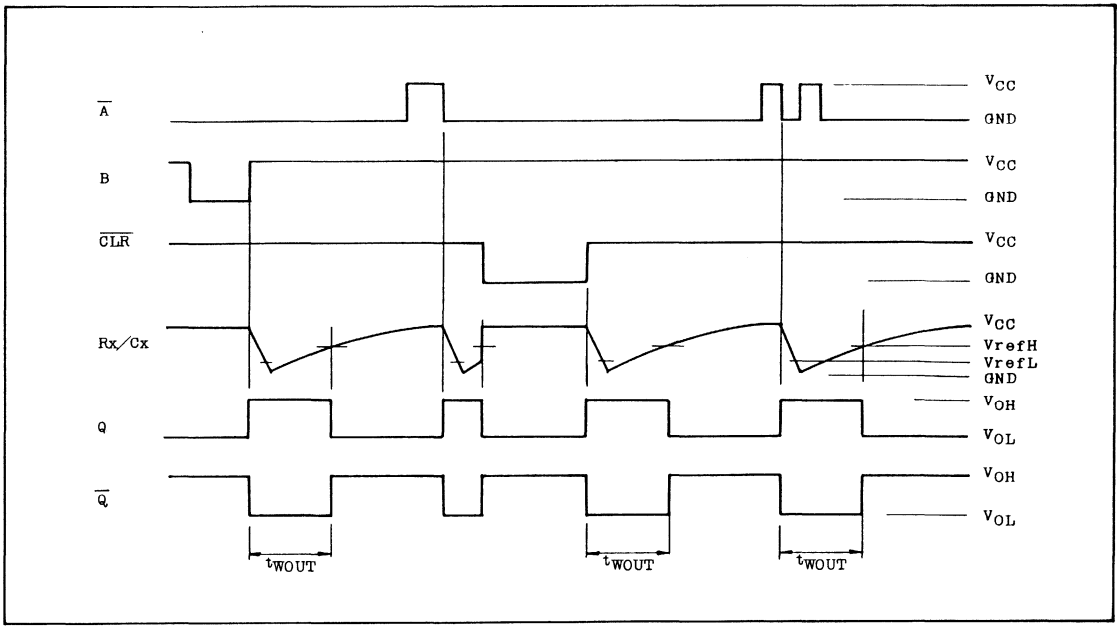
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

TC74HC221P/F

SYSTEM DIAGRAM



TIMING CHART



TC74HC221P/F

FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CLR}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx.Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_W(OUT)$ is as follows.

$$t_W(OUT) = 0.70 \quad Cx\ Rx$$

(3) Reset operation

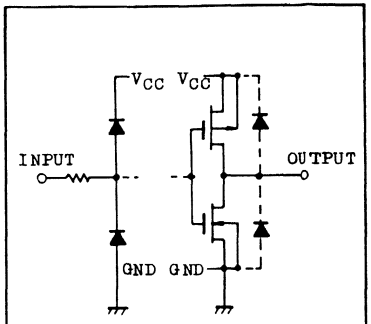
$\overline{CLR}$ is normally "H". If $\overline{CLR}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CLR}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC221P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.31	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=VCC or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per Circuit

TC74HC221P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

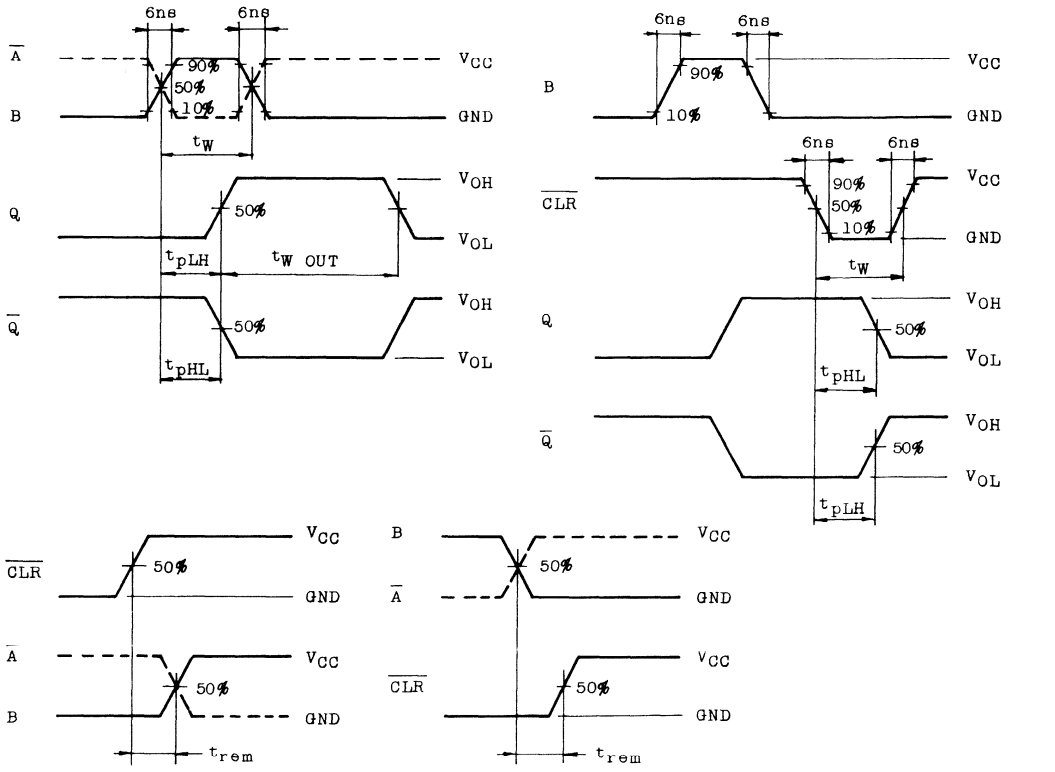
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$,B TRIGGER-Q,$\overline{Q}$)	t_{pLH}		2.0	-	144	280	-	350	
	t_{pHL}		4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CLR}$ TRIGGER-Q,$\overline{Q}$)	t_{pLH}		2.0	-	164	310	-	390	
	t_{pHL}		4.5	-	41	62	-	78	
			6.0	-	35	53	-	66	
Propagation Delay Time ($\overline{CLR}$-Q,$\overline{Q}$)	t_{pLH}		2.0	-	108	210	-	265	
	t_{pHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Trigger Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error. Between Circuits In same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Removal Time ($\overline{A}$,B TRIGGER)	t_{rem}		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$ TRIGGER)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Output Pulse Width	t_{wOUT} (MIN)	Cx=0 Rx=5kΩ (V_{CC}=2V)	2.0	-	490	1450	-	1825	
		Rx=1kΩ (V_{CC}=4.5, 6V)	4.5	-	190	290	-	365	
			6.0	-	170	260	-	325	
Output Pulse Width	t_{wOUT}	Cx=0.01μF Rx=10kΩ	2.0	72	85	98	72	98	μs
			4.5	72	80	88	72	88	
			6.0	72	80	88	72	88	
		Cx=0.1μF Rx=10kΩ	2.0	0.67	0.75	0.83	0.67	0.83	ms
			4.5	0.67	0.73	0.79	0.67	0.79	
			6.0	0.67	0.73	0.79	0.67	0.79	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	109	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test circuit). Average operating current can be obtained by equation hereunder.

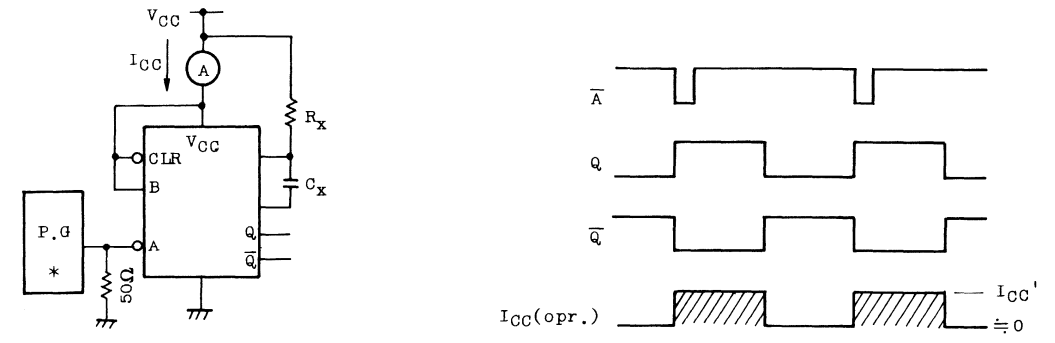
$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current, Duty: %)

SWITCHING CHARACTERISTICS TEST WAVEFORM



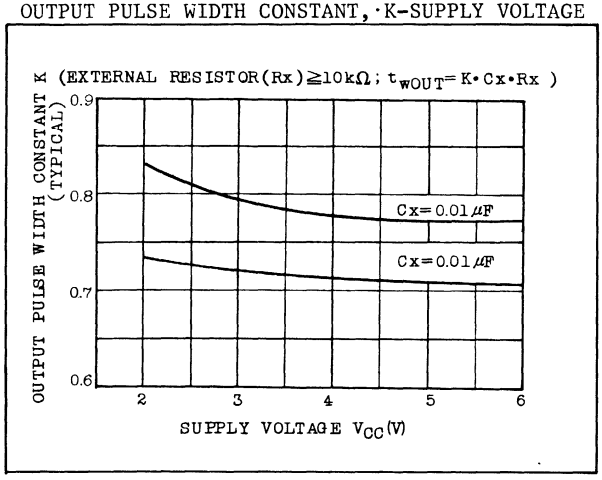
I_{CC}(opr.) TEST WAVEFROM



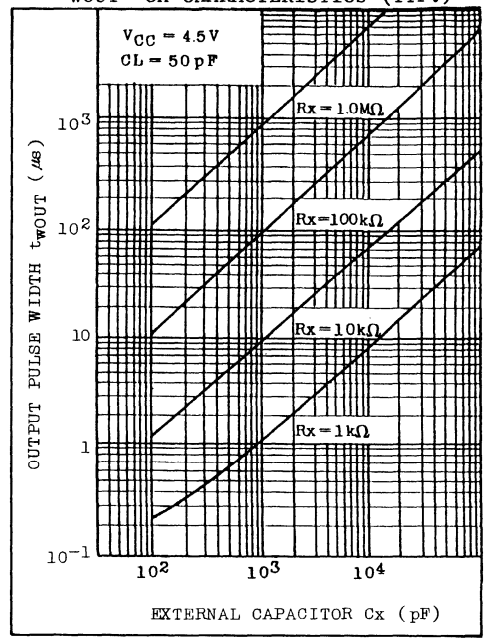
* INPUT TRANSITION TIME : 6ns ,
$V_{IH} = V_{CC}, V_{IL} = GND$

TC74HC221P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



C²MOS DIGITAL INTEGRATED CIRCUIT

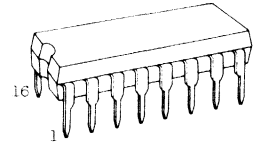
TC74HC237P/F

TC74HC237P/F 3-TO-8 LINE DECODER/LATCH

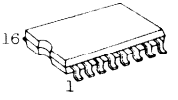
The TC74HC237 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go high. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Inverting type of the 74HC137



DIP16(3D16A-P)



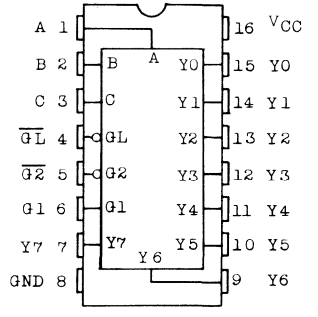
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

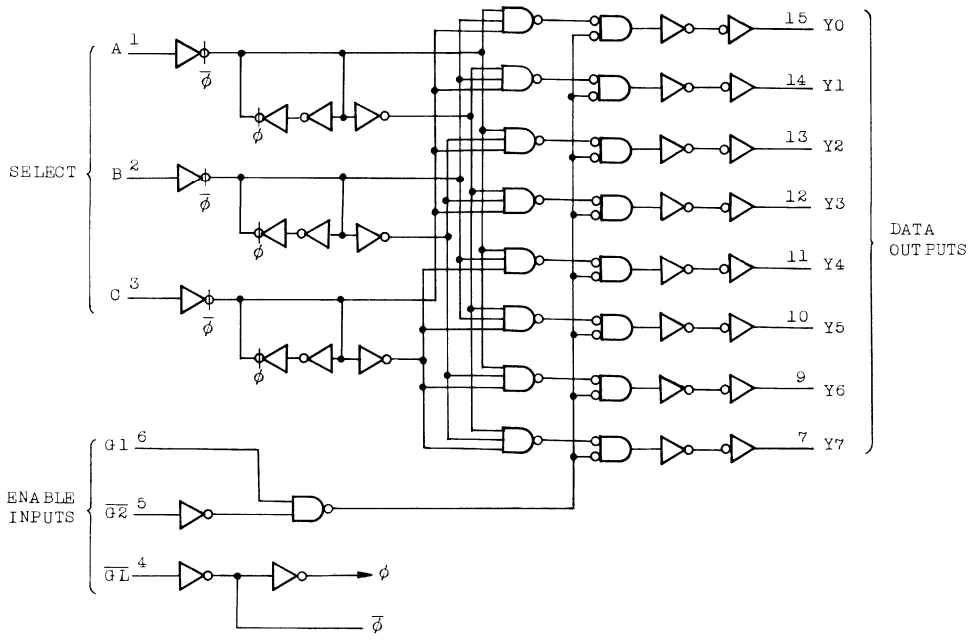
TC74HC237P/F

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H ; ALL OTHERS, L							

X : DON'T CARE

LOGIC DIAGRAM

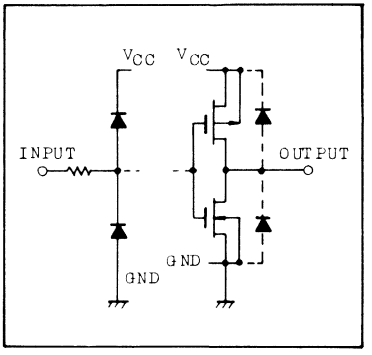


TC74HC237P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC237P/F

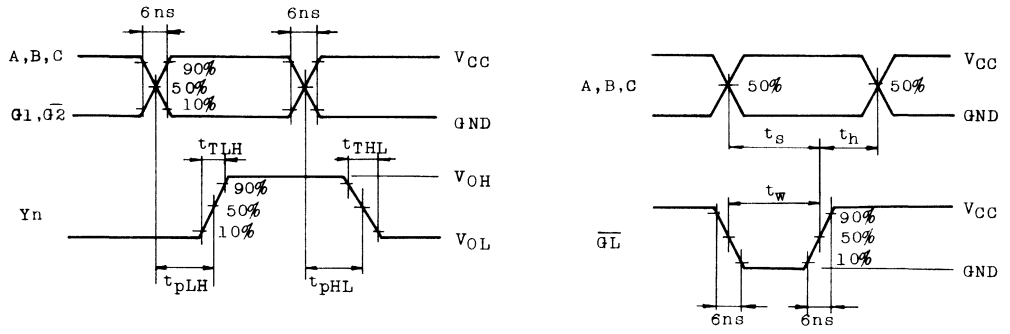
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{GL}$ - Y)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		2.0	-	12	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

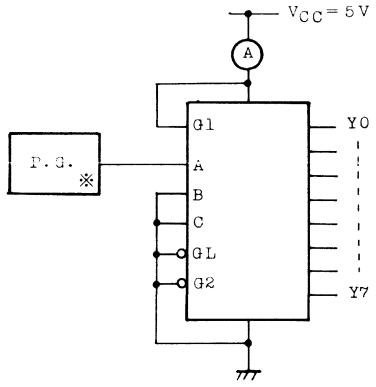
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



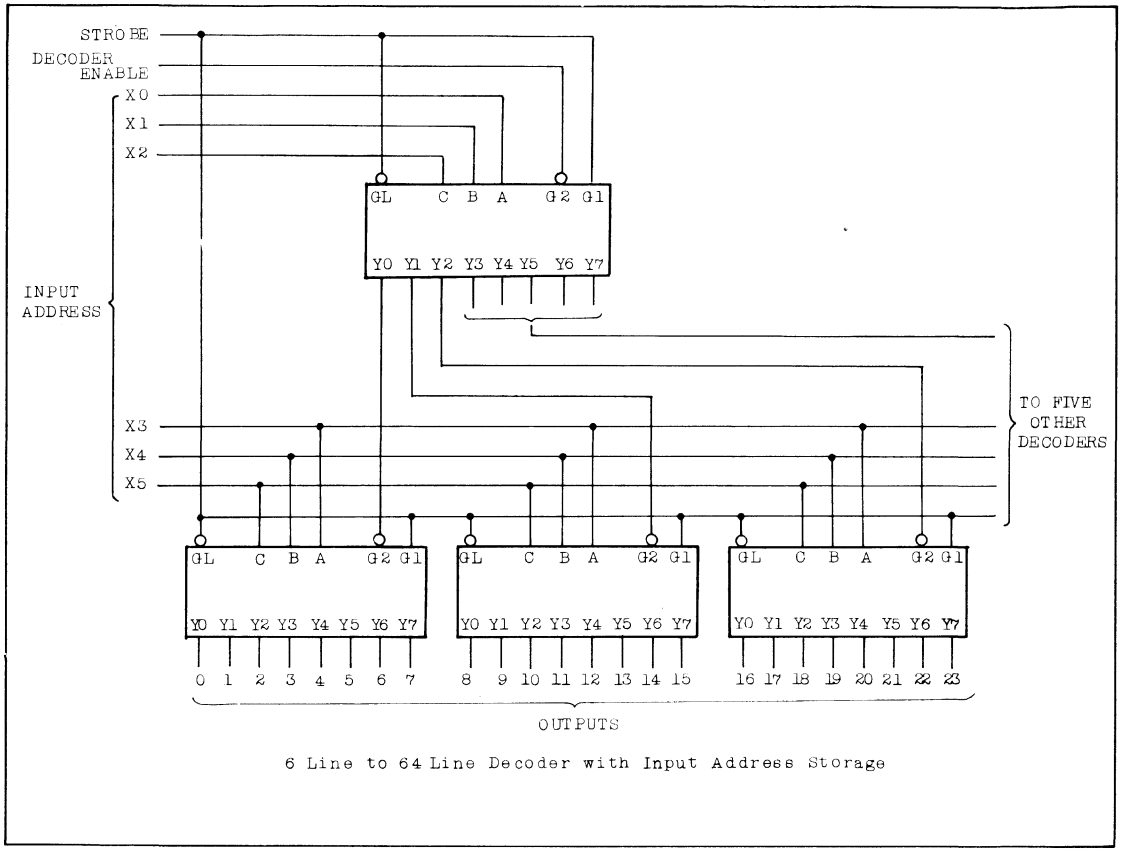
$I_{CC(Opr.)}$ TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TC74HC237P/F

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

C²MOS DIGITAL INTEGRATED CIRCUIT

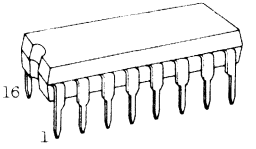
TC74HC238P/F

TC74HC238P/F 3-TO-8 LINE DECODER

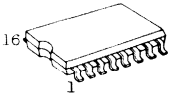
The TC74HC238 is a high speed CMOS 3-TO-8 LINE DECODER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go high. Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low. 3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... tpLH≒tpHL
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Noninverting type of the 74HC138



DIP16(3D16A-P)



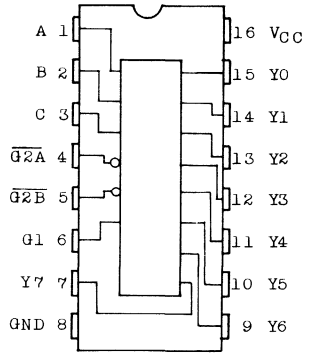
MFP16(F160C-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

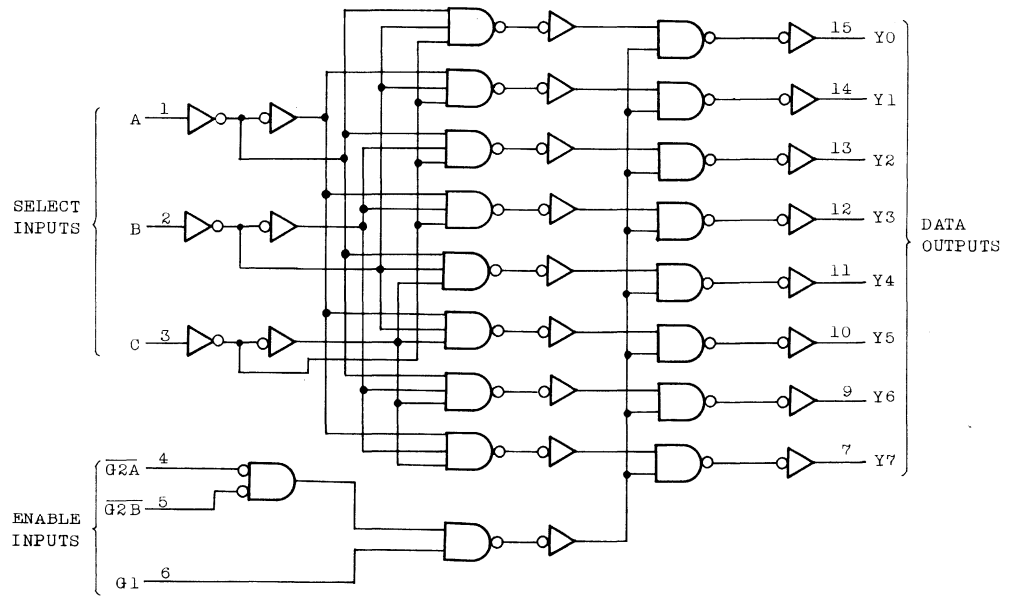
TC74HC238P/F

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED
ENABLE			SELECT											OUTPUT
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
X	X	L	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
H	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y0
L	L	H	L	L	H	L	H	L	L	L	L	L	L	Y1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	Y2
L	L	H	L	H	H	L	L	L	H	L	L	L	L	Y3
L	L	H	H	L	L	L	L	L	L	H	L	L	L	Y4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	Y5
L	L	H	H	H	L	L	L	L	L	L	L	H	L	Y6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Y7

X: Don't care

LOGIC DIAGRAM

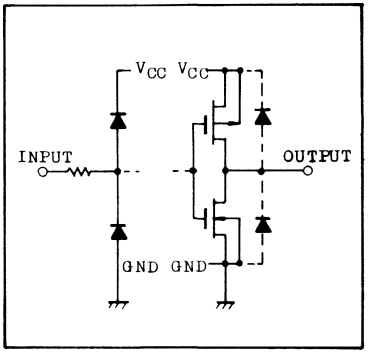


TC74HC238P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC238P/F

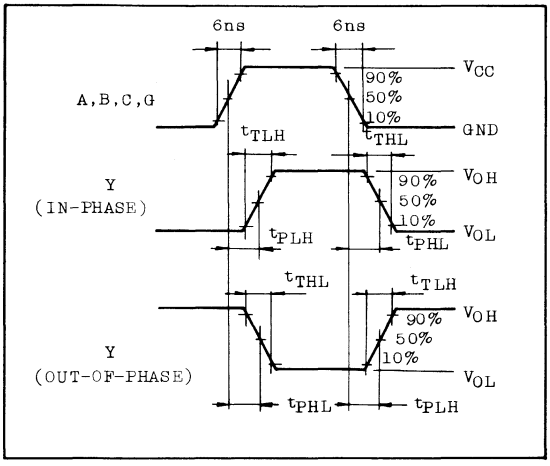
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	80	155	-	195	
			4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	88	170	-	215	
			4.5	-	22	34	-	43	
			6.0	-	19	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	67	-	-	-	

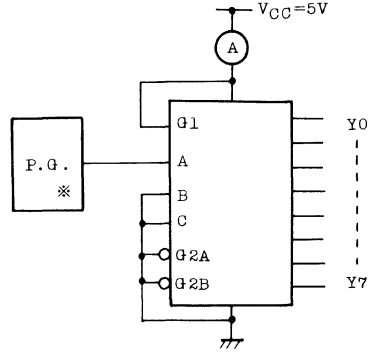
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



※ INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC240P/F·TC74HC241P/F
TC74HC244P/F

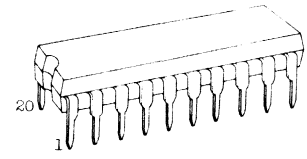
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC240P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HC241P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS
TC74HC244P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

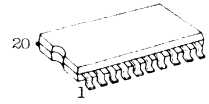
The TC74HC240, TC74HC241 and TC74HC244 are high speed CMOS OCTAL BUS BUFFER's fabricated with silicon C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input govern four BUS BUFFERs.
These divices are designated to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=12ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS 240/241/244



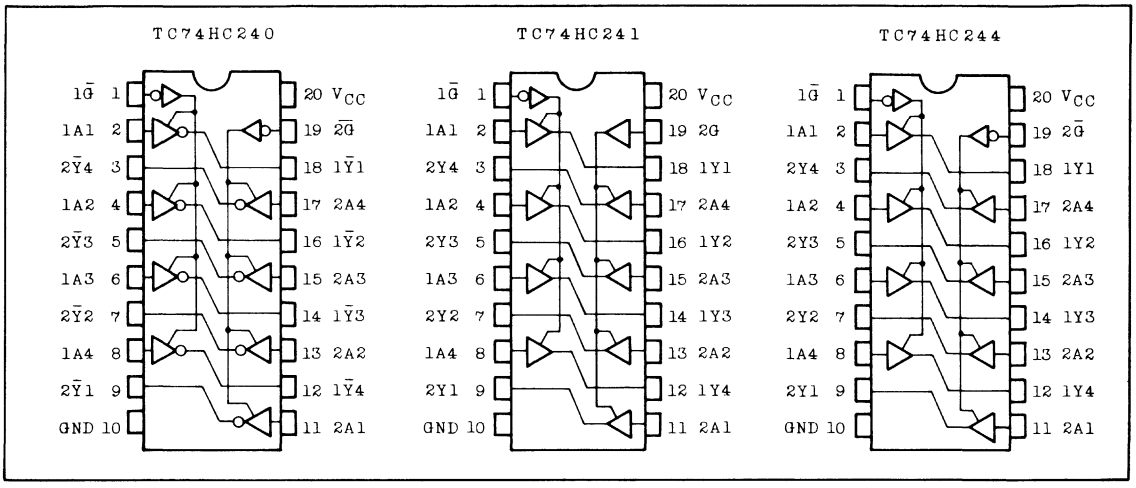
DIP20(3D20A-P)



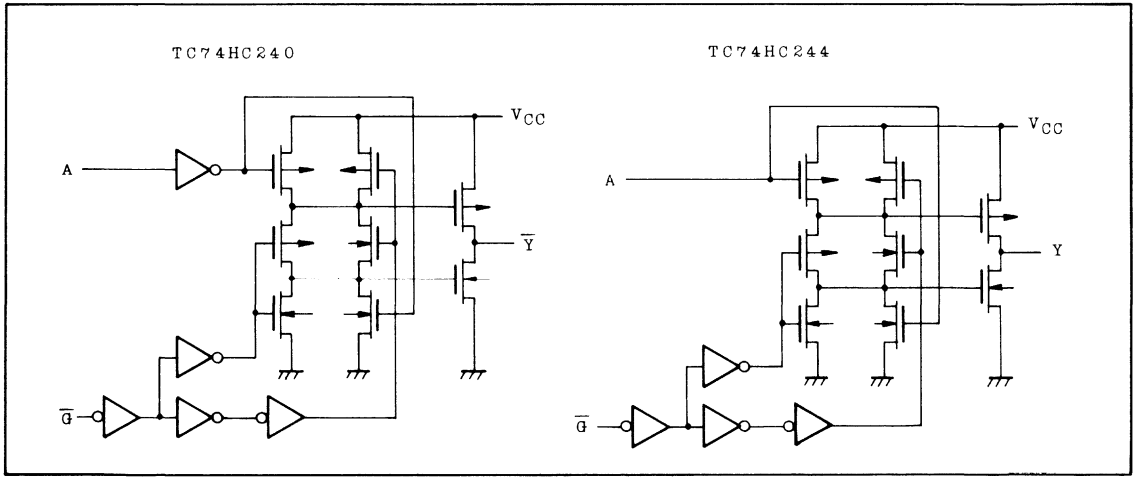
MFP20(F20GA-P)

TC74HC240P/F • TC74HC241P/F TC74HC244P/F

PIN ASSIGNMENT (TOP VIEW)



CIRCUIT SCHEMATC (1/8 PACKAGE)



TRUTH TABLE

INPUTS			OUTPUTS	
$\bar{G}$	G△	A_n	Y_n	$\bar{Y}_n$ △△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : Applied only for TC74HC241

△△ : Applied only for TC74HC240

X : Don't Care

Z : High Impedance

TC74HC240P/F·TC74HC241P/F TC74HC244P/F

ABSOLUTE MAXIMUM RATINGS

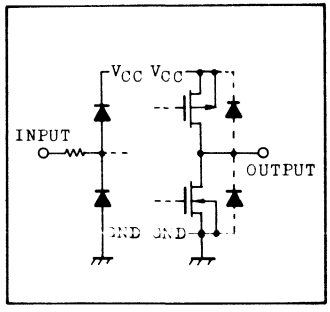
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

TC74HC240P/F·TC74HC241P/F TC74HC244P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

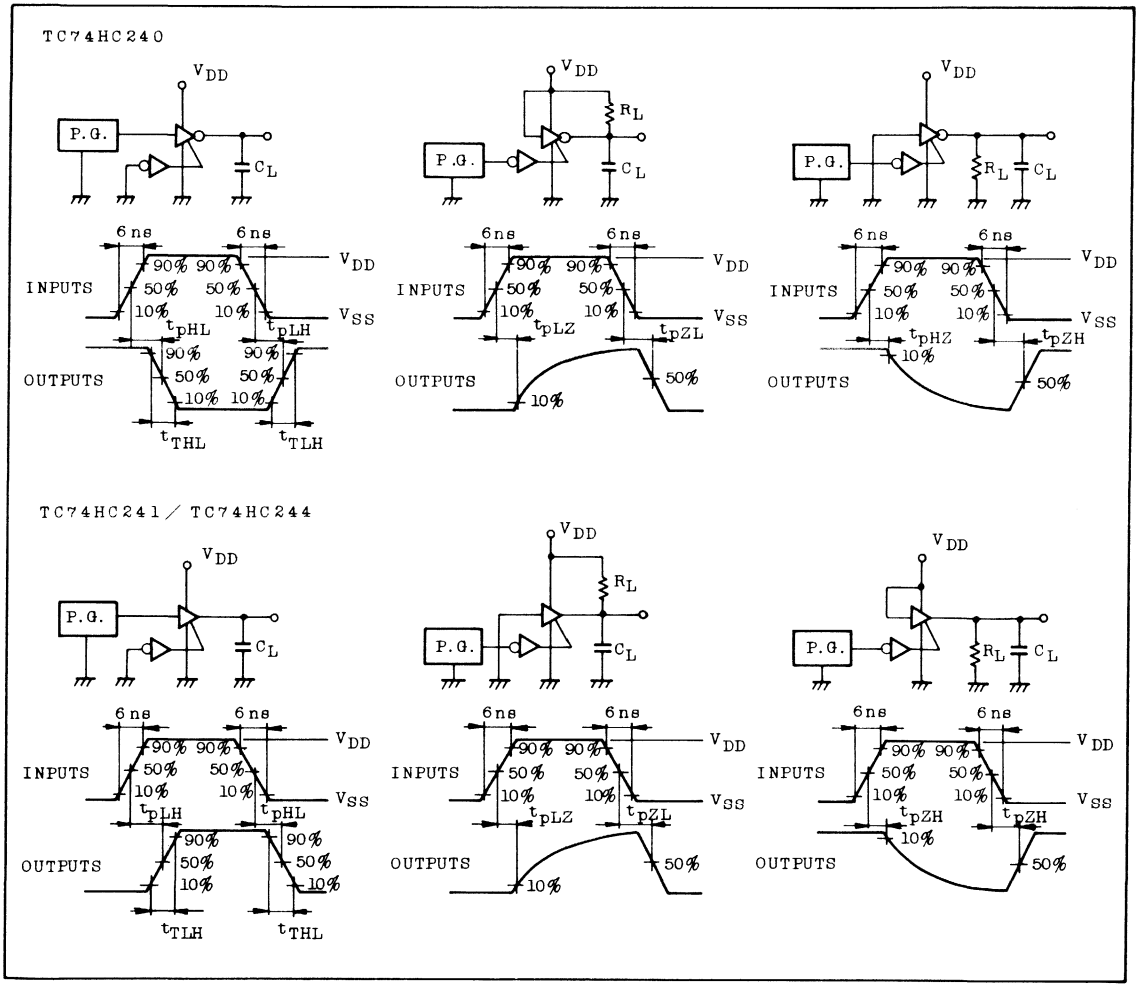
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	
Propagation Delay Time ΔΔ	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Output Enable Time Δ	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	44	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	40	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/8$ (per Gate)

(2) Δ : for TC74HC241 only
ΔΔ: for TC74HC240 only

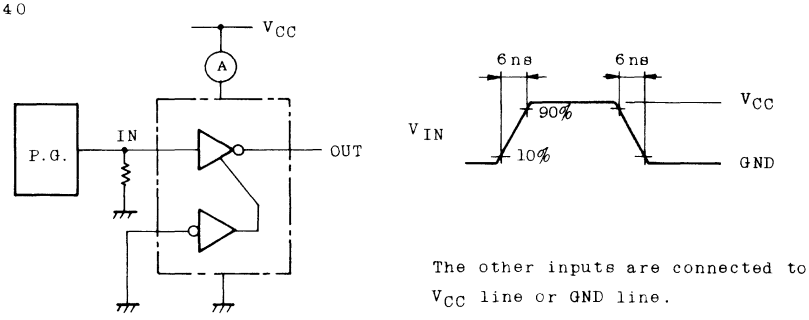
SWITCHING CHARACTERISTICS TEST CIRCUIT



TC74HC240P/F · TC74HC241P/F
TC74HC244P/F

$I_{CC(opr)}$ TEST CIRCUIT

TC74HC240



The other inputs are connected to V_{CC} line or GND line.

TC74HCT240P·TC74HCT241P TC74HCT244P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT240P OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS (TTL INPUT LVEL)
TC74HCT241P OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS (TTL INPUT LEVEL)
TC74HCT244P OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS (TTL INPUT LEVEL)

GENERAL DESCRIPTION

The TC74HCT240, TC74HCT241 and TC74HCT244 are high speed CMOS OCTAL BUS BUFFER's fabricated with silicon C^2MOS technology.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

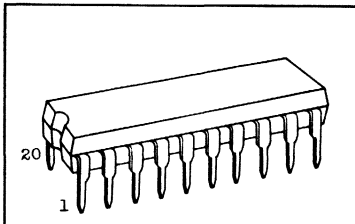
The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input govern four BUS BUFFERs.

These divices are designated to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage

FEATURES:

- High Speed ..... t_{pd}=20ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS 240/241/244



DIP20(3D20A-P)

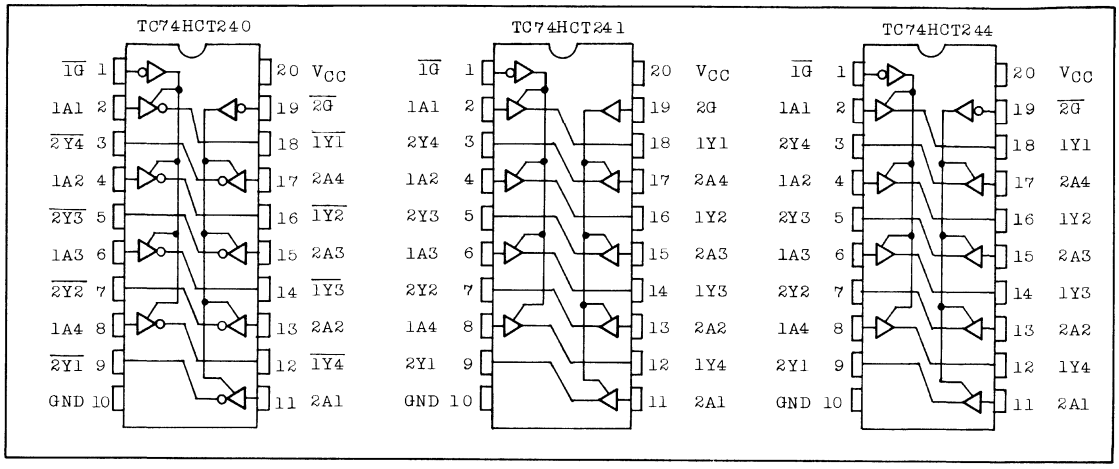
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	An	Yn	$\overline{Yn}$ △△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

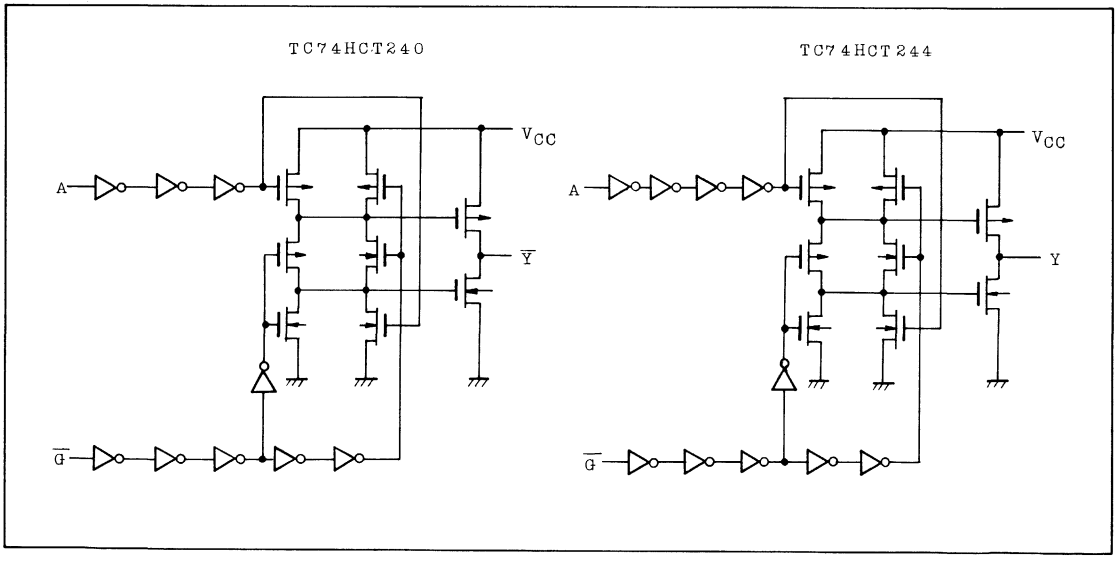
△ : TC74HCT241 ONLY
△△ : TC74HCT240 ONLY
X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HCT240P·TC74HCT241P
TC74HCT244P

PIN ASSIGNMENT (TOP VIEW)



CIRCUIT DIAGRAM (Per Circuit)

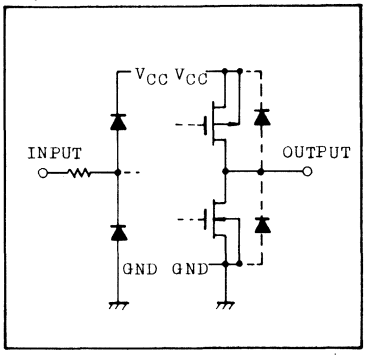


TC74HCT240P·TC74HCT241P TC74HCT244P

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

INPUT and OUTPUT EQUIVALENT CIRCUIT



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	

TC74HCT240P·TC74HCT241P TC74HCT244P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

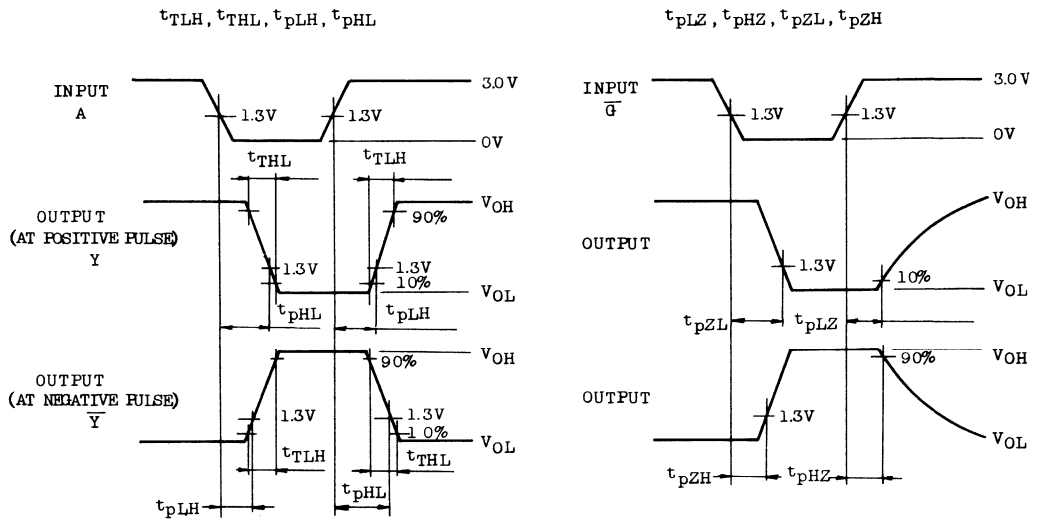
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{TLH}		4.5	-	8	12	-	15	ns
Propagation Delay Time (HCT240)	t_{pLH} t_{pHL}		4.5	-	22	35	-	42	
Propagation Delay Time (HCT241, HCT244)	t_{pLH} t_{pHL}		4.5	-	23	36	-	44	
Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	4.5	-	23	35	-	43	
Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	4.5	-	30	47	-	57	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT240		-	42	-	-	-	
		TC74HCT241		-	49	-	-	-	
		TC74HCT244		-	46	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

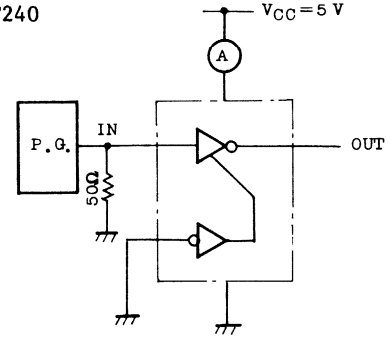
TC74HCT240P·TC74HCT241P
TC74HCT244P

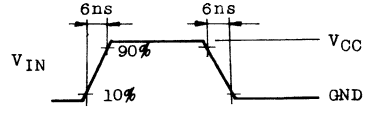
SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT

TC74HCT240





The other inputs are connected to V_{CC} line or GND line.

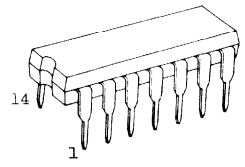
TC74HC242P/F
TC74HC243P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

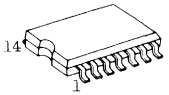
QUAD BUS TRANSCEIVER

TC74HC242P/F 3-STATE, INVERTING
TC74HC243P/F 3-STATE, NON-INVERTING

The TC74HC242 and TC74HC243 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by $\overline{GAB}$, GBA. $\overline{GAB}$ and GBA inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14(3D14A-P)



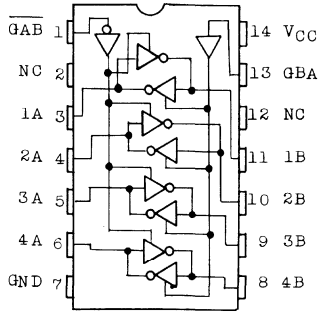
MFP14(F14GB-P)

FEATURES:

- High Speed ..... t_{pd}=10ns[242] t_{pd}=9ns[243] (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS242/243

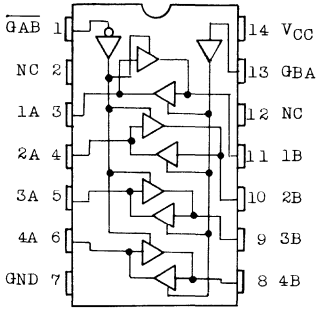
PIN ASSIGNMENT

TC74HC242



(TOP VIEW)

TC74HC243



(TOP VIEW)

NC : NO CONNECTION

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GBA	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	A=$\overline{B}$	A=B
L	L	INPUT	OUTPUT	B=$\overline{A}$	B=A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

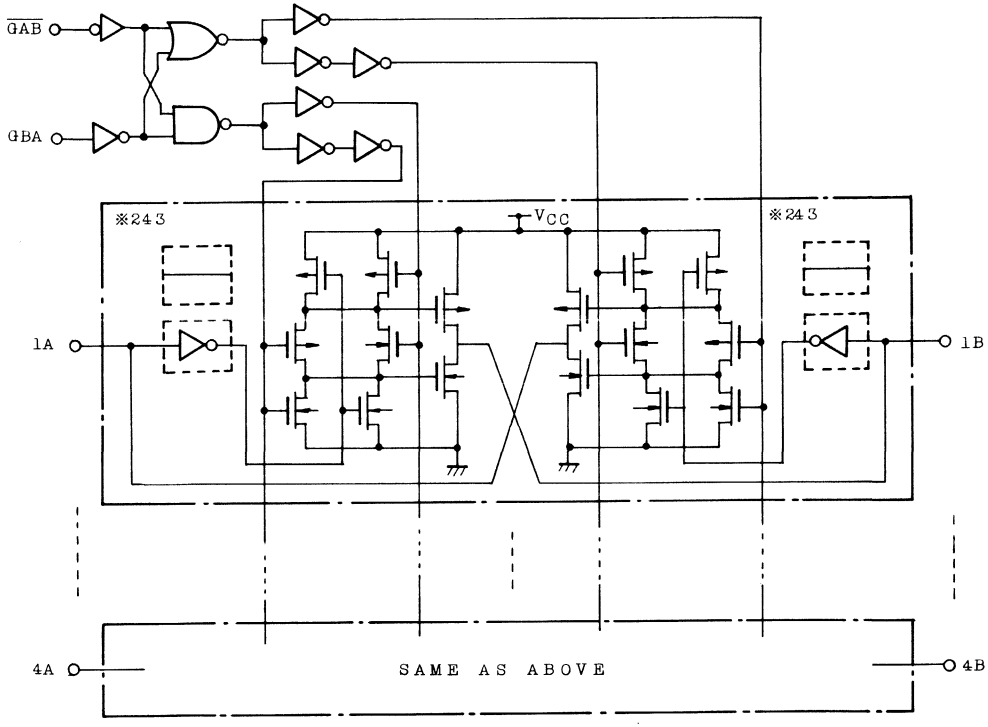
Z : HIGH IMPEDANCE

TC74HC242P/F
TC74HC243P/F

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

LOGIC DIAGRAM



In case of TC74HC243, input inverters marked ※ are eliminated.

TC74HC242P/F
TC74HC243P/F

ABSOLUTE MAXIMUM RATINGS

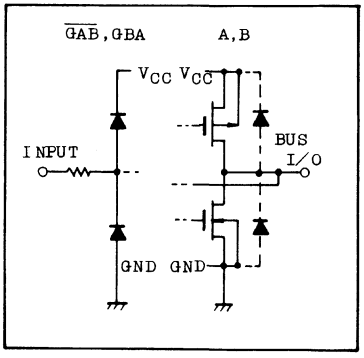
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be a applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MIN.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to $\overline{GAB}$, GBA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

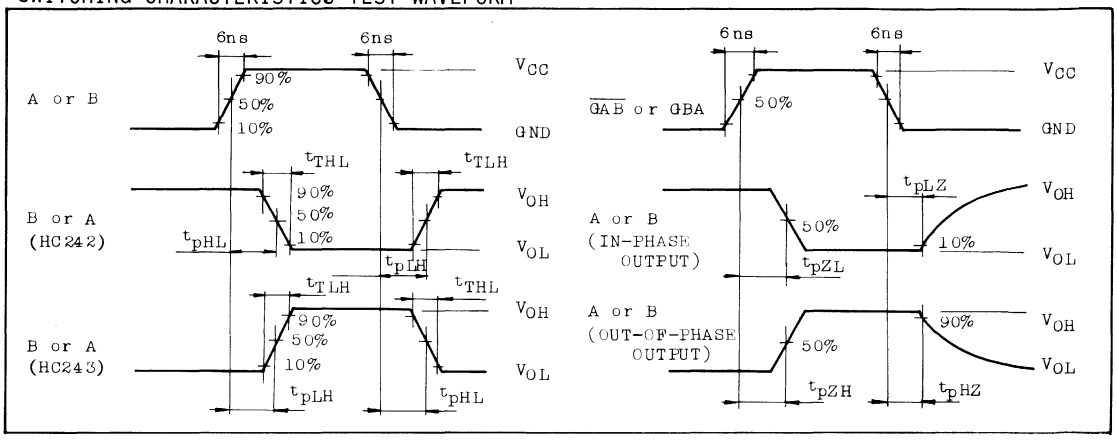
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time	t_{pLH}	TC74HC242	2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
	t_{pHL}	TC74HC243	2.0	-	44	90	-	115	
			4.5	-	11	18	-	23	
			6.0	-	9	15	-	20	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}	$\overline{GAB}$, GBA		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC242		-	42	-	-	-	
		TC74HC243		-	36	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

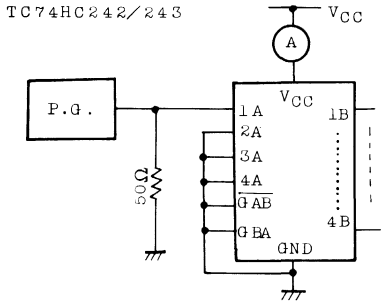
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

TC74HC242P/F
TC74HC243P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC245P/F·TC74HC640P/F TC74HC643P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

OCTAL BUS TRANSCEIVER

TC74HC245P/F 3-STATE, NON-INVERTING

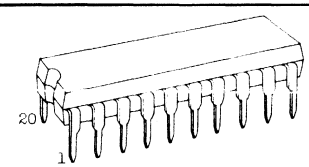
TC74HC640P/F 3-STATE, INVERTING

TC74HC643P/F 3-STATE, INVERTING AND NON-INVERTING

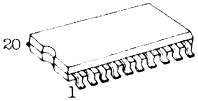
The TC74HC245, TC74HC640 and TC74HC643 utilize silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the driving capability of 15 LSTTL loads.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS245/640/643



DIP20(3D20A-P)

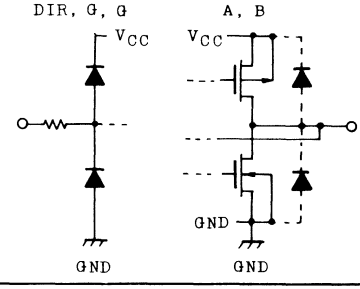


MFP20(F20GA-P)

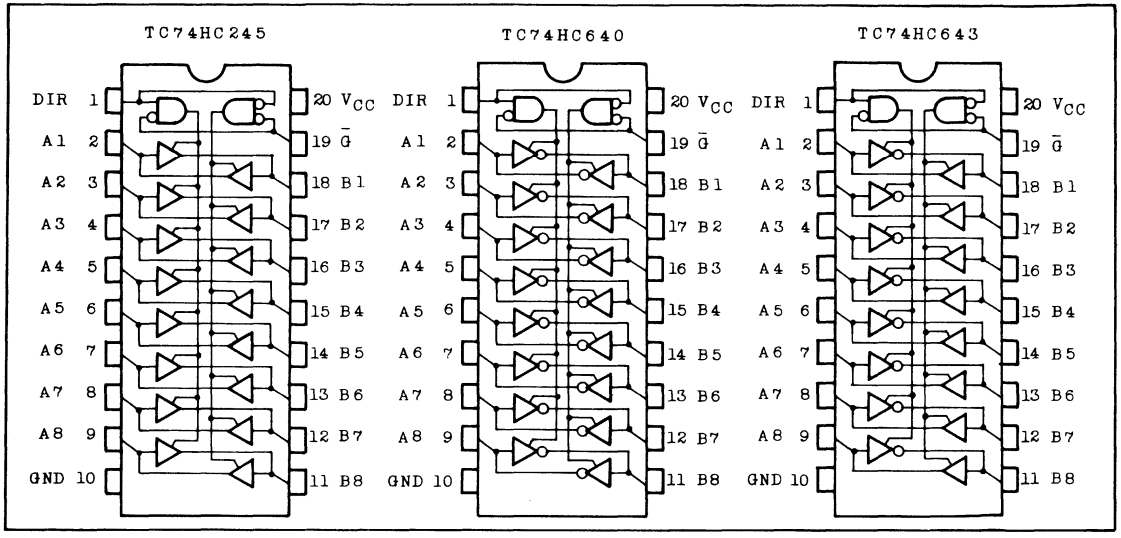
NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

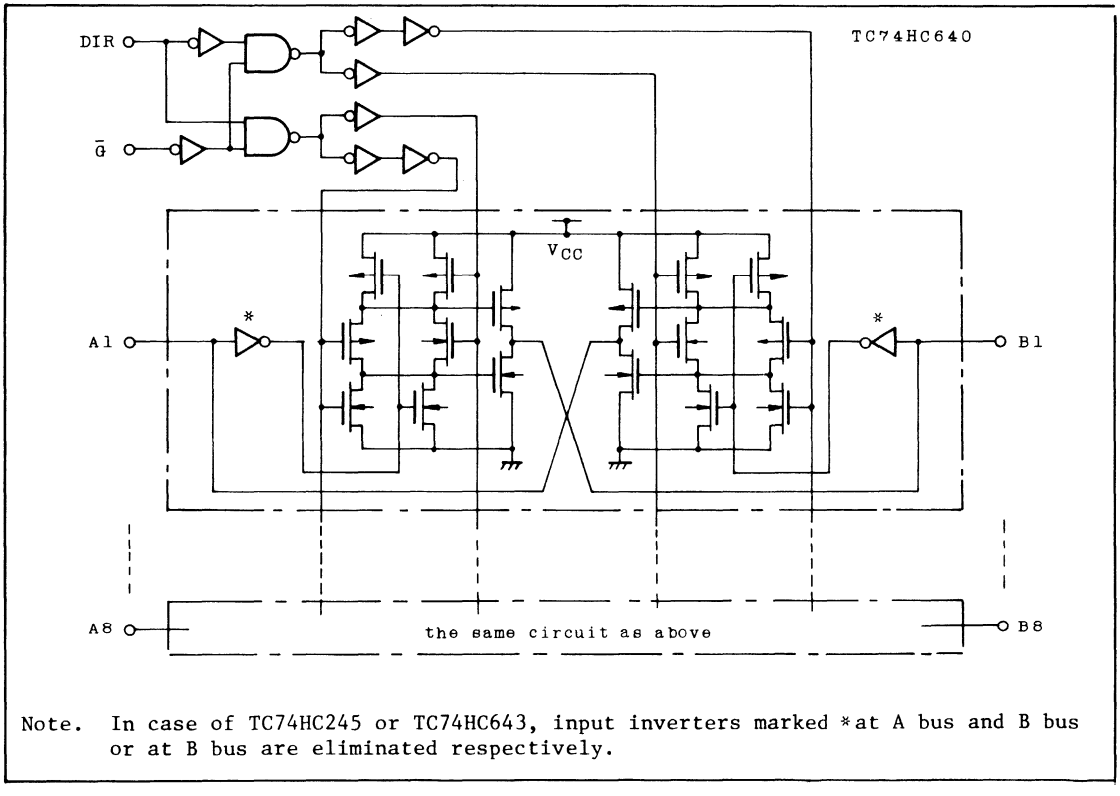
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC245P/F • TC74HC640P/F TC74HC643P/F



LOGIC DIAGRAM



Note. In case of TC74HC245 or TC74HC643, input inverters marked * at A bus and B bus or at B bus are eliminated respectively.

TC74HC245P/F·TC74HC640P/F TC74HC643P/F

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

TC74HC245P/F • TC74HC640P/F TC74HC643P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current*	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to DIR, G, $\overline{G}$ input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{tHL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	48	90	-	115	
			4.5	-	12	18	-	23	
			6.0	-	10	15	-	20	
Propagation Delay Time **	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

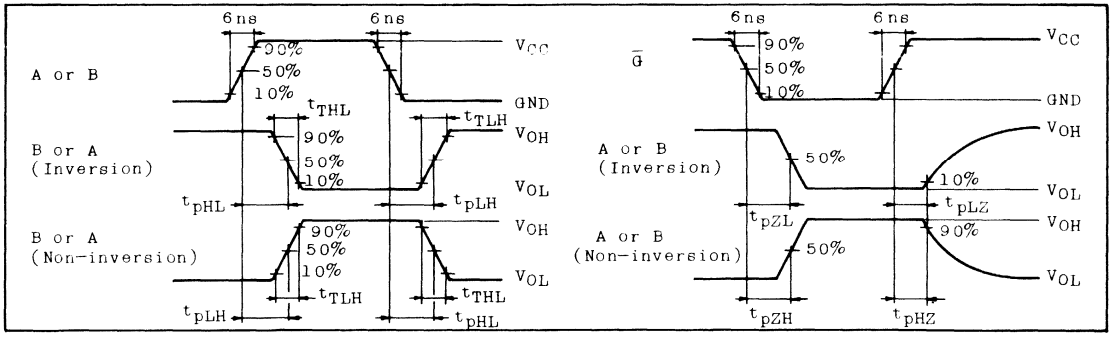
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
3-State Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	80	160	-	200	ns
	t_{pZH}		4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
3-State Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	80	190	-	240	
	t_{pHZ}		4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Input Capacitance	C_{IN}	DIR, G, $\overline{G}$		-	5	10	-	10	pF
Bus Input Capacitance	$C_{I/O}$	A_n, B_n		-	13		-		
Power Dissipation Capacitance	C_{PD}(1)	TC74HC245		-	33	-	-	-	
		TC74HC640/643		-	40	-	-	-	

Note (1) C_{PD} is the value of internal equivalent capacitance calculated from I_{CC} operation without load. Average operating current can be obtained by the following formula.

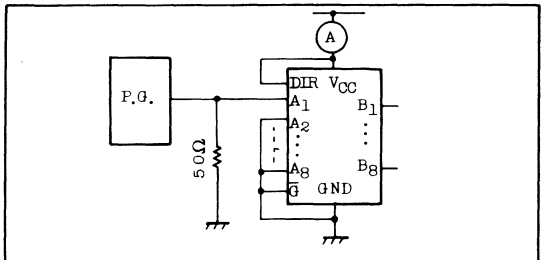
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) *: for TC74HC245 only.
**: for TC74HC640/643 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

TC74HCT245P/F·TC74HCT640P/F TC74HCT643P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

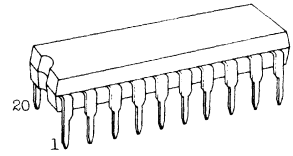
OCTAL BUS TRANCEIVER

TC74HCT245P/F 3-STATE, NON-INVERTING
TC74HCT640P/F 3-STATE, INVERTING
TC74HCT643P/F 3-STATE, INVERTING AND NON-INVERTING

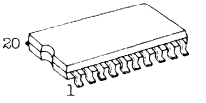
The TC74HCT245, TC74HCT640 and TC74HCT643 utilize silicon gate C^2MOS technology to achieve operating speed equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C^2MOS integrated circuit, it possesses the driving capability of 15 LSTTL loads.
The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS245/640/643



DIP20(3D20A-P)

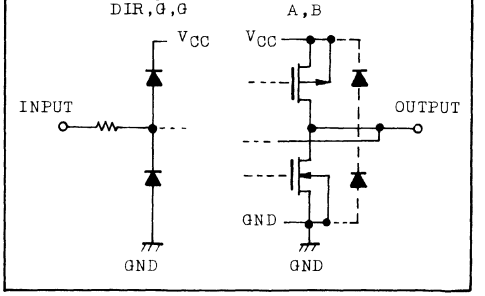


MFP20(F20GA-P)

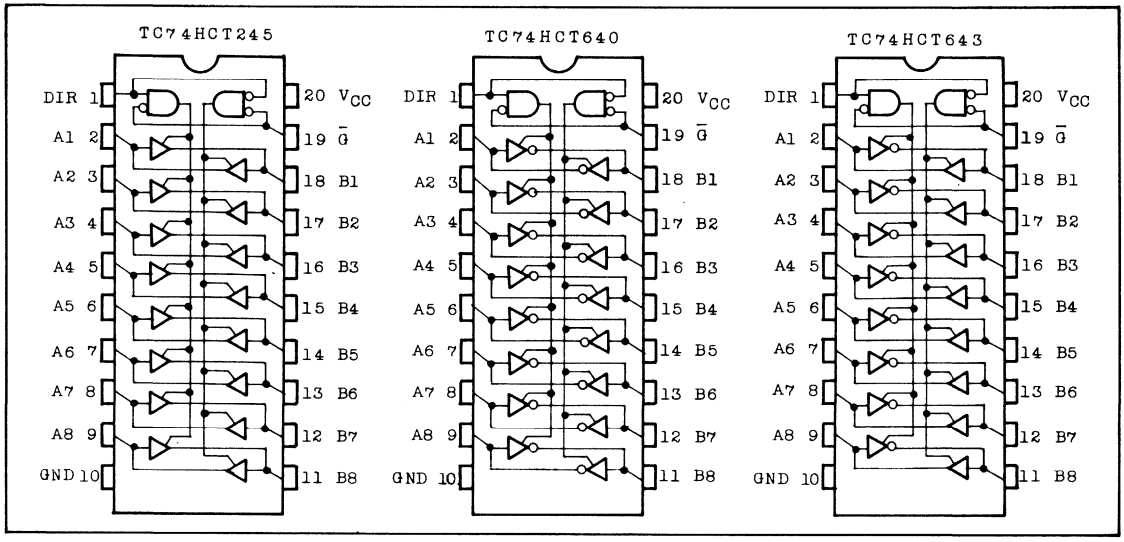
NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

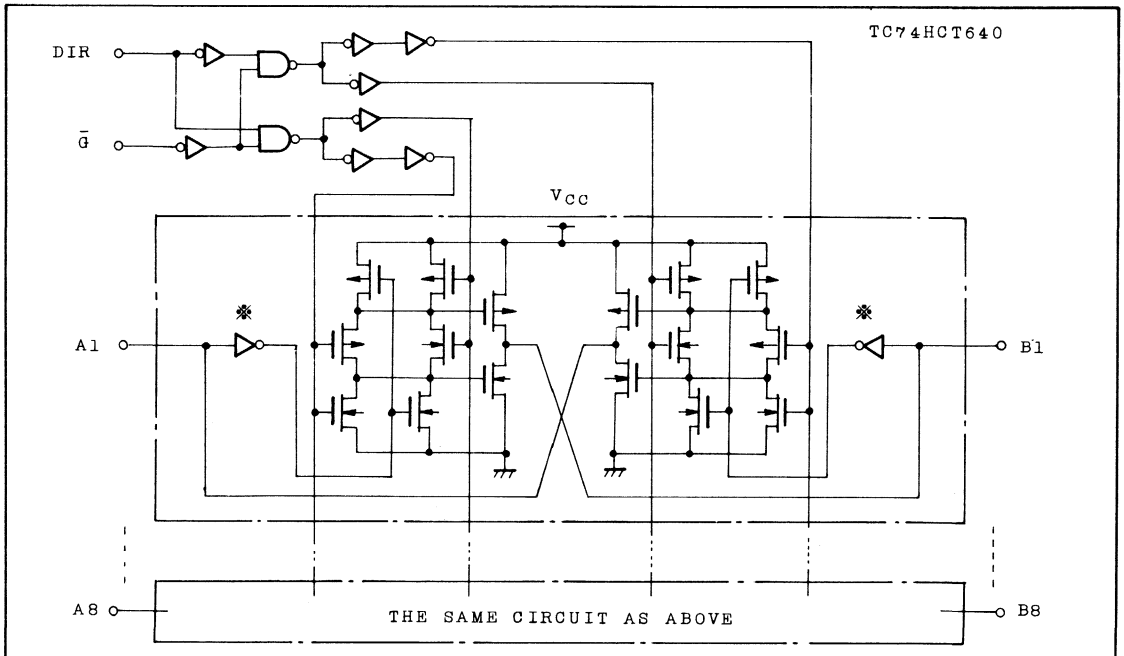
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT245P/F · TC74HCT640P/F TC74HCT643P/F



LOGIC DIAGRAM



Note: In case of TC74HCT245 or TC74HCT643, input inverters marked ※ at A bus and B bus or at B bus are eliminated respectively.

TC74HCT245P/F • TC74HCT640P/F TC74HCT643P/F

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HCT245	HCT640	HCT643
L	L	OUTPUT	INPUT	A = B	A = B	A = B
L	H	INPUT	OUTPUT	B = A	B = A	B = A
H	X	Z		Z	Z	Z

X: Don't Care

Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C, and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	°C

TC74HCT245P/F · TC74HCT640P/F TC74HCT643P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5	-	4.4	-	V
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.31	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	
	I_C	Per Input: $V_{IN}=0.5V$ or 2.4V Other Input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

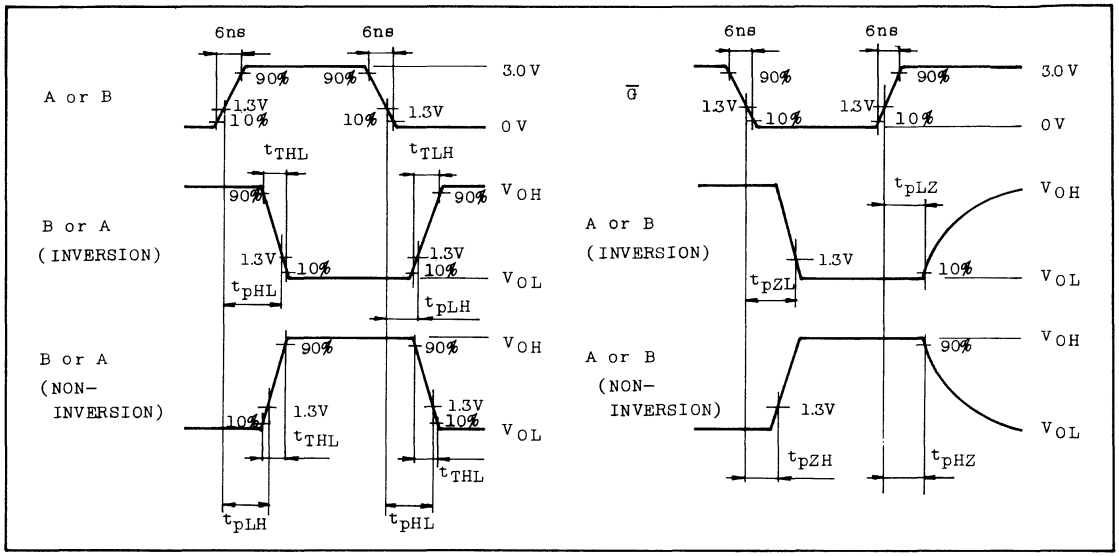
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	12	-	15	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	19	28	-	35	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	27	42	-	53	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	27	40	-	50	
Input Capacitance	C_{IN}	DIR, G, $\overline{G}$		-	5	10	-	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HCT245		-	46	-	-	-	
		TC74HCT640/643		-	44	-	-	-	

TC74HCT245P/F·TC74HCT640P/F TC74HCT643P/F

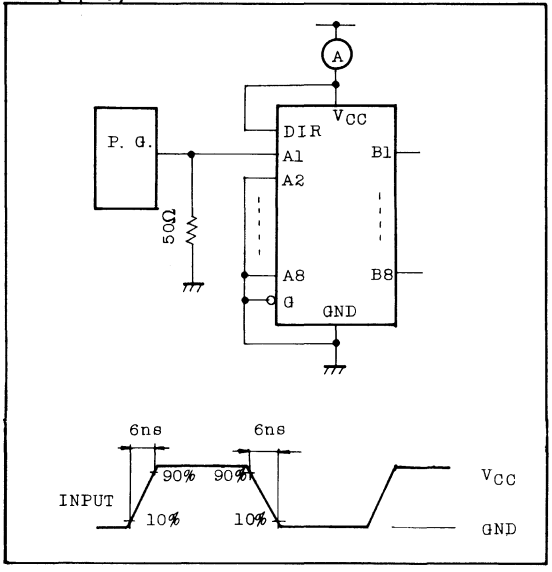
Note (1) C_{PD} is the value of internal equivalent capacitance calculated from I_{CC} operation without load. Average operating current can be obtained by the following formula.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

C²MOS DIGITAL INTEGRATED CIRCUIT

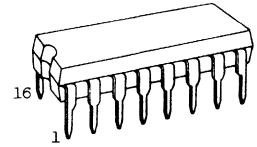
TC74HC251P/F

TC74HC251P/F 8-CHANNEL MULTIPLEXER (3-STATE)

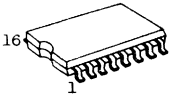
The TC74HC251 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. One of the eight data input signal (D0 ∿ D7) is selected by a three-bit address input (A, B, C) and the selected data will be provided on two outputs; a non-inverting output (Y) and a inverting output (W). When STROBE input is held high, both outputs become high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=19ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS251



DIP16(3D16A-P)



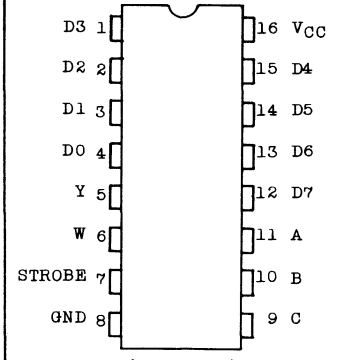
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC251P/F

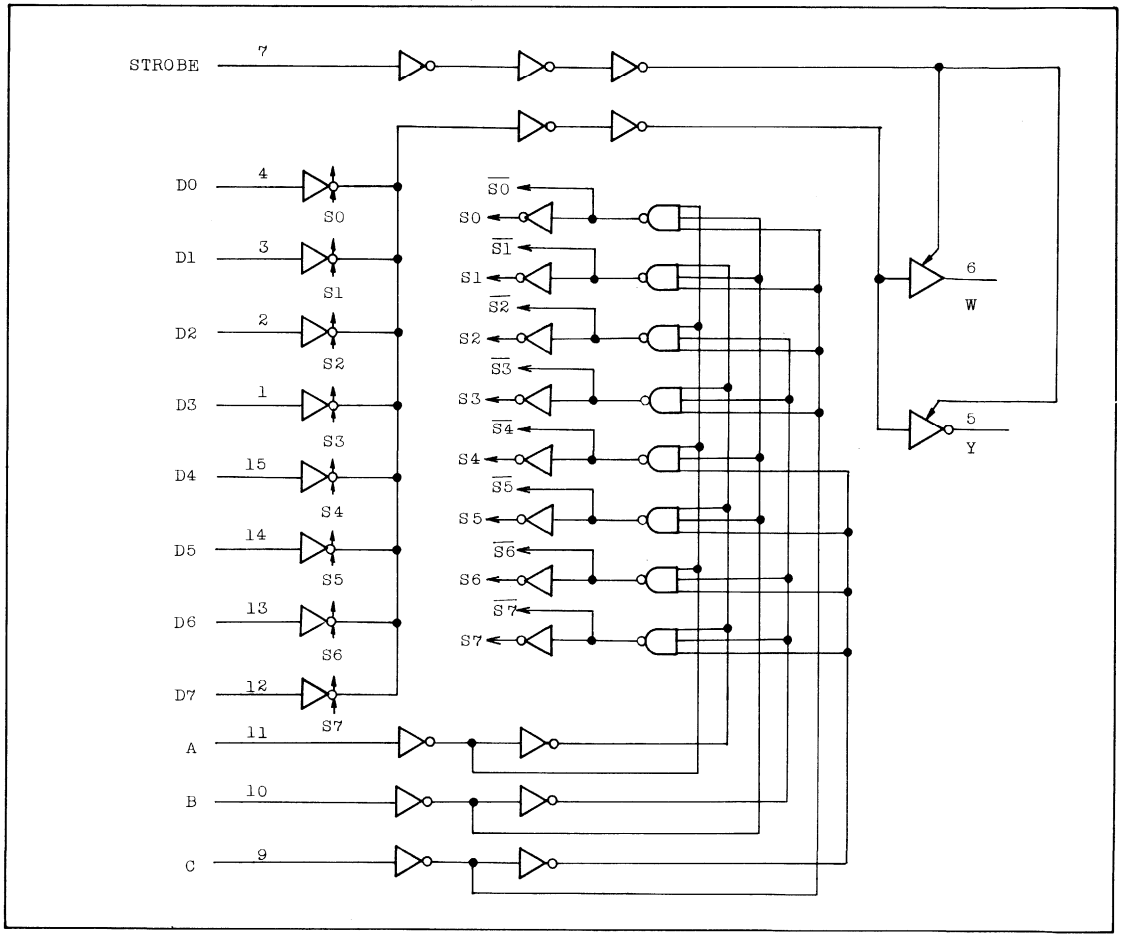
TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Z: HIGH IMPEDANCE

X: DON'T CARE

LOGIC DIAGRAM

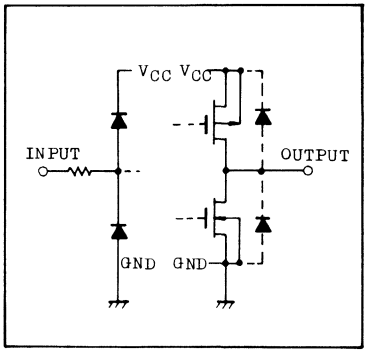


TC74HC251P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC251P/F

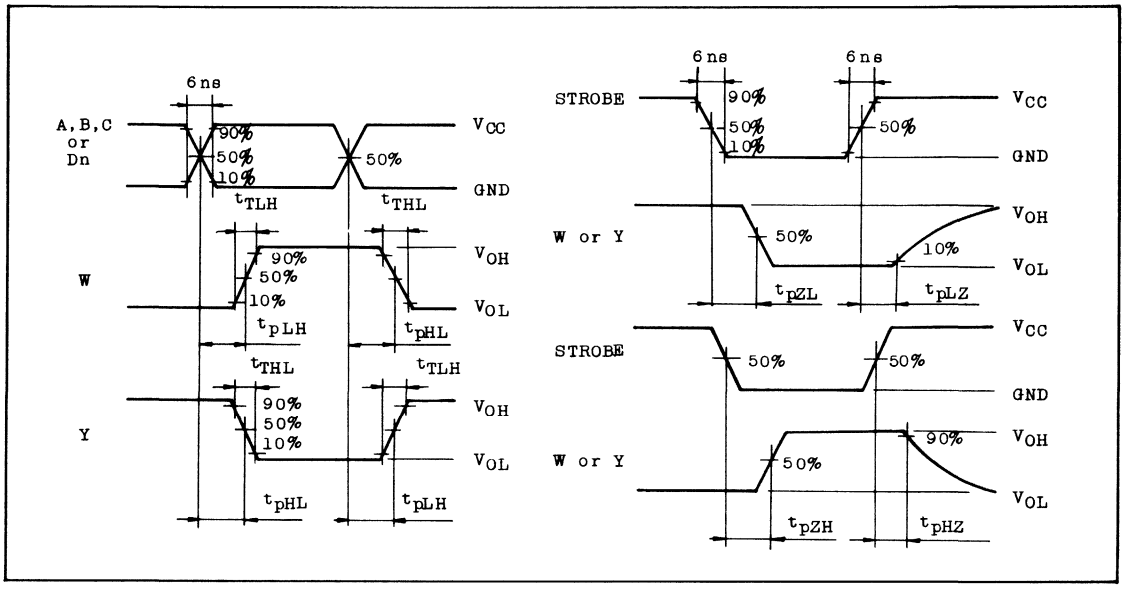
AC ELECTIRCAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (D - Y)	t_{pLH} t_{pHL}		2.0	-	76	160	-	200	
			4.5	-	19	32	-	40	
			6.0	-	16	27	-	34	
Propagation Delay Time (D - W)	t_{pLH} t_{pHL}		2.0	-	76	165	-	205	
			4.5	-	19	33	-	41	
			6.0	-	16	28	-	35	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	96	195	-	245	
			4.5	-	24	39	-	49	
			6.0	-	20	33	-	42	
Propagation Delay Time (D - W)	t_{pLH} t_{pHL}		2.0	-	96	205	-	255	
			4.5	-	24	41	-	51	
			6.0	-	20	35	-	43	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
3-State Output Enable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	60	105	-	130	
			4.5	-	15	21	-	26	
			6.0	-	13	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	100	-	-	-	

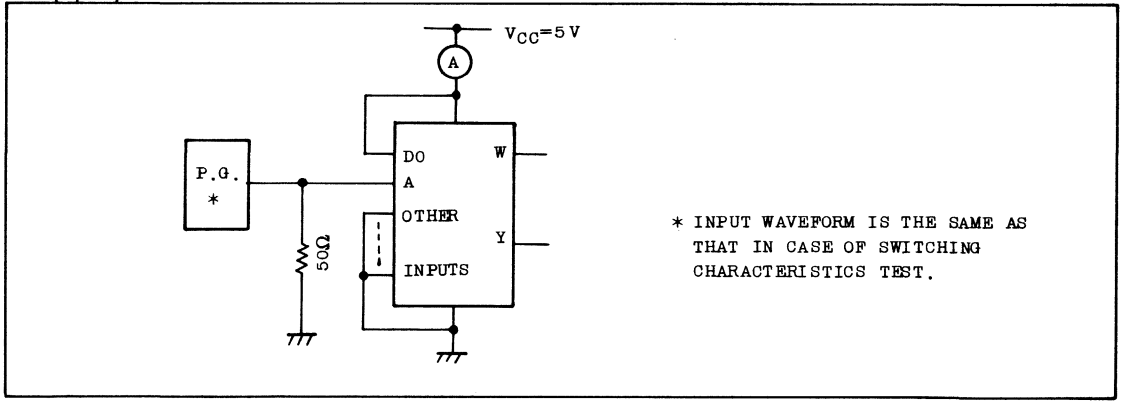
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC257P/F
TC74HC258P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

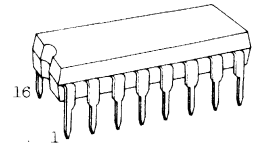
TC74HC257P/F QUAD 2-CHANNEL MULTIPLEXER (3-STATE)

TC74HC258P/F QUAD 2-CHANNEL MULTIPLEXER (3-STATE, INVERTING)

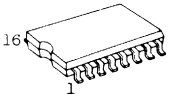
The TC74HC257 and the TC74HC258 are high speed CMOS MULTIPLEXER's fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These IC's are composed of independent 2-channel multiplexer with common SELECT and ENABLE INPUT.
The TC74HC258 is an inverting multiplexer while the TC74HC257 is a non-inverting multiplexer.
If ENABLE INPUT is held "H", outputs of both IC's become high-impedance state.
SELECT INPUT is held "L", A data is chosen, while "H", B data is chosen.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS257/258.



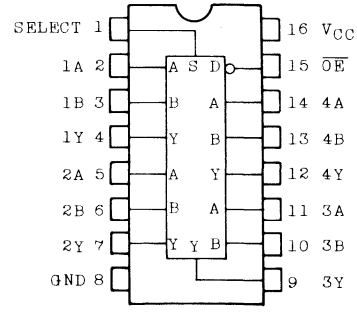
DIP16(3D16A-P)



MFP16(F16GC-P)

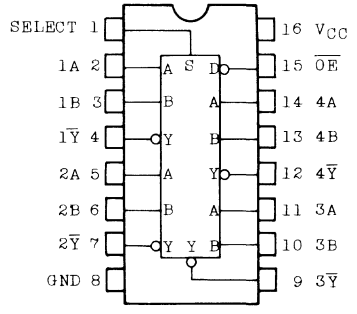
PIN ASSIGNMENT

TC74HC257



(TOP VIEW)

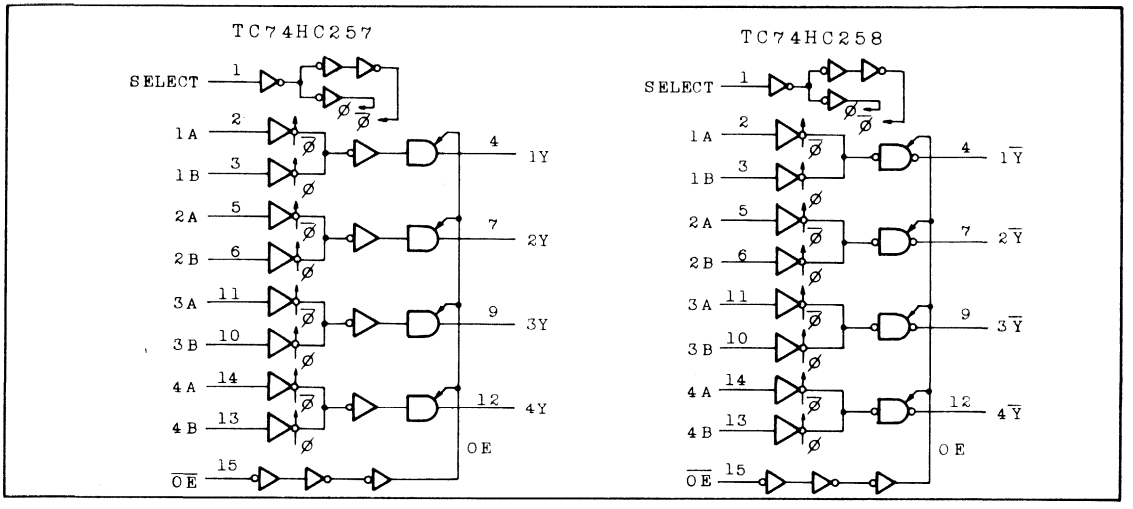
TC74HC258



(TOP VIEW)

TC74HC257P/F
TC74HC258P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y (257)	$\overline{Y}$ (258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't care

Z : High impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

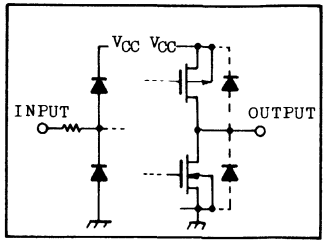
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC257P/F
TC74HC258P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

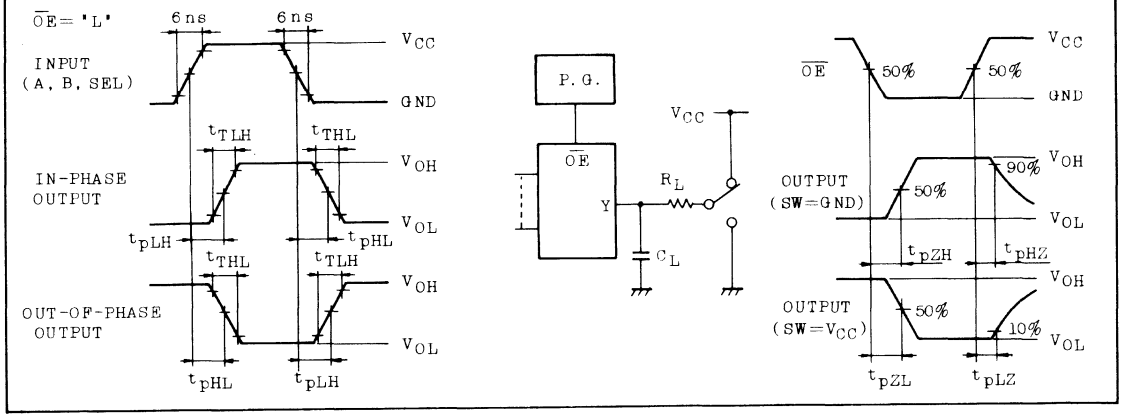
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
TC74HC257 Propagation Delay Time A,B - Y	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
SELECT -Y	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
TC74HC258 Propagation Delay Time A,B - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
SELECT - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	140	-	175	
			4.5	-	20	28	-	35	
			6.0	-	17	24	-	30	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC257		-	60	-	-	-	
		TC74HC258		-	59	-	-	-	

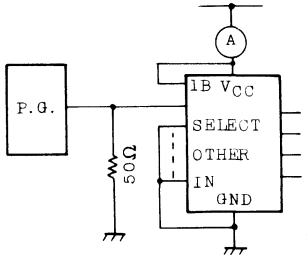
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\ f_{IN}+I_{CC}/4$ (per Channel)

TC74HC257P/F
TC74HC258P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

C²MOS DIGITAL INTEGRATED CIRCUIT

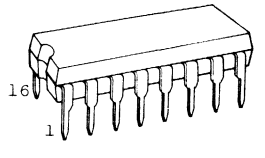
TC74HC259P/F

TC74HC259P/F 8-BIT ADDRESSABLE LATCH

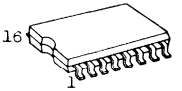
The TC74HC259 is a high speed CMOS 8-BIT ADDRESSABLE LATCH fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by A, B and C inputs. When $\overline{CLEAR}$ input is held "H" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "L" level, the data is written into the bit selected by A, B and C inputs, the other bits hold their previous conditions. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$($\overline{G}$) input held "H" level, write of all bits is inhibited regardless of A, B and C input, and their previous conditions are held. When $\overline{CLEAR}$ input is held "L" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "H" level, all bits are reset to "L" level regardless of the other inputs. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$ ($\overline{G}$) input held "L" level, all bits which isn't selected by A, B and C inputs are reset to "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS259



DIP16(3D16A-P)



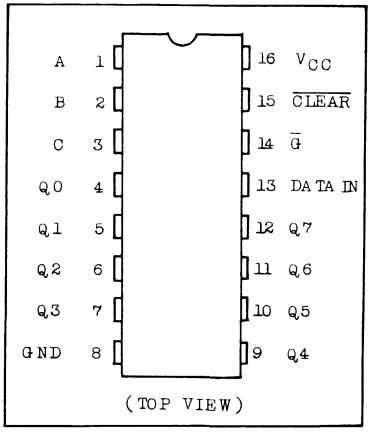
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC259P/F

TRUTH TABLE

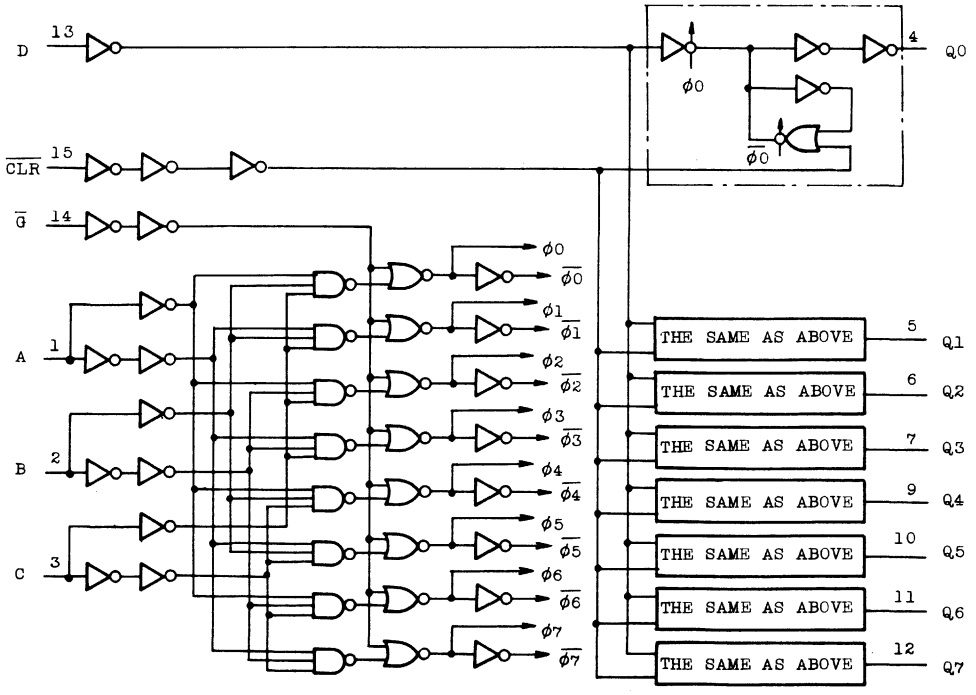
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO "L"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : THE LEVEL AT THE DATA INPUT

Q_{i0} : THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i=0,1,……,7).

LOGIC DIAGRAM

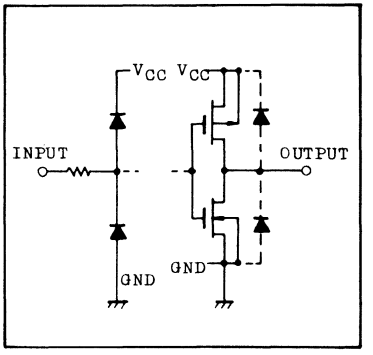


TC74HC259P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC259P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

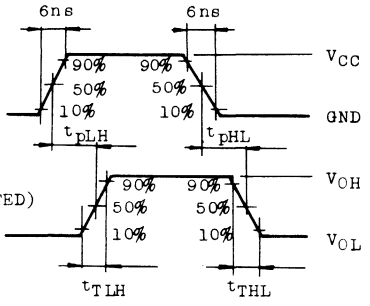
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (A, B, C - Q)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time ($\overline{G}$ - Q)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	15	23	-	29	
Minimum Pulse Width ($\overline{G}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (DATA)	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Hold Time (DATA)	t_h		2.0	-	10	25	-	30	
			4.5	-	2	5	-	6	
			6.0	-	2	5	-	5	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	32	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

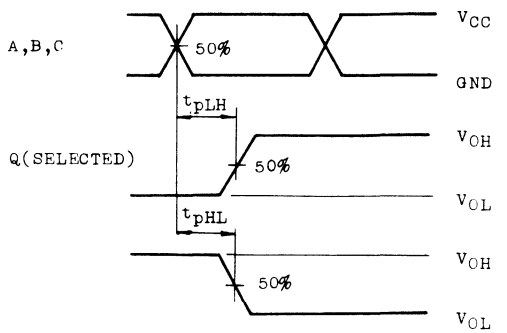
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

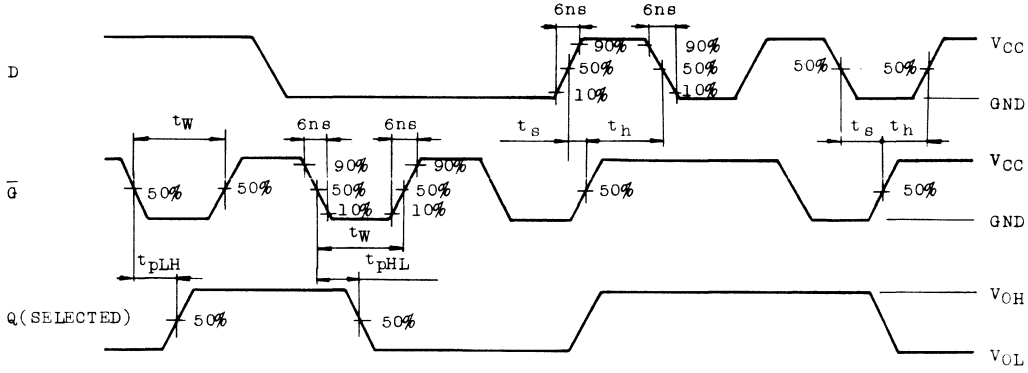
WAVEFORM 1. ($\overline{G}$=L, $\overline{CLR}$=H, A~C=STABLE)



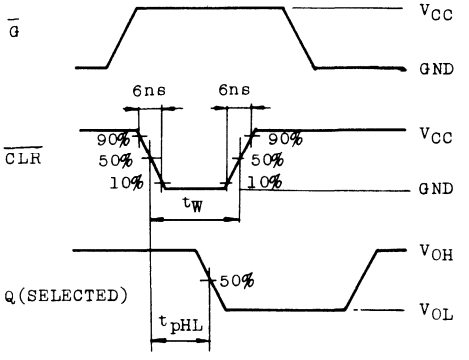
WAVEFORM 2. ($\overline{G}$=L)



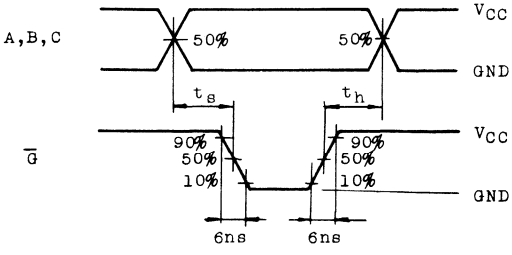
WAVEFORM 3. ($\overline{CLR}$=H, A~C=STABLE)



WAVEFORM 4. (D=H, A~C=STABLE)

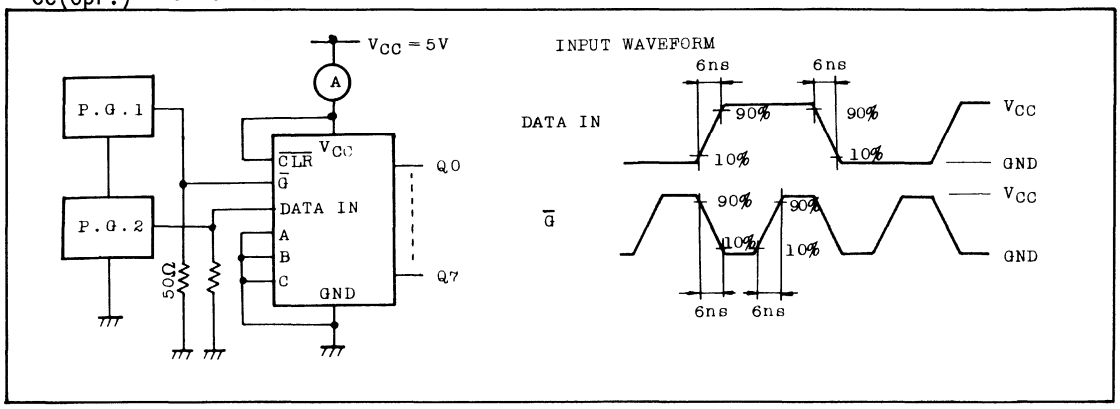


WAVEFORM 5. ($\overline{CLR}$=H)



TC74HC259P/F

$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC273P/F

TC74HC273P/F OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achives the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

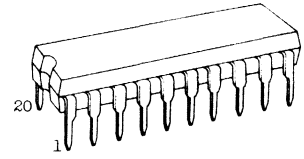
Information signals applied to D inputs are transfered to the Q outputs on the positive-going edge of the clock pulse.

When the $\overline{\text{CLEAR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

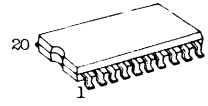
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=48MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS273

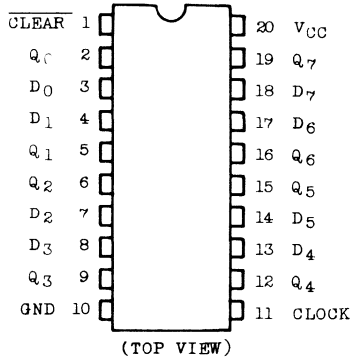


DIP20(3D20A-P)



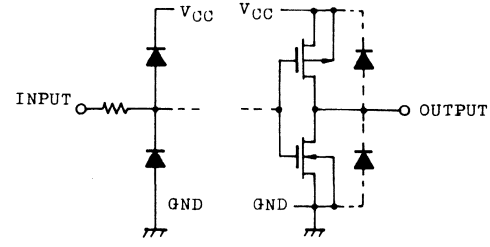
MFP20(F20GA-P)

PIN ASSIGNMENT



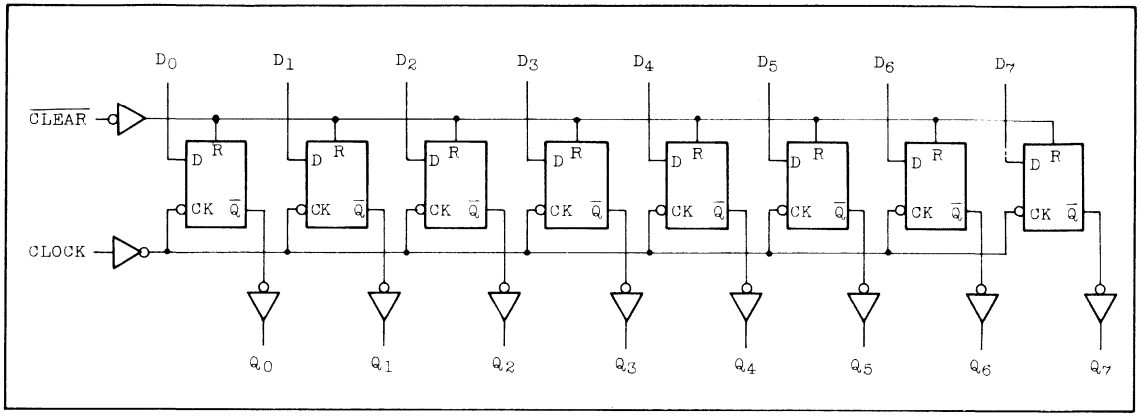
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC273P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	-
H	H	↑	H	-
H	X	↓	Qn	No change

X: Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=60°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC273P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time $\overline{\text{CLEAR}}$ - Q	t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	44	-	22	-	
			6.0	32	52	-	26	-	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width $\overline{\text{CLEAR}}$	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{\text{CLEAR}}$	t_{rem}		2.0	-	15	75	-	95	
			4.5	-	4	15	-	19	
			6.0	-	3	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	53	-	-	-	

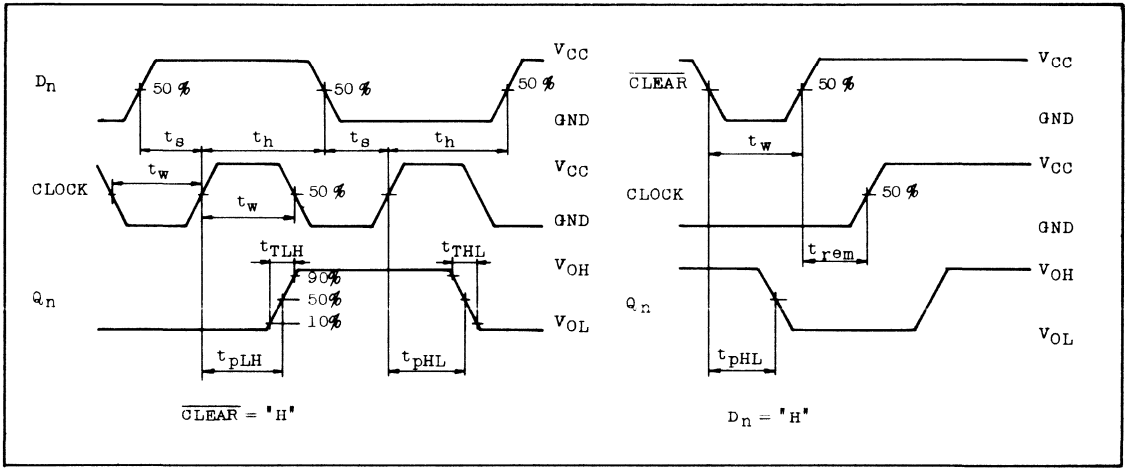
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Flip Flop)}$$

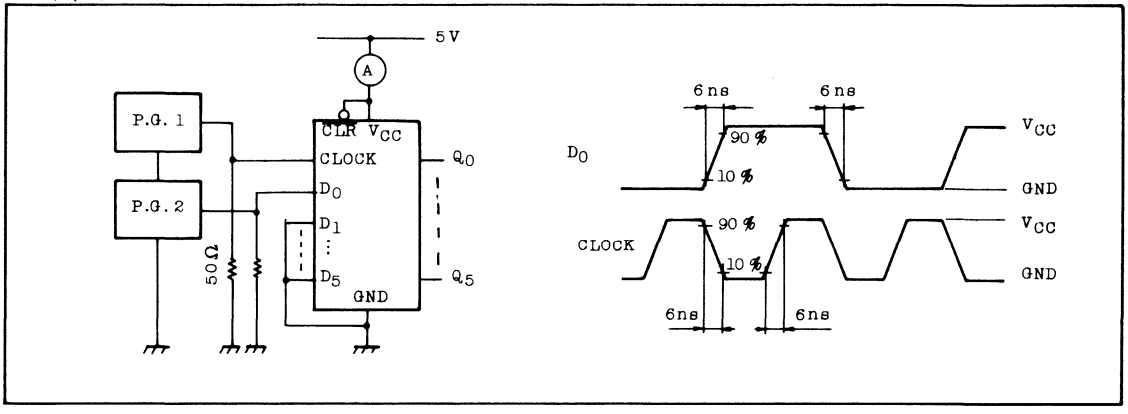
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD(total)} = 38 + 15 \cdot n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC279P/F

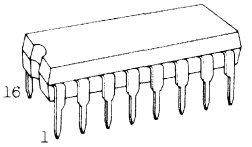
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC279P/F QUAD S-R LATCH

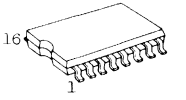
The TC74HC279 is a high speed CMOS QUAD S-R LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Each latch has an independent Q output and set and reset inputs. $\overline{S}$ and $\overline{R}$ are accomplished by "L" level. When $\overline{S}$ input is placed at "L", Q output becomes "H" and when $\overline{R}$ input is placed at "L", Q output becomes "L". When both of $\overline{S}$ and $\overline{R}$ are placed at "L", $\overline{S}$ takes precedence resulting Q="H" and when both of $\overline{S}$ and $\overline{R}$ are placed at "H", Q output doesn't change.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{PLH}\fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS279



DIP16(3D16A-P)



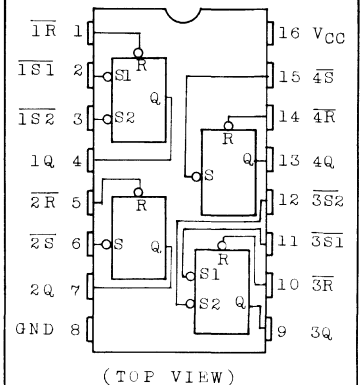
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC279P/F

TRUTH TABLE

INPUTS		OUTPUT
$\overline{S}$ #	$\overline{R}$	Q
H	H	Q0
L	H	H
H	L	L
L	L	H

NOTE :

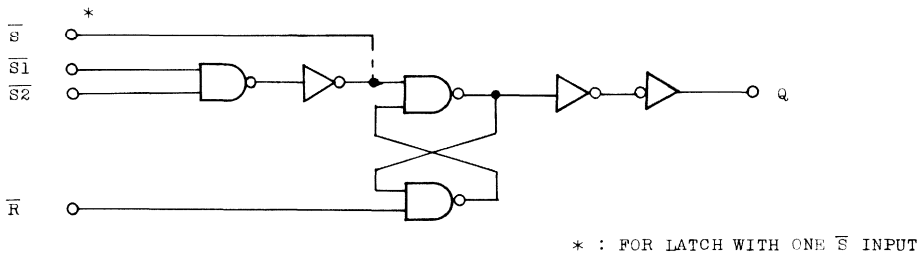
Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:

H = BOTH $\overline{S}$ INPUTS HIGH

L = ONE OF BOTH INPUTS LOW

LOGIC DIAGRAM (Per Circuit)

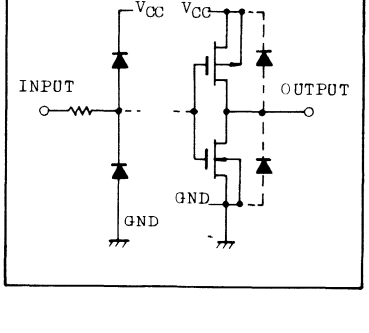


* : FOR LATCH WITH ONE $\overline{S}$ INPUT

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC279P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{S1}$, $\overline{S2}$ - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{S}$ - Q)	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Delay Time ($\overline{R}$ - Q)	t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	

TC74HC279P/F

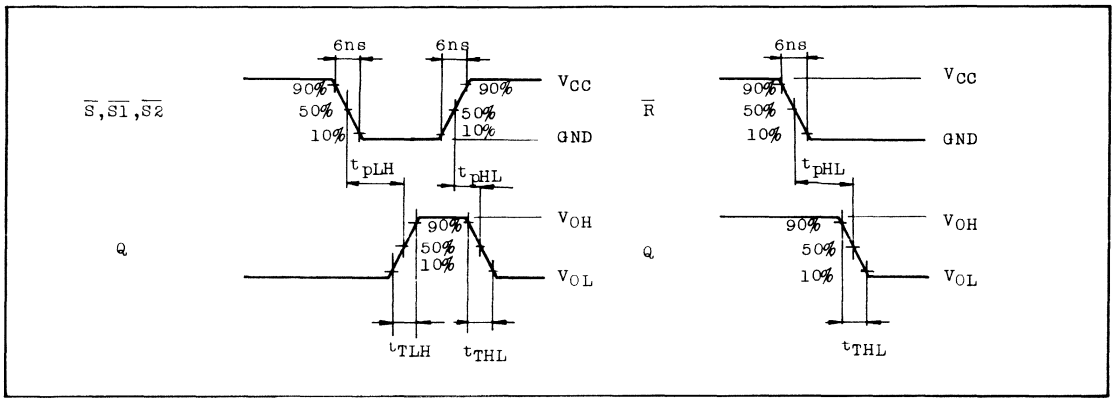
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	26	-	-	-	

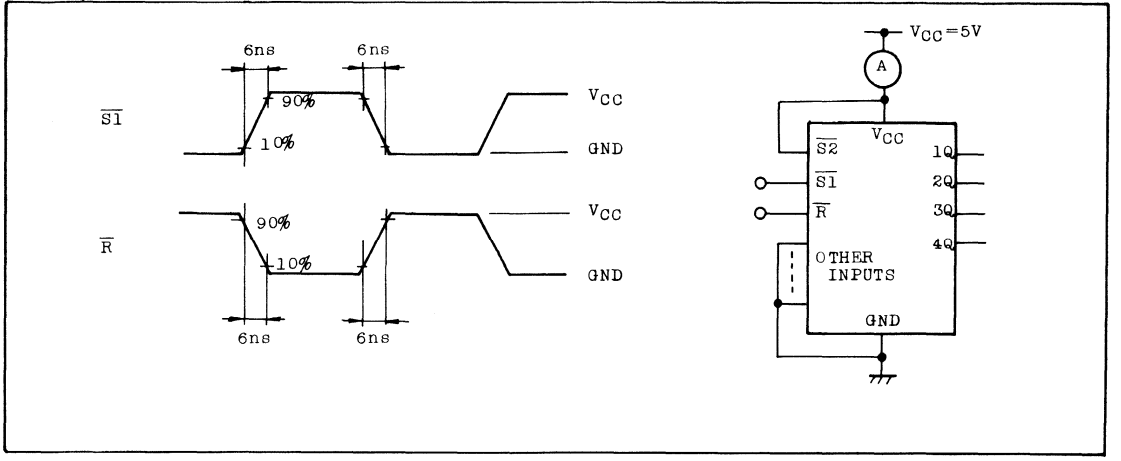
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC280P/F

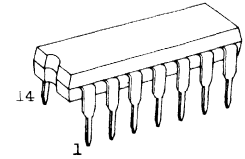
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC280P/F 9-BIT PARITY GENERATOR/CHECKER

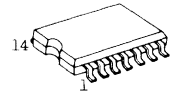
TheTC74HC280 is a high speed CMOS 9-BIT PARITY GENERATOR fabricated with silicon gate CMOS technology.
It acieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of nine data inputs (A thru I) and odd/even parity outputs (Σ ODD and Σ EVEN).
The nine input data control the output conditions.
When the number of high level inputs is odd, ΣODD output is kept high and ΣEVEN output low. On the contary, when the number is ven, ΣEVEN output is kept high and ΣODD low.
This IC facilitates operation of either odd or even aprity application.
The word-length capability is easily expanded by cascading.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=25ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{HIL}=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}=t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS280



DIP14(3D14A-P)



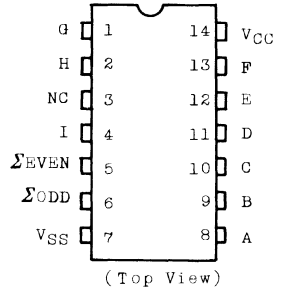
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Dicde Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

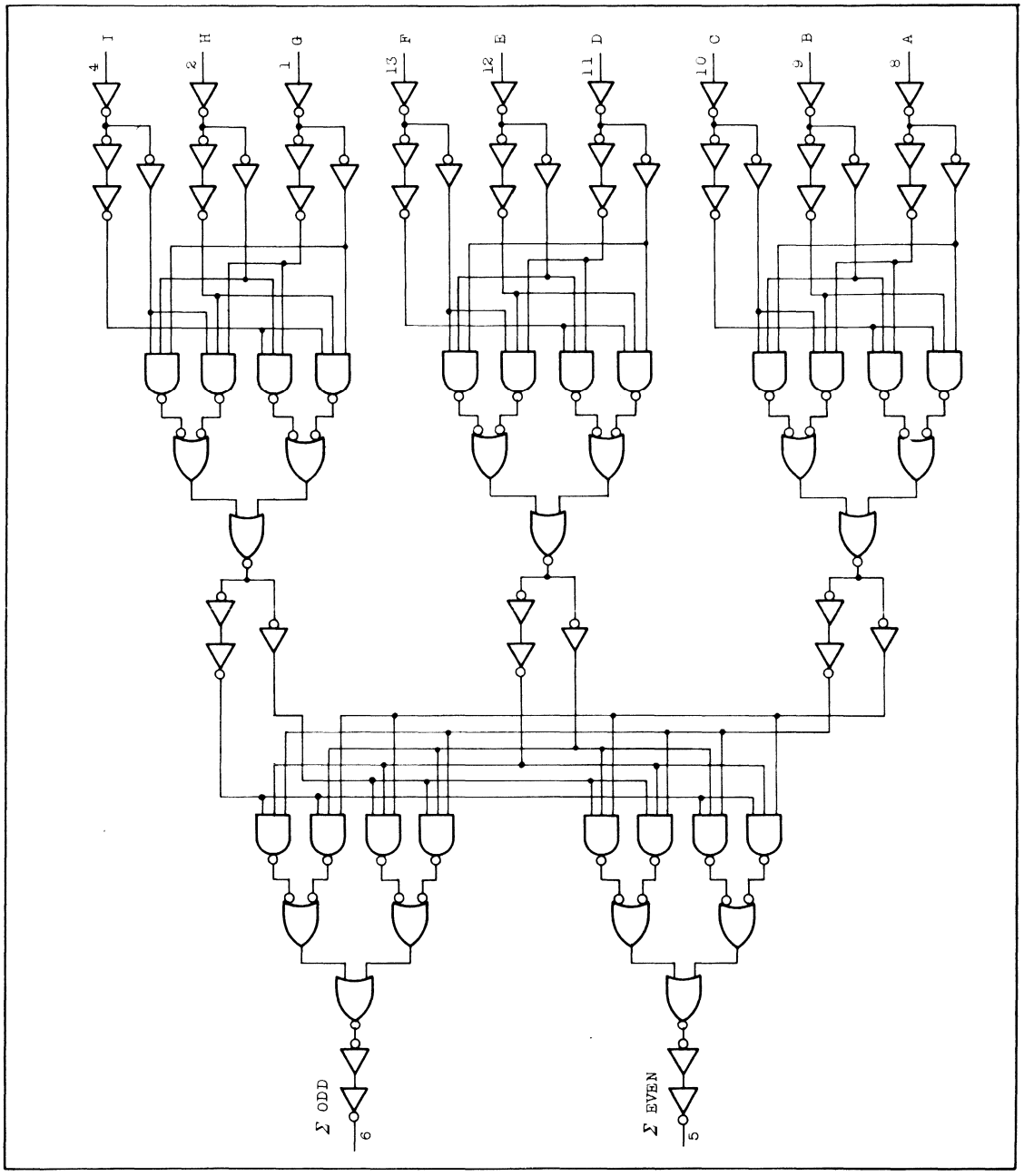


NC : No Connection

TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUT	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

LOGIC DIAGRAM



TC74HC280P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

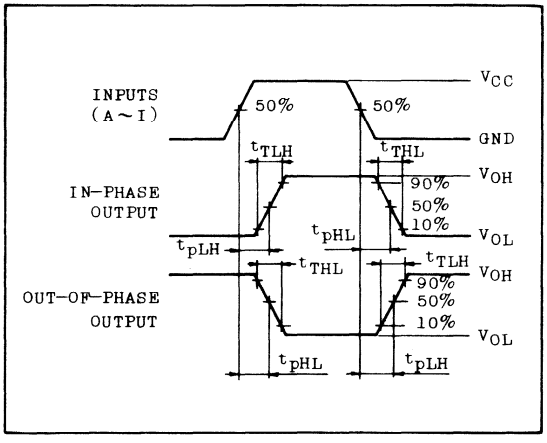
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

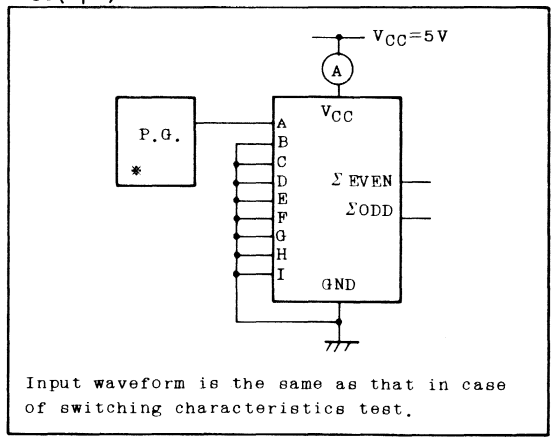
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	124	235	-	295	ns
			4.5	-	31	47	-	59	
			6.0	-	26	40	-	50	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	110	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC283P/F

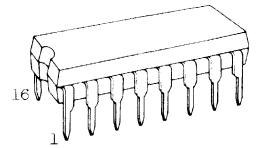
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC283P/F 4-BIT BINARY FULL ADDER

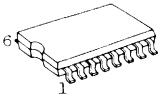
The TC74HC283 is a high speed CMOS 4-BIT BINARY FULL ADDER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit. This adder features full internal look a head across all four bits. 4 × n bit binary adder is easily built up by cascading without any additional logic. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Ouptut Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS283



DIP16(3D16A-P)



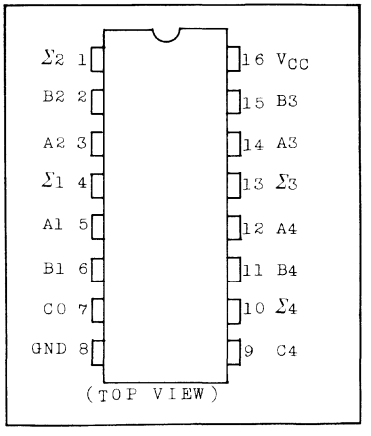
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

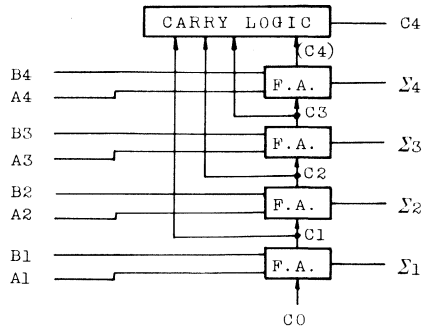


TC74HC283P/F

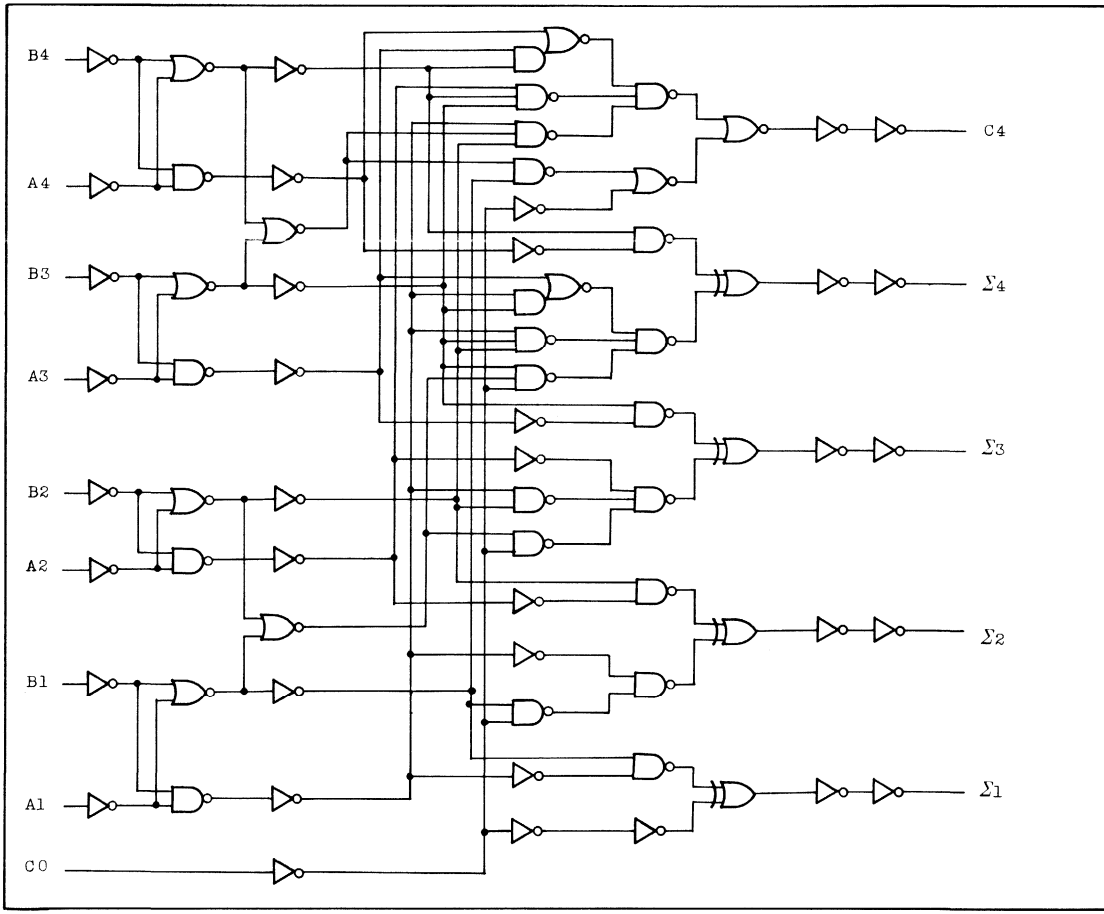
TRUTH TABLE (1 bit)

INPUTS			OUTPUTS	
Bn	An	Cn-1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

BLOCK DIAGRAM



LOGIC DIAGRAM

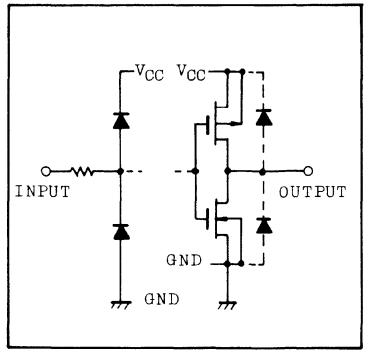


TC74HC283P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC283P/F

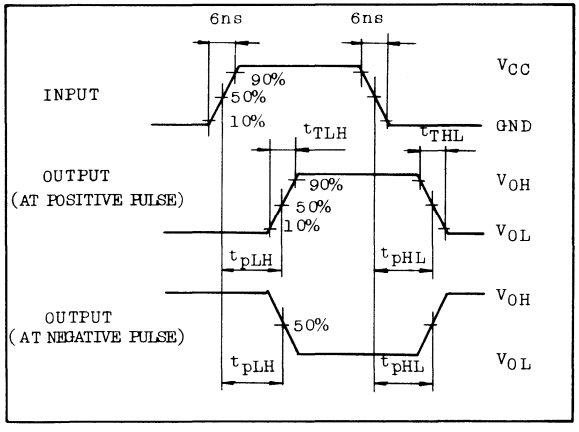
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (Co - Σn)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (Co - C4)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay time (An, Bn - Σn)	t_{pLH} t_{pHL}		2.0	-	140	270	-	340	
			4.5	-	35	54	-	68	
			6.0	-	30	46	-	58	
Propagation Delay Time (An, Bn - C4)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	114	-	-	-	

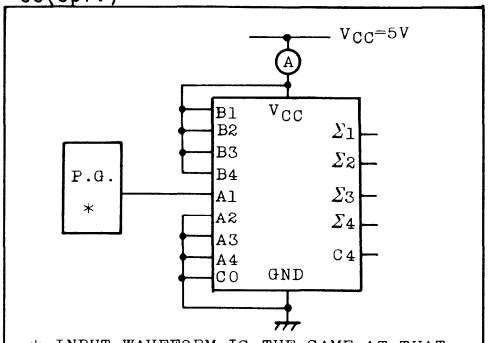
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AT THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC298P/F

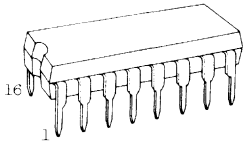
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC298P/F QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

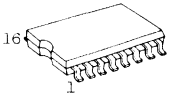
The TC74HC298 is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contains a 4 bit 2-channel multiplexer and a 4-bit output register. When the word-select input (W.S.) is held low, word 1 (A1, B1, C1, D1) input data is selected and is applied to the registers. On the other hand W.S. is held high, word 2 (A2, B2, C2, D2) input data will be applied to the registers. This selected data is transfered to the output terminals (Q_A, Q_B, Q_C, Q_D) on the negative-going transition of the clock pulse ($\overline{CLOCK}$).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS298



DIP16(3D16A-P)



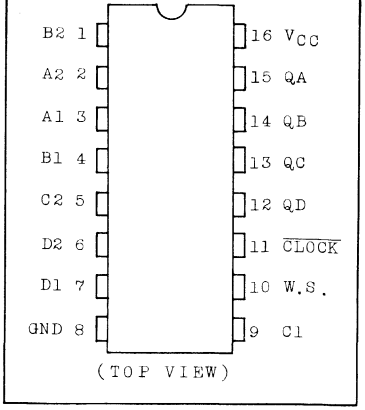
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

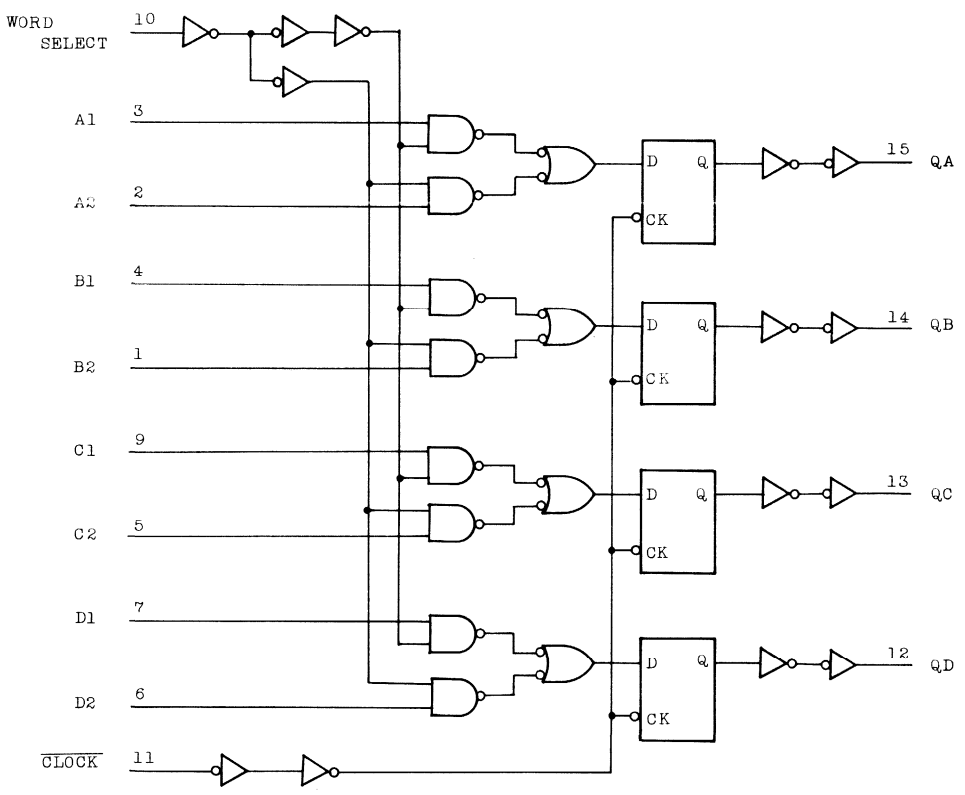
TC74HC298P/F

TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CLOCK}$	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QC0	QD0

X : DON'T CARE(INCLUDING TRANSITION)
a1,a2, ETC. : THE LEVEL OF STEADY-STATE INPUT AT A1,A2,ETC.
QA0,QB0,ETC. : THE LEVEL OF QA,QB,ETC. ENTERED ON THE MOST RECENT NEGATIVE TRANSITION OF THE CLOCK INPUT.

LOGIC DIAGRAM

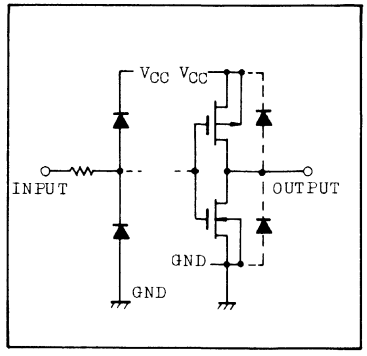


TC74HC298P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
($\overline{CLOCK}$ - Q)	t_{pHL}		6.0	-	15	24	-	30	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
($\overline{CLOCK}$)	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
(A, B, C, D)			6.0	-	2	9	-	11	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
(W.S.)			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
(A, B, C, D, W.S.)			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

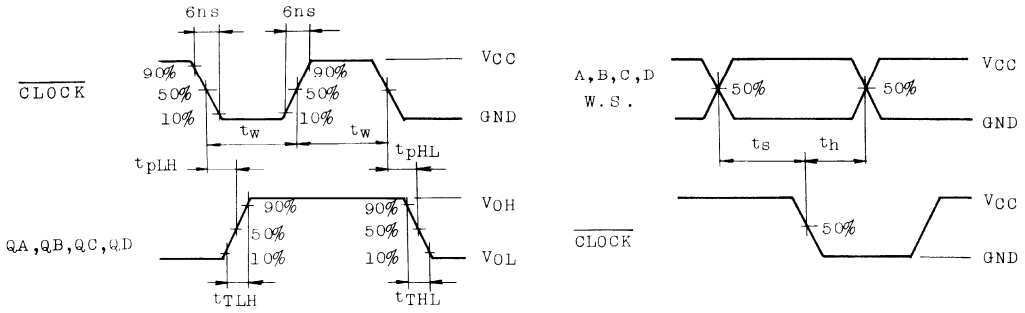
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

And the C_{PD} for the operating n-bit can be obtained by the following equation.

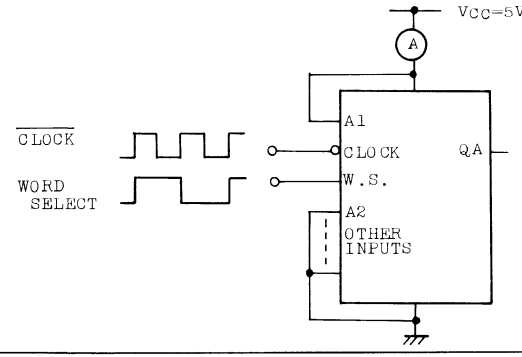
$$C_{PD} = 32 + n \cdot 15$$

TC74HC298P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



TRANSITION TIME AND V_{IH}, VIL OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC299P
TC74HC323P

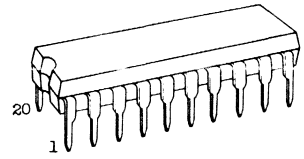
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC299P 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
TC74HC323P 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

The TC74HC299 and TC74HC323 is a high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This device has four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected. Clear function on the TC74HC299 is asynchronous to CLOCK, while the TC74HC323 is cleared synchronous to clock.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=35MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....
  $|I_{OH}|=I_{OL}$=6mA(Min.) For QA ∿ QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QA', QH'
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS299



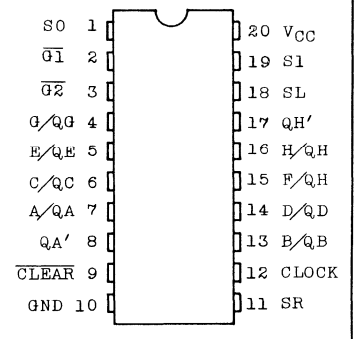
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC299P
TC74HC323P

TRUTH TABLE

MODE	INPUTS								INPUTS/OUTPUTS		OUTPUTS	
	$\overline{CLEAR}$	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *	(299)(323)	SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X ↓	X	X	L	L	L	L
	L	X	L	L	L	X ↓	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓	X	H	H	QGn	H	QGn
	H	L	H	L	L	↓	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓	H	X	QBn	H	QBn	H
	H	H	L	L	L	↓	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↓	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Z : High Impedance

Qno: The level of An before the indicated steady-state input conditions were established.

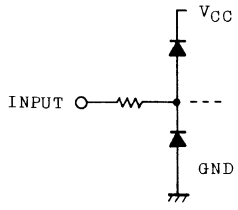
Qnn: The level of Qn before the most recent active transition indicated by ↓ or ↑.

a,h: The level of the steady-state inputs A, H, respectively.

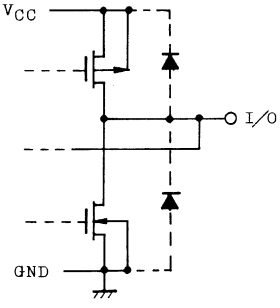
X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT

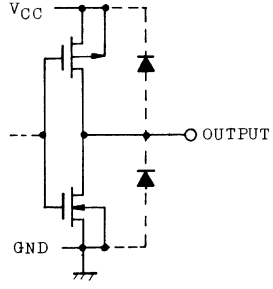
CLEAR, CLOCK
S0, S1, $\overline{G1}$, $\overline{G2}$,
SR, SL



A/QA ····· H/QH

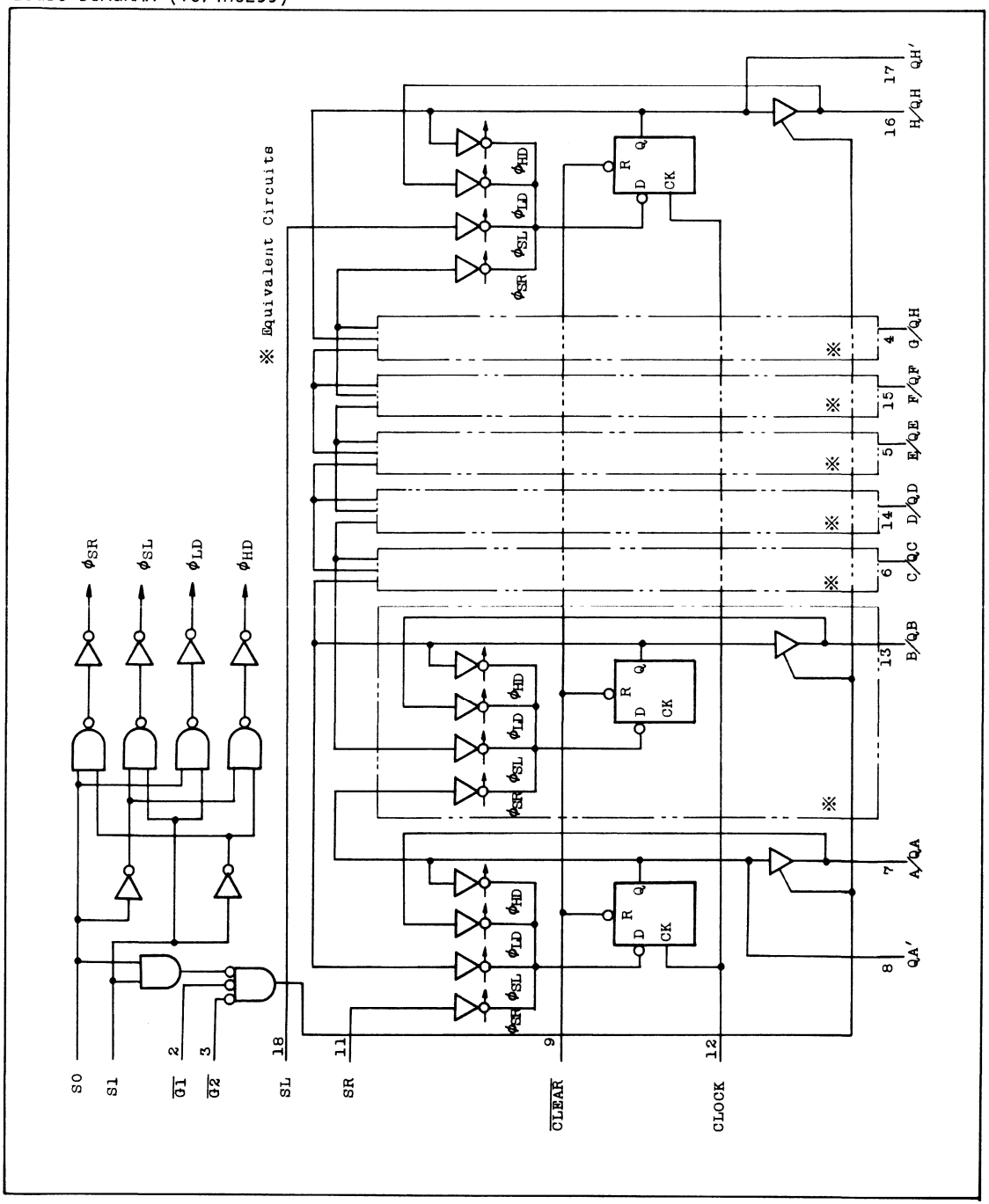


QA', QH'



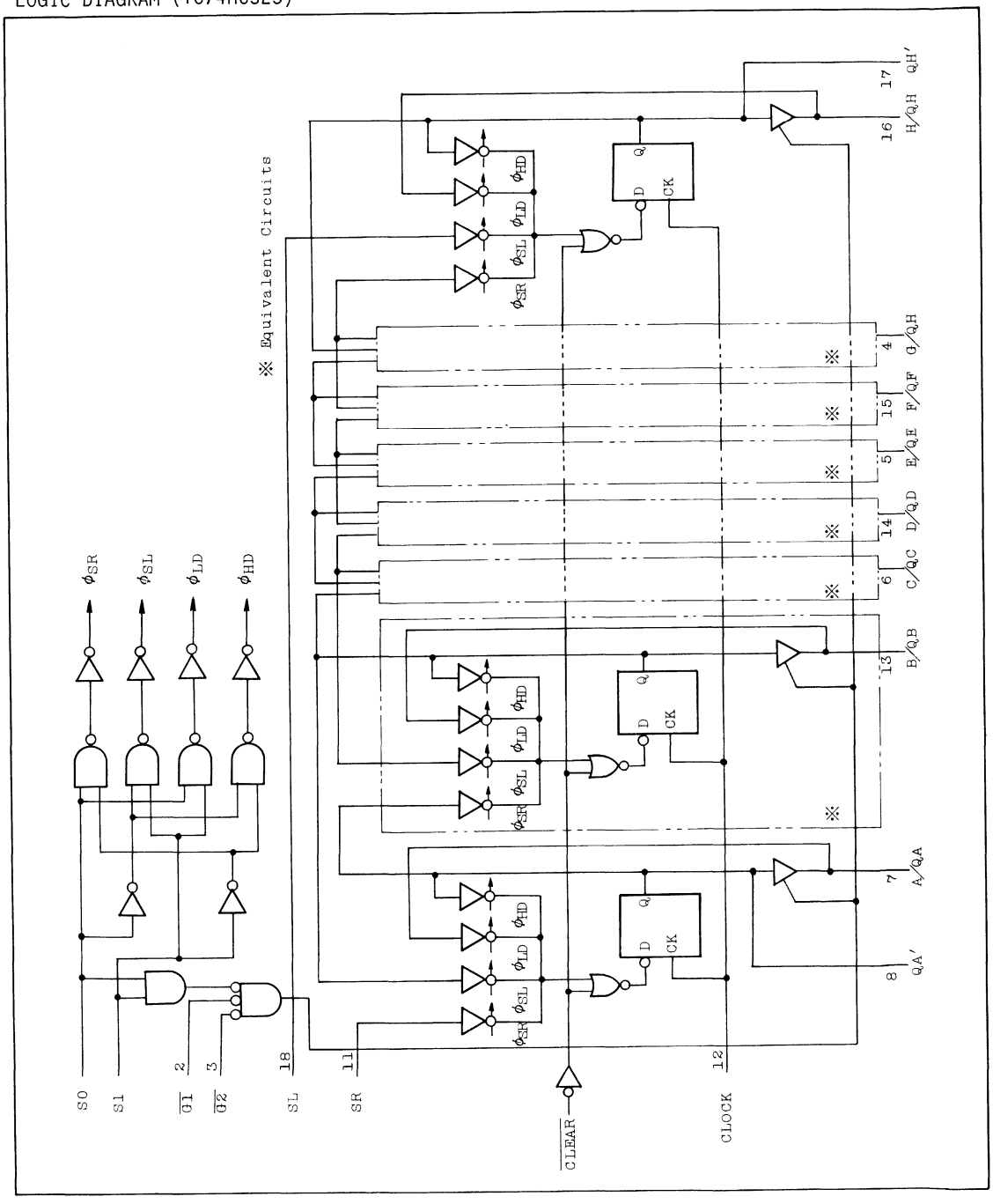
TC74HC299P
TC74HC323P

LOGIC DIAGRAM (TC74HC299)



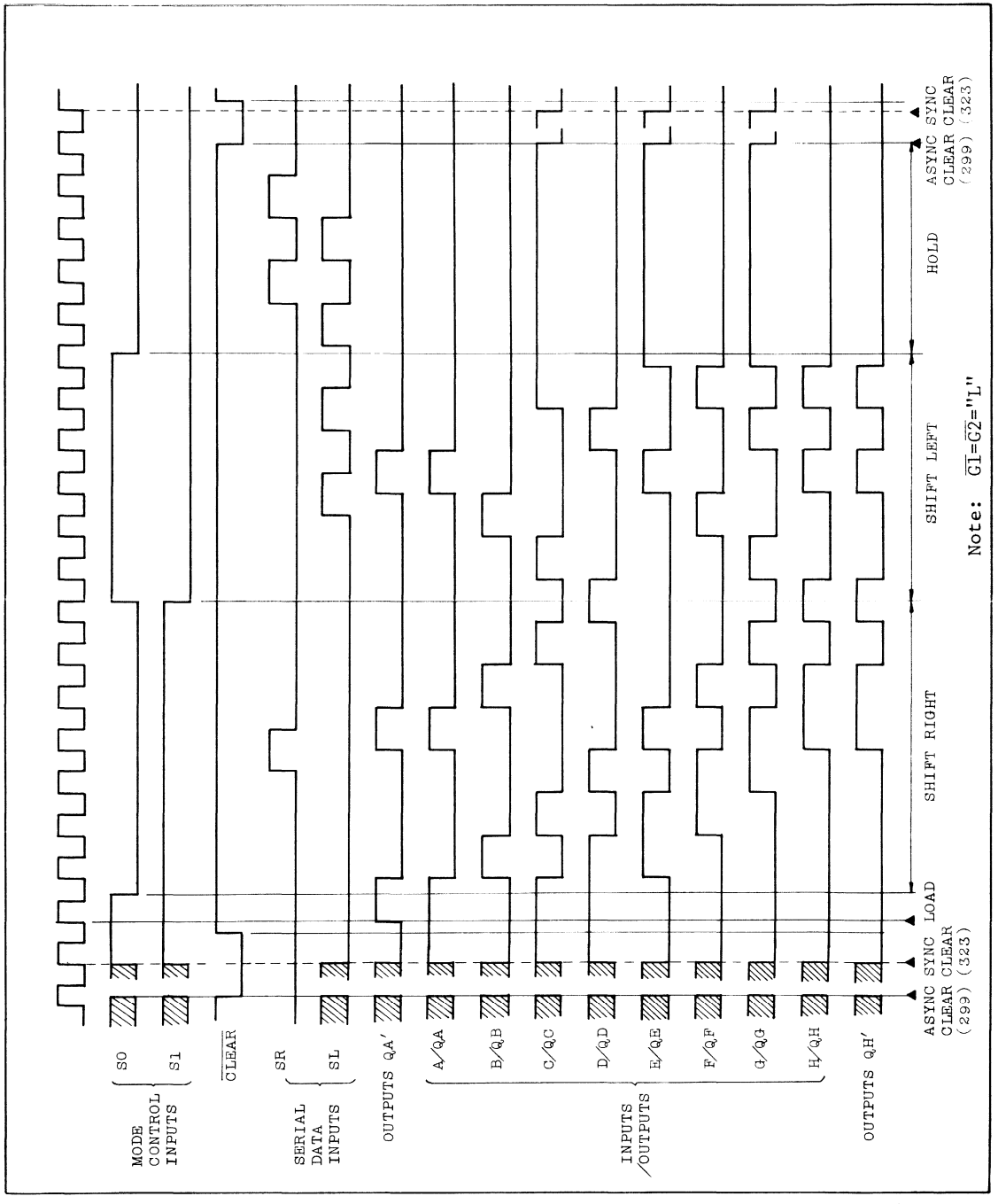
TC74HC299P
TC74HC323P

LOGIC DIAGRAM (TC74HC323)



TC74HC299P
TC74HC323P

TIMING CHART



TC74HC299P
TC74HC323P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Q_A ∿ Q_H	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		Q_A', Q_H'	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		Q_A ∿ Q_H	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		Q_A', Q_H'	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC299P
TC74HC323P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (QA∿QH)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (QA', QH')	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - QA∿QH)	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (CLOCK - QA', QH')	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time ($\overline{CLEAR}$ - QA∿QH) *	t_{pHL}		2.0	-	116	230	-	290	
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Propagation Delay Time ($\overline{CLEAR}$ - QA', QH') *	t_{pHL}		2.0	-	116	230	-	290	
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	33	-	16	-	
			6.0	24	39	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Minimum Set-up Time (SL, SR, A∿H)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set-up Time (S0, S1)	t_s		2.0	-	50	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
Minimum Set-up time ($\overline{CLEAR}$) **	t_s		2.0	-	32	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

TC74HC299P
TC74HC323P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Hold Time (SL, SR, A∿H)	t_h		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time (S0, S1)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time ($\overline{CLEAR}$) **	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLEAR}$)*	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	112	200	-	250	
			4.5	-	28	40	-	50	
			6.0	-	24	34	-	43	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance (QA∿QH)	C_{OUT}			-	13	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	221	-	-	-	

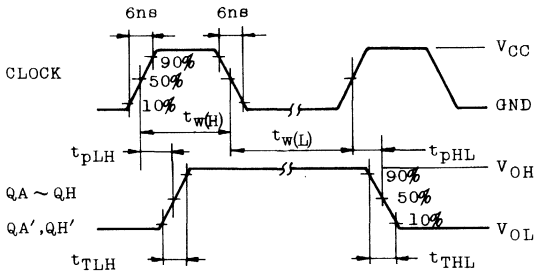
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

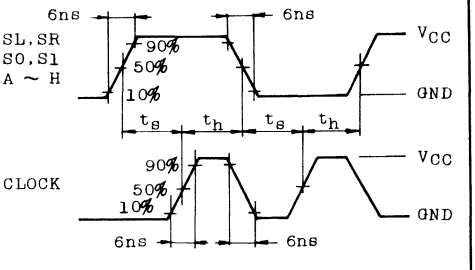
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2): * Apply to TC74HC299

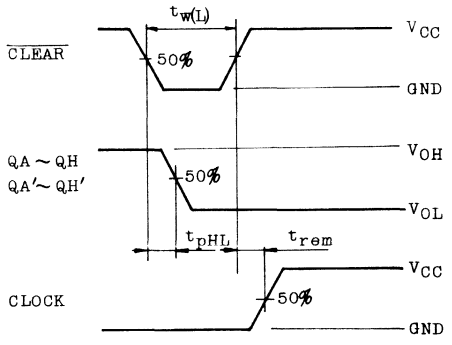
** Apply to TC74HC323

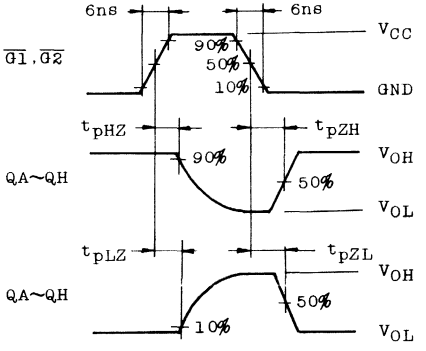
SWITCHING CHARACTERISTICS TEST WAVEFORM



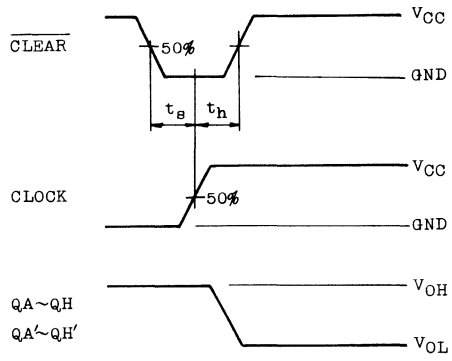


TC74HC299



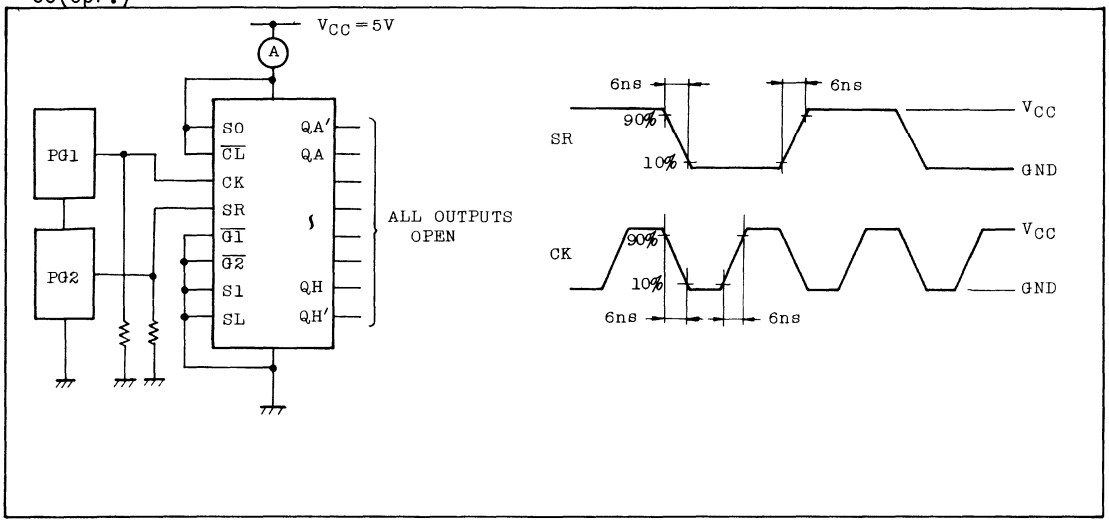


TC74HC323



TC74HC299P
TC74HC323P

$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

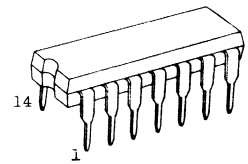
TC74HC354P/F

TC74HC354P/F 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

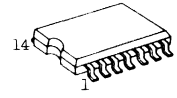
The TC74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC354 is similar in function to TC74HC356, which has a 8-bit flip-flop as the data registers instead of 8-bit latch. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=33ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS354



DIP14(3D14A-P)



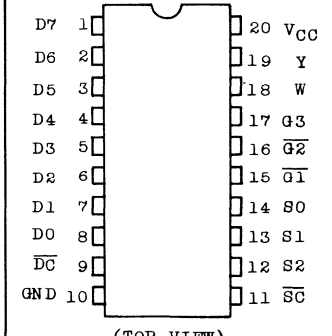
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC354P/F

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	$\overline{DC}$	G1	G2	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z : HIGH IMPEDANCE

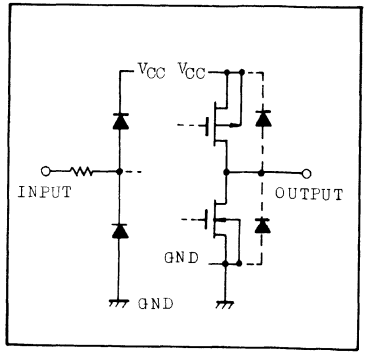
D0n·····D7n : THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7 ,RESPECTIVELY, BEFORE THE MOST RECENT LOW-TO-HIGH TRANSITION OF DATA CONTROL.

: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW.

RECOMMENDED OPERATING CONDITIONS

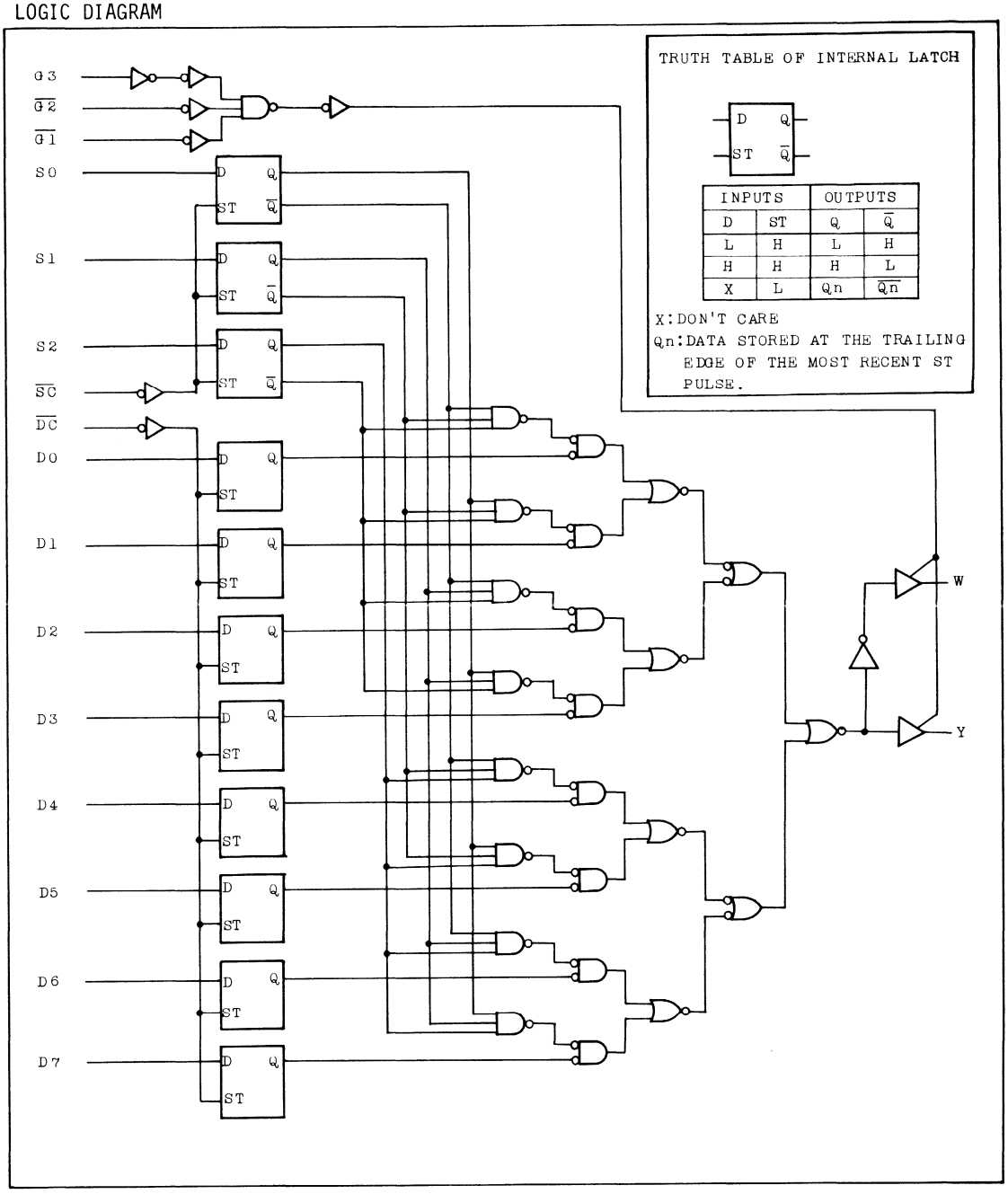
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC354P/F

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TC74HC354P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-7.8mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=7.8mA$	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (Dn - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time ($\overline{DC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	

AC ELECTRICAL CHARACTERISTICS (Continued)

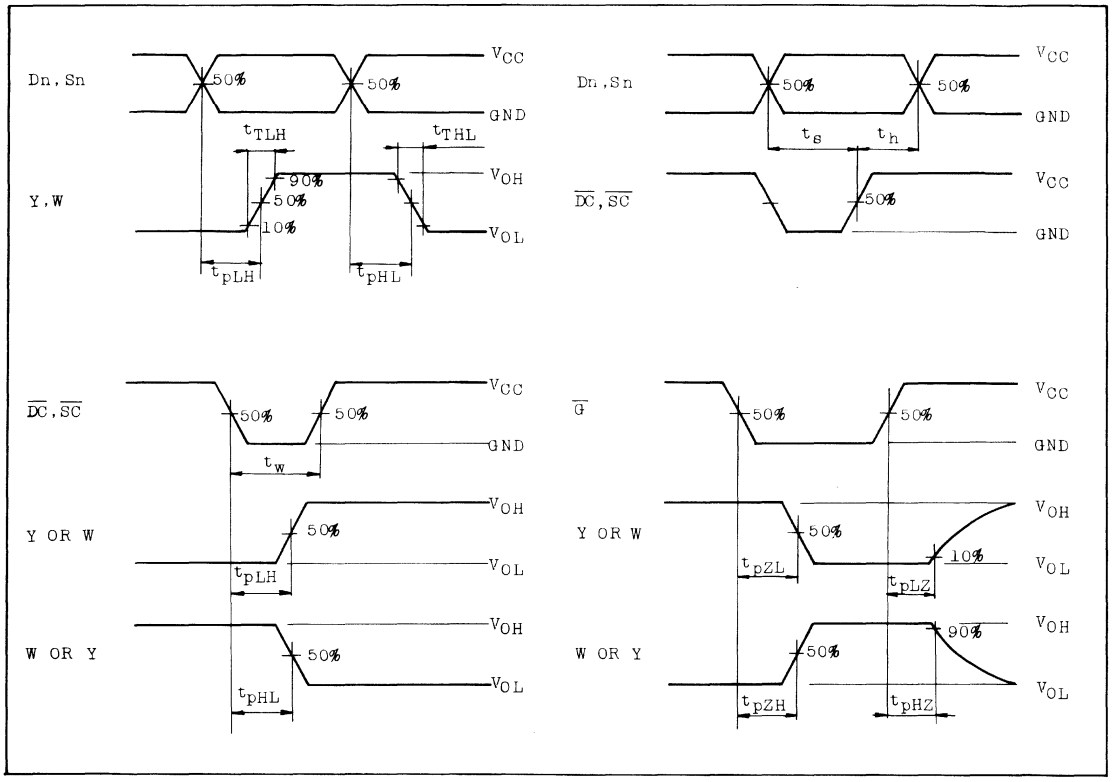
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time (Sn - Y, W)	t_{pLH} t_{pHL}		2.0	-	152	285	-	355	nS
			4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	156	295	-	370	
			4.5	-	39	59	-	74	
			6.0	-	33	50	-	63	
Minimum Pulse Width ($\overline{DC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	84	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

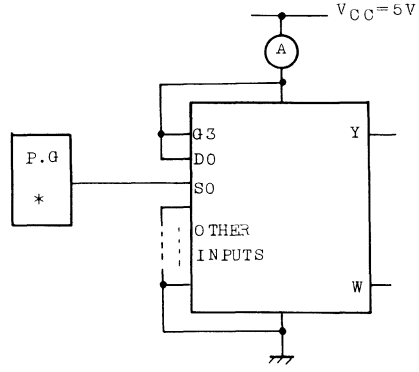
$$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC354P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr.) TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC356P/F

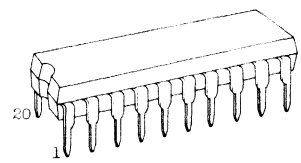
TC74HC356P/F 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

GENERAL DESCRIPTION

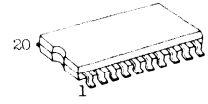
The TC74HC356 is high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC356 is similar in function to TC74HC354, which has a 8-bit latch as the data register instead of 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=29ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Ouptut Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS356



DIP20(3D20A-P)



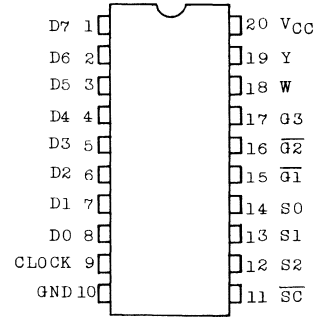
MFP20(F20GA-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC356P/F

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	CLOCK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z: HIGH IMPEDANCE

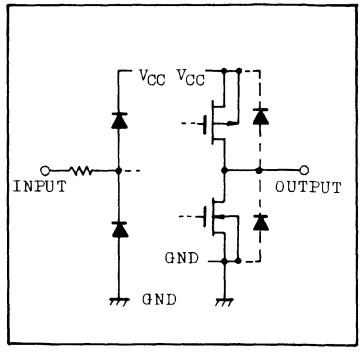
D0 …… D7: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, AT THE TIME OF THE LOW-TO-HIGH TRANSITION OF CLOCK.

#: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH SC LOW.

RECOMMENDED OPERATING CONDITIONS

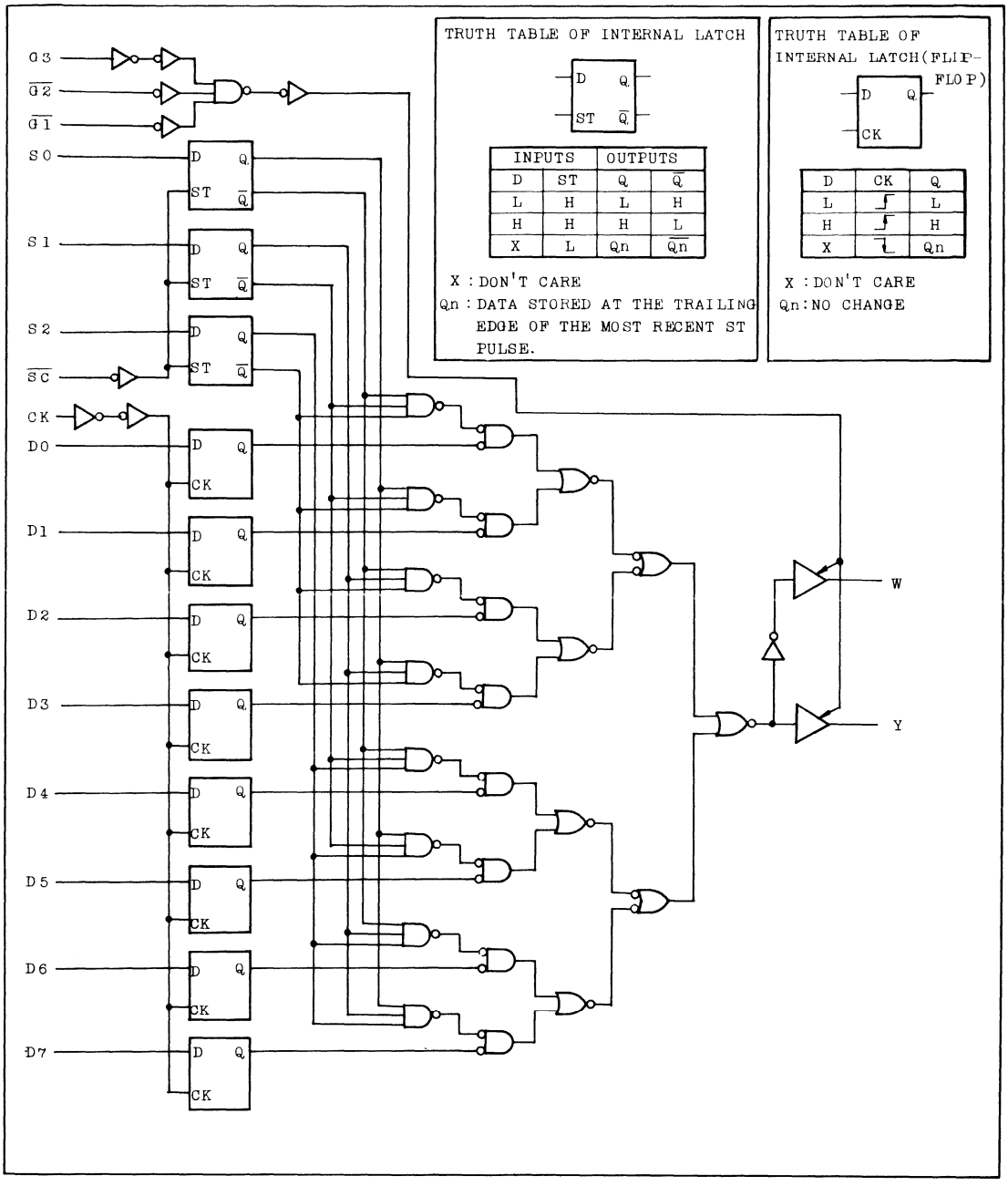
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC356P/F

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE
Qn : DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE OF INTERNAL LATCH(FLIP-FLOP)

D	CK	Q
L	↑	L
H	↑	H
X	↓	Qn

X : DON'T CARE
Qn : NO CHANGE

TC74HC356P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Ouptut Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (CLOCK - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (Sn - Y, W)	t_{pLH} t_{pHL}		2.0	-	152	285	-	355	
			4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	

AC ELECTRICAL CHARACTERISTICS (Continued)

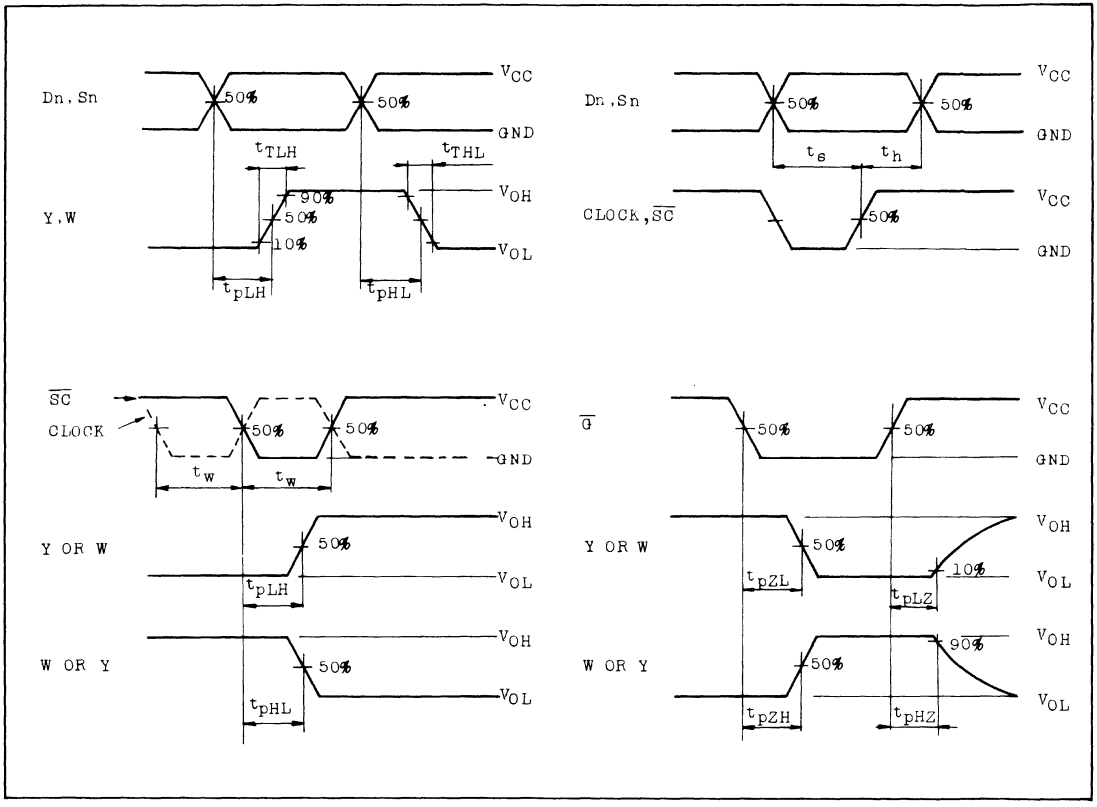
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH}		2.0	-	156	295	-	370	ns
			4.5	-	39	59	-	74	
	t_{pHL}		6.0	-	33	50	-	63	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{PZL}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
	t_{PZH}		6.0	-	14	21	-	26	
Output Disable Time	t_{PLZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
	t_{PHZ}		6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	53	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

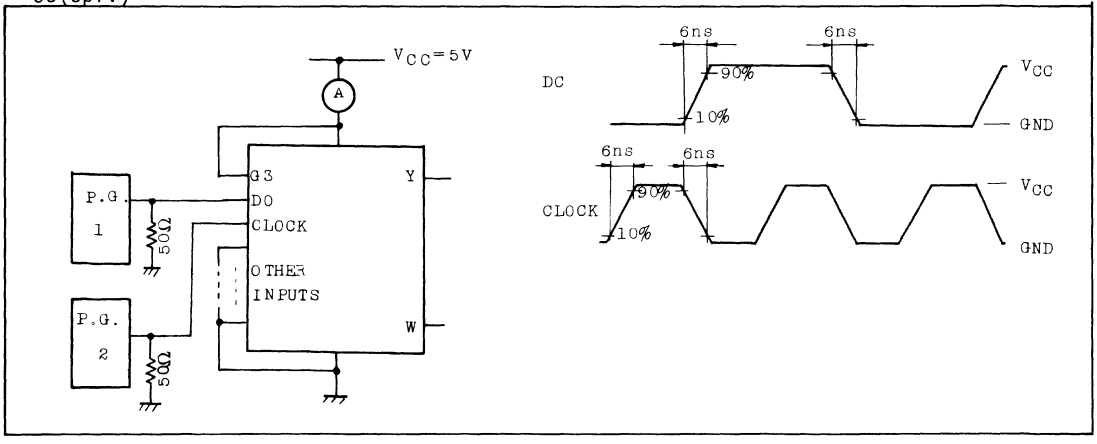
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC356P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT, WAVEFORM



TC74HC365P/F
TC74HC366P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

HEX BUS BUFFER
TC74HC365P/F NON-INVERTING
TC74HC366P/F INVERTING

The TC74HC365 and TC74HC366 are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.

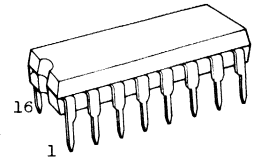
These devices achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$); all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, and at the other conditions these output are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366).

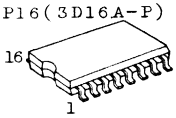
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS365/366

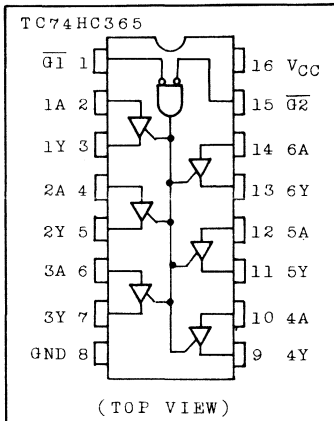


DIP16(3D16A-P)

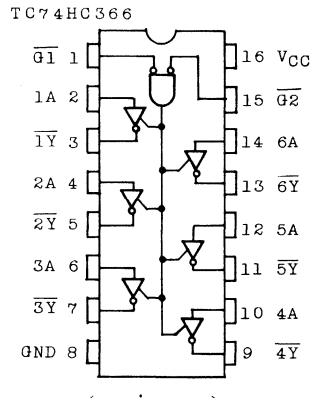


MFP16(F16GC-P)

PIN ASSIGNMENT



(TOP VIEW)



(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn(365)	$\overline{Yn}$(366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC365P/F
TC74HC366P/F

ABSOLUTE MAXIMUM RATINGS

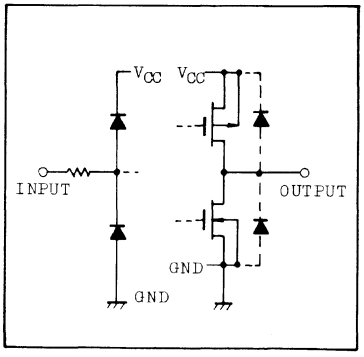
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC365P/F
TC74HC366P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}= 6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}= 7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time **	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	96	175	-	220	
			4.5	-	24	35	-	44	
			6.0	-	20	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

TC74HC365P/F
TC74HC366P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

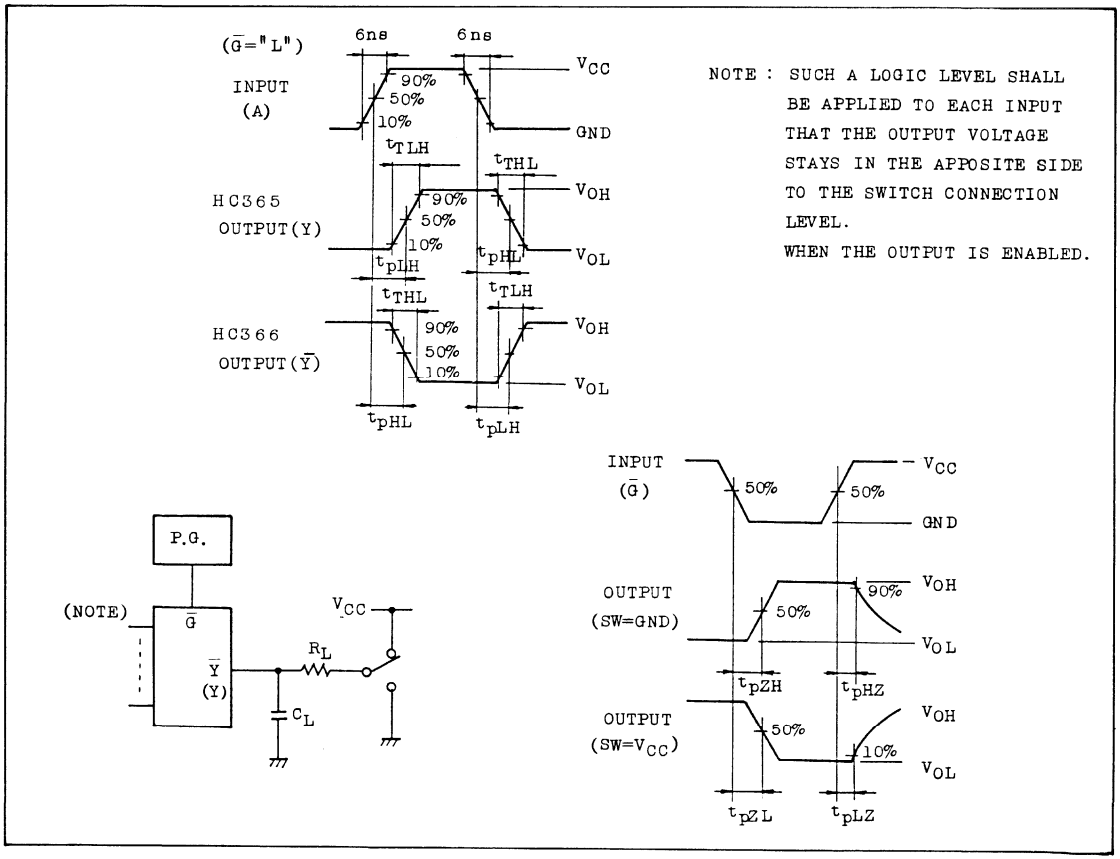
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Power Dissipation Capacitance	C_{PD}(1)	TC74HC365		-	33	-	-	-	pF
		TC74HC366		-	31	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per Circuit)}$$

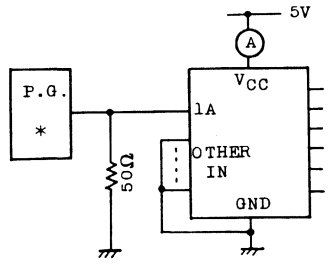
(2) * : for TC74HC365 only.
**: for TC74HC366 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC365P/F
TC74HC366P/F

$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

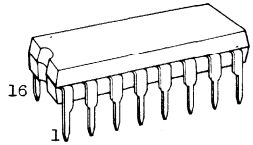
At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC367P/F
TC74HC368P/F

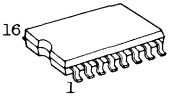
C²MOS DIGITAL INTEGRATED CIRCUIT

HEX BUS BUFFER
TC74HC367P/F NON-INVERTING
TC74HC368P/F INVERTING

The TC74HC367 and TC74HC368 are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.
These devices achieve the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation. These devices contain six buffers, and four buffers are controlled by a enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$); these outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.
These outputs are capable of driving up to 15 LSTTL.
The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).
All outputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)



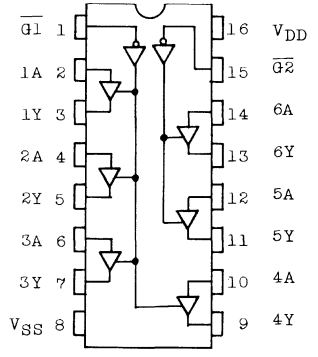
MFP16(F16GC-P)

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$= 6 mA
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS367/368

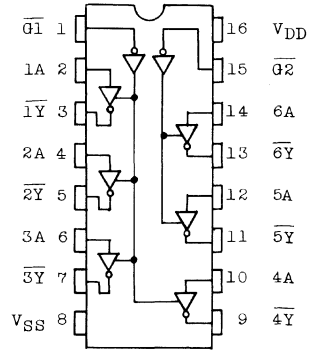
PIN ASSIGNMENT

TC74HC367



(TOP VIEW)

TC74HC368



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Yn(367)	$\overline{Yn}$(368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC367P/F
TC74HC368P/F

ABSOLUTE MAXIMUM RATINGS

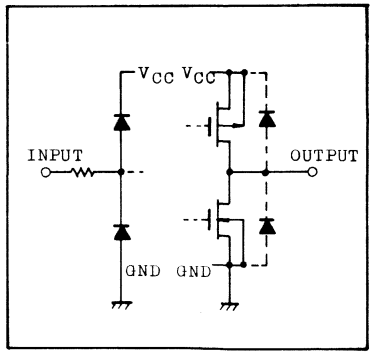
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC367P/F
TC74HC368P/F

DC ELECTRICAL CHARACTERISITCS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time *	t_{pLH}		2.0	-	60	120	-	150	
	t_{pHL}		4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time **	t_{pLH}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
	t_{pHL}		6.0	-	12	20	-	25	
Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	60	120	-	150	
	t_{pZH}		4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	80	150	-	190	
			4.5	-	20	30	-	38	
	t_{pHZ}		6.0	-	17	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

AC ELECTRICAL CHACTERISTICS (Continued)

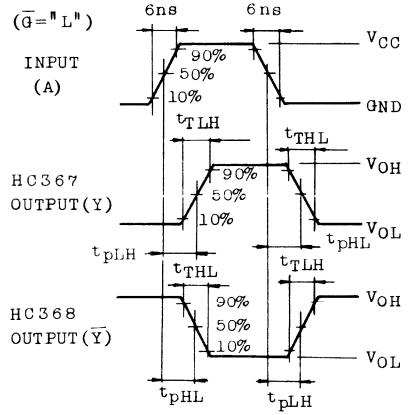
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Power Dissipation Capacitance	C_{PD}(1)	TC74HC367		-	32	-	-	-	pF
		TC74HC368		-	29	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

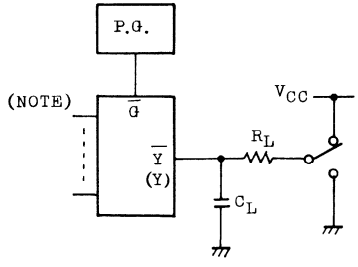
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(Per Circuit)}$$

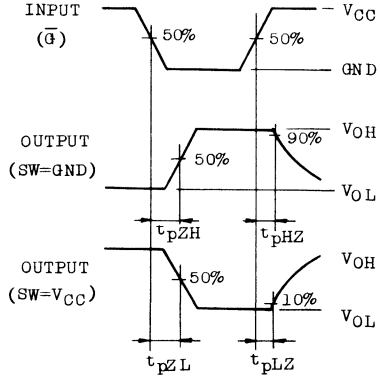
(2) *: for TC74HC367 only.
**: for TC74HC368 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



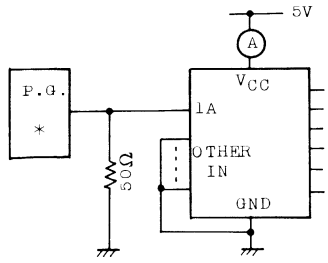
NOTE : SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL, WHEN THE OUTPUT IS ENABLED.





TC74HC367P/F
TC74HC368P/F

$I_{CC(opr)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the for mula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC373P/F • TC74HC533P/F TC74HC563P/F • TC74HC573P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC373P/F NON-INVERTING
TC74HC533P/F INVERTING
TC74HC563P/F INVERTING
TC74HC573P/F NON-INVERTING

The TC74HC373, TC74HC533, TC74HC563 and TC74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

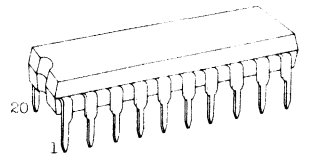
The TC74HC373 and the TC74HC573, the TC74HC533 and The TC74HC563 have the same function and the same characteristics respectively, but have the different pin layouts.

The three-state output configuration and the wide choice of outline will make the bus-organized system simple.

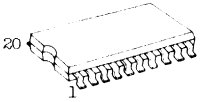
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance...$|I_{OH}|$=I_{OL}=6mA
- Balanced Propagation Delays....t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range...$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS373/533/563/573



DIP20(3D20A-P)

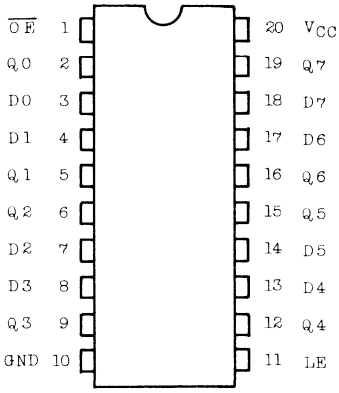


MFP20(F20GA-P)

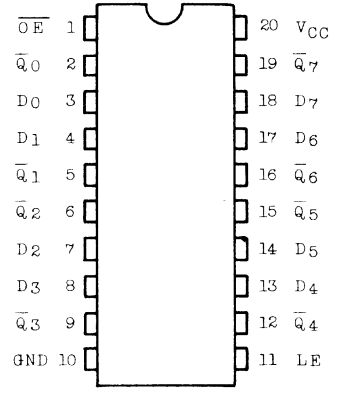
TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

PIN ASSIGNMENT (TOP VIEW)

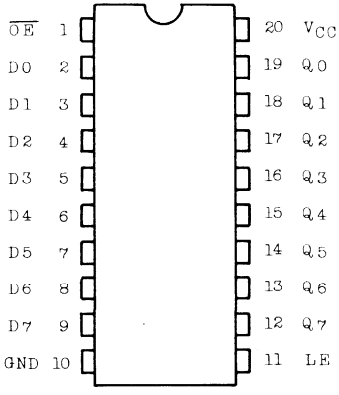
TC74HC373



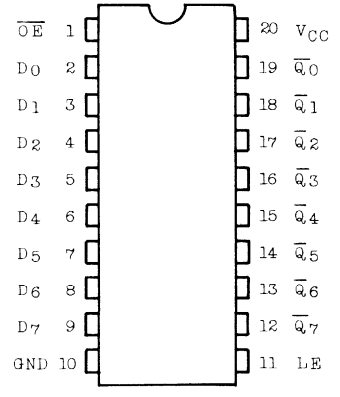
TC74HC533



TC74HC573



TC74HC563



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373,HC573)	$\overline{Q}$ (HC533,HC563)
H	X	X	Z	Z
L	L	X	No change *	No change *
L	H	L	L	H
L	H	H	H	L

X : Don't care

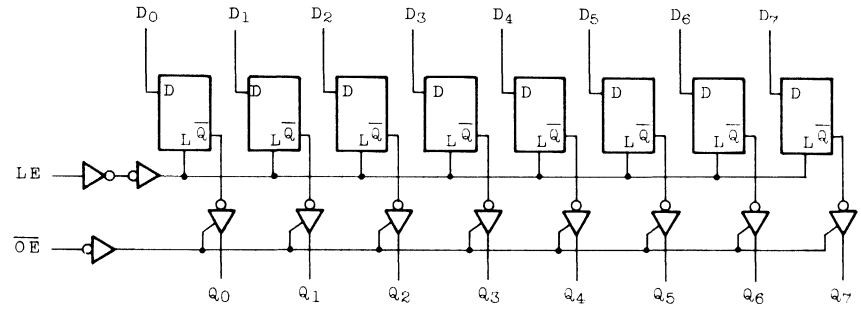
Z : High impedance

* : Q/$\overline{Q}$ outputs are latched at the time when the LE input is taken low logic level.

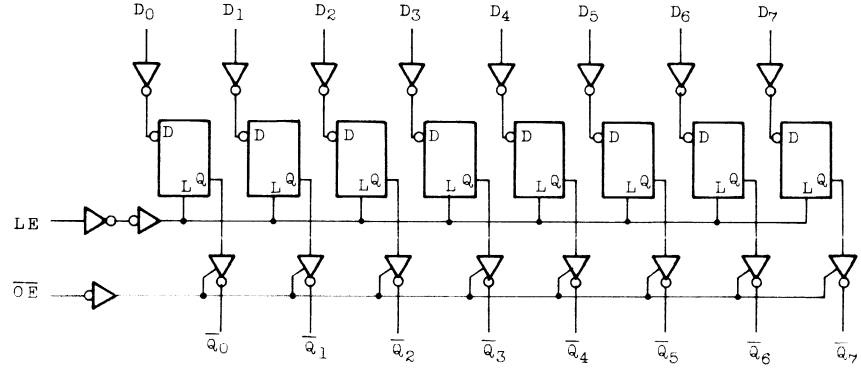
TC74HC373P/F·TC74HC533P/F
TC74HC563P/F·TC74HC573P/F

LOGIC DIAGRAM

TC74HC373, TC74HC573



TC74HC533, TC74HC563



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

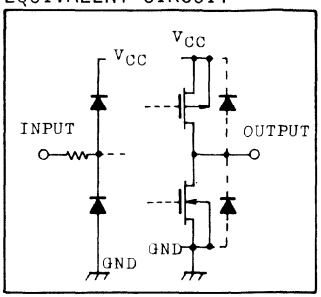
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC373P/F・TC74HC533P/F
TC74HC563P/F・TC74HC573P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC373P/F · TC74HC533P/F
TC74HC563P/F · TC74HC573P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (LE - Q, $\overline{Q}$) *	t_{pLH}		2.0	-	88	175	-	220	
	t_{pHL}		4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (D - Q, $\overline{Q}$) *	t_{pLH}		2.0	-	72	145	-	180	
	t_{pHL}		4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time (LE - Q, $\overline{Q}$) **	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (D - Q, $\overline{Q}$) **	t_{pLH}		2.0	-	64	130	-	165	
	t_{pHL}		4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Minimum Pulse Width (LE)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time	t_h		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Output Enable Time *	t_{pZL}	R_L=1kΩ	2.0	-	72	150	-	190	
	t_{pZH}		4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Output Disable Time *	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
	t_{pHZ}		4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Output Enable Time **	t_{pZL}	R_L=1kΩ	2.0	-	64	140	-	175	
	t_{pZH}		4.5	-	16	28	-	35	
			6.0	-	14	24	-	30	
Output Disable Time **	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
	t_{pHZ}		4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	41	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

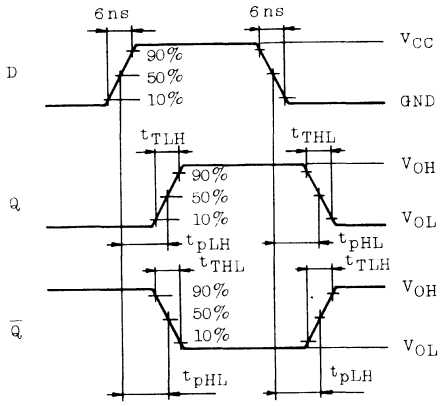
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

(2) *: for TC74HC373/533
**: for TC74HC563/573

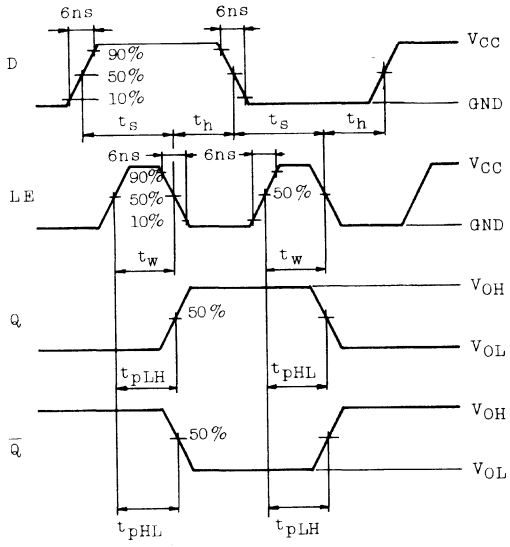
TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL} (D - Q,$\overline{Q}$)



t_{pLH}, t_{pHL} (LE - Q,$\overline{Q}$), t_s, th, t_w

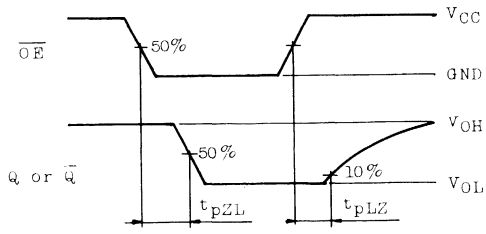


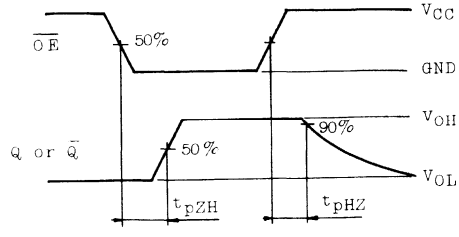
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

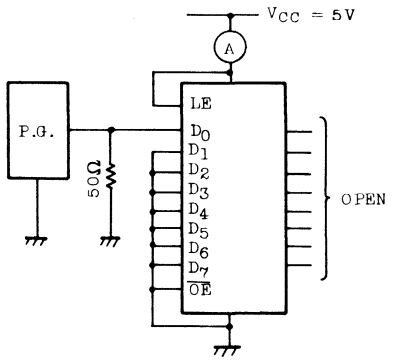
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





$I_{CC(opr)}$ TEST CIRCUIT



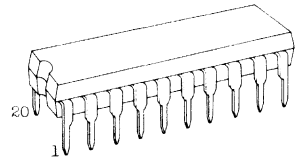
Input waveform is the same as thah in case of switching characteristics test.

TC74HCT373P/F

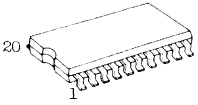
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT373P/F OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74HCT373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
It may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT373 is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The TC74HCT373 and the TC74HCT573 have the same function and the same characteristics respectively, but have the different pin layouts. The three-state output configuration and the wide choise of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)

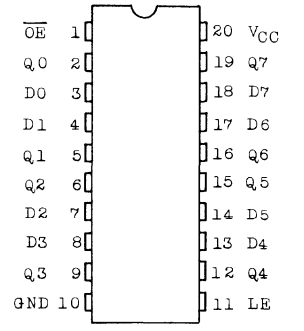


MFP20(F20GA-P)

FEATURES:

- High speed ..... t_{pd}=19ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V (Min.), V_{IL}=0.8V(Max.)
- Wide interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS373

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q(HCT373)
H	X	X	Z
L	L	X	No change*
L	H	L	L
L	H	H	H

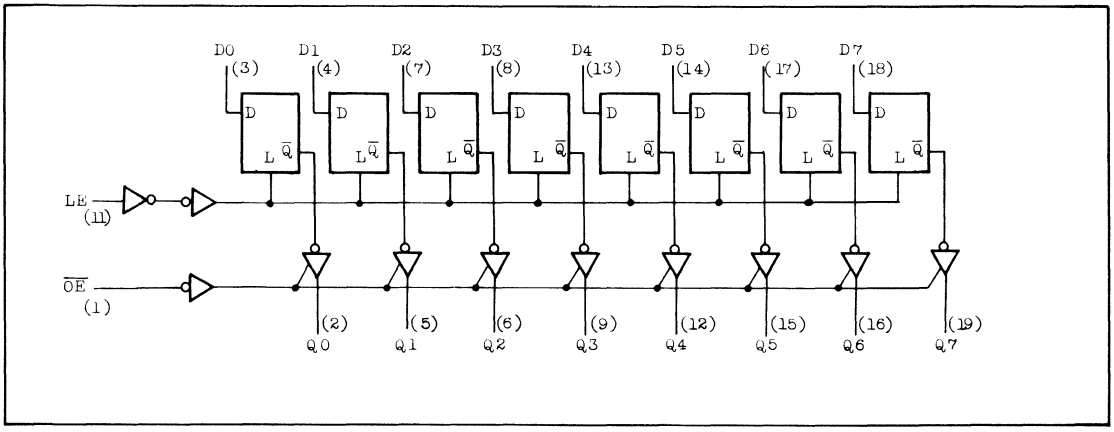
X: Don't care

Z: High impedance

*: Q output was latched at the time when the LE input is taken low logic level.

TC74HCT373P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

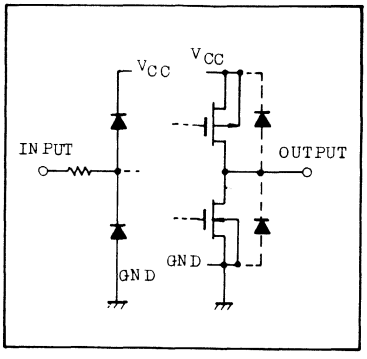
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT373P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∫ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∫ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (LE - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Propagation Delay Time (D - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	ns

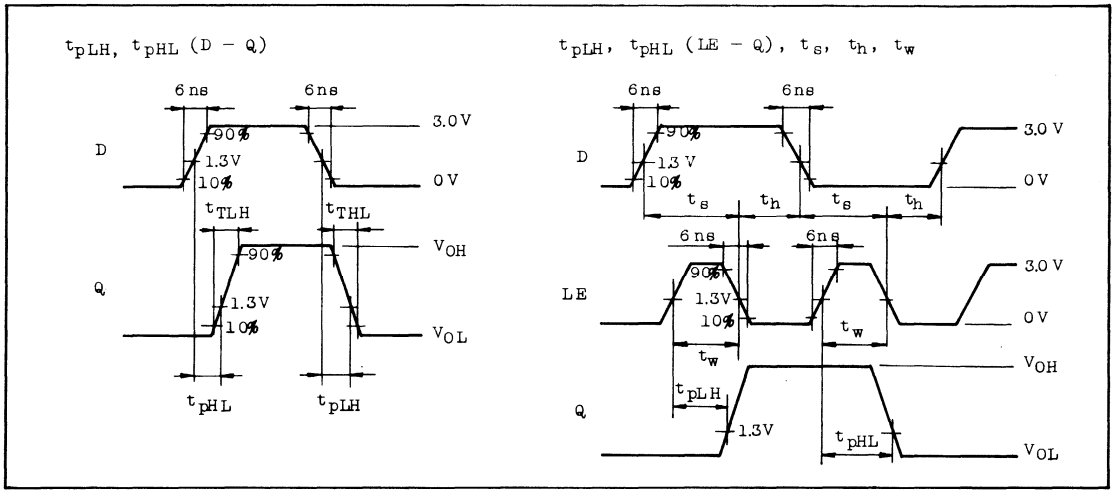
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time	t_s		4.5	-	0	5	-	6	ns
Minimum Hold Time	t_h		4.5	-	3	10	-	13	ns
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	23	35	-	44	ns
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	21	30	-	38	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	55	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumpiton without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

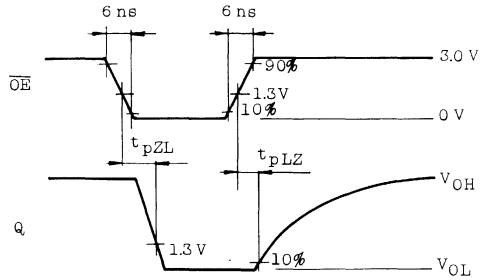


TC74HCT373P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

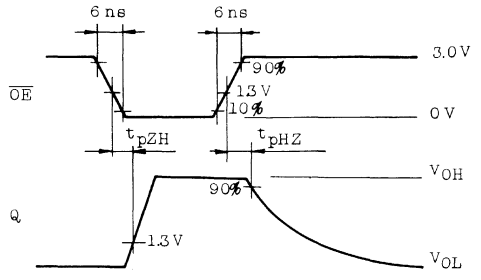
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line to GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

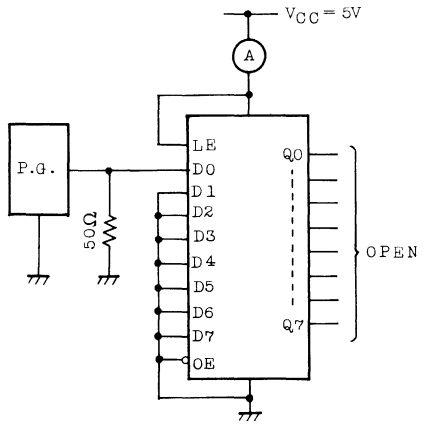


t_{pHZ}, t_{pZH}

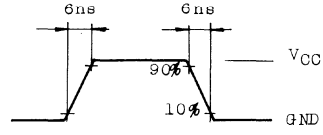
The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.



I_{CC}(Opr.) TEST CIRCUIT



INPUT WAVEFORM



TC74HC374P/F · TC74HC534P/F
TC74HC564P/F · TC74HC574P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

OCTAL D-TYPE FLIP-FLIP WITH 3-STATE OUTPUT

TC74HC374P/F NON-INVERTING
TC74HC534P/F INVERTING
TC74HC564P/F INVERTING
TC74HC574P/F NON-INVERTING

The TC74HC374P, TC74HC534P, TC74HC564P and TC74HC574P are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely (HC374 and HC574) or inversely (HC534 and HC564) to the logic state that were setup at the D inputs.

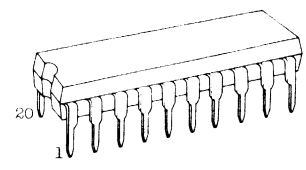
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

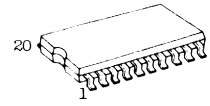
The TC74HC374 and the TC74HC574, the TC74HC534 and the TC74HC564 are identical respectively except the pin layout. The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=45MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS374/534/564/574



DIP20(3D20A-P)

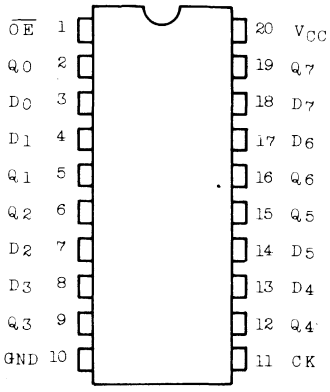


MFP20(F200A-P)

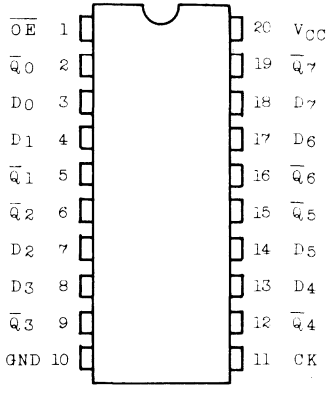
TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

PIN ASSIGNMENT

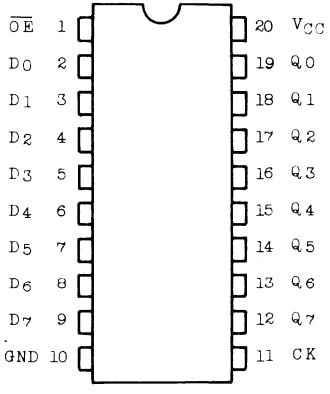
TC74HC374



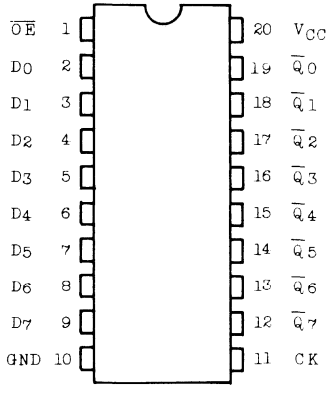
TC74HC534



TC74HC574



TC74HC564



TRUTH TABLE

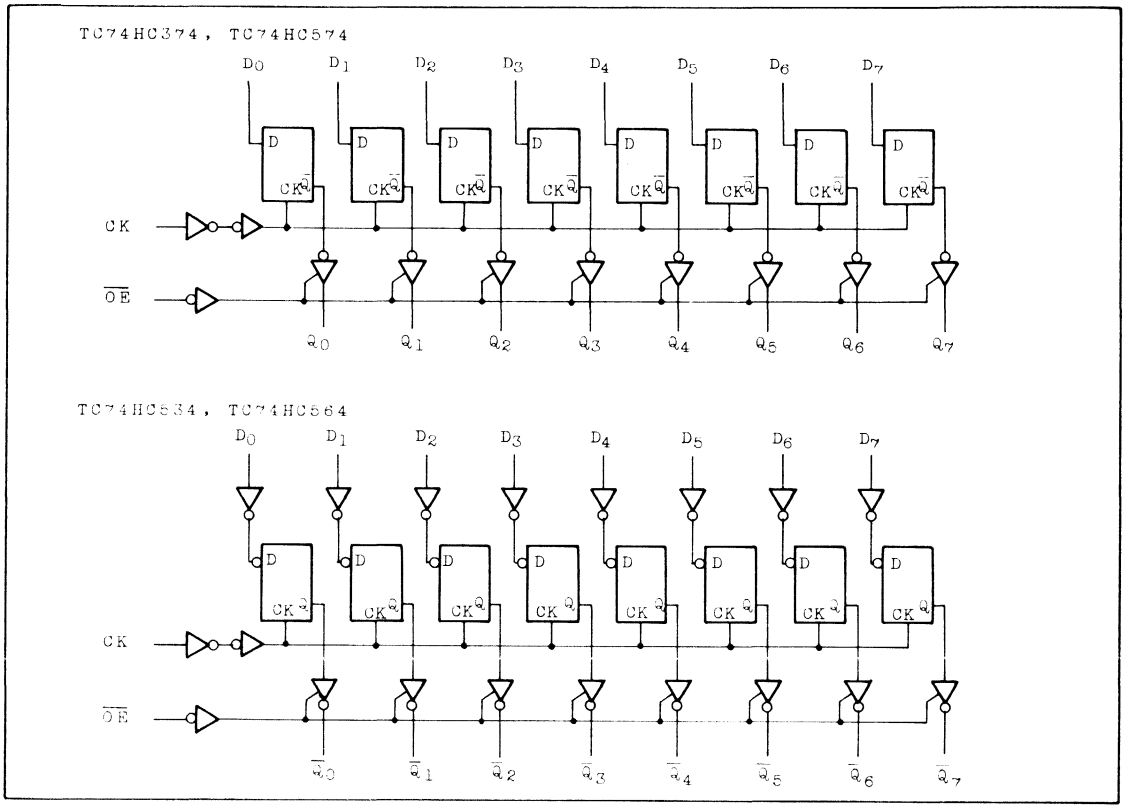
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374,HC574)	$\overline{Q}$ (HC534,HC564)
H	X	X	Z	Z
L	↓	X	No change	No change
L	↓	L	L	H
L	↓	H	H	L

X : Don't care

Z : High impedance

TC74HC374P/F·TC74HC534P/F
TC74HC564P/F·TC74HC574P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

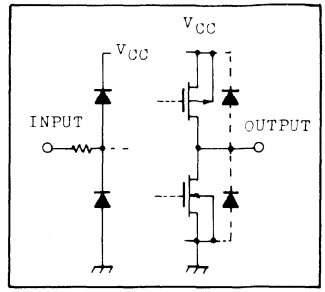
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC374P/F · TC74HC534P/F
TC74HC564P/F · TC74HC574P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
	t_{THL}		6.0	-	6	10	-	13	
Propagation Delay Time (CK - Q, $\overline{Q}$) *	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	
Propagation Delay Time (CK - Q, $\overline{Q}$) **	t_{pLH}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
	t_{pHL}		6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Set-up Time *	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time *	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set up Time **	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time **	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time *	t_{pZL}	R_L=1kΩ	2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
	t_{pZH}		6.0	-	15	26	-	33	
Output Disable Time *	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
	t_{pHZ}		6.0	-	18	26	-	33	
Output Enable Time **	t_{pZL}	R_L=1kΩ	2.0	-	64	140	-	175	
			4.5	-	16	28	-	35	
	t_{pZH}		6.0	-	14	24	-	30	
Output Disable Time **	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
	t_{pHZ}		6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	51	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Flip-Flop)}$$

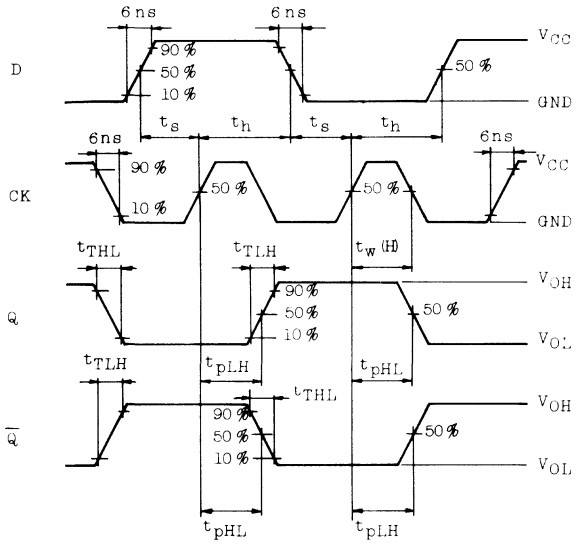
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation. $C_{PD(TOTAL)} = 34 + 17 \times N$ [pF]

(2) *: for TC74HC374/534
**: for TC74HC564/574

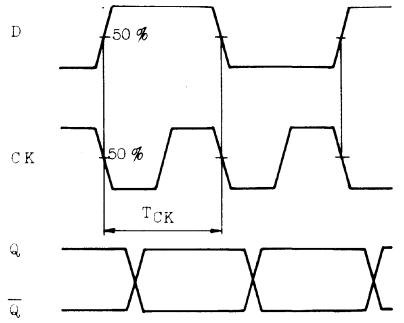
TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



f_{MAX}



Duty cycle of CK: 50%

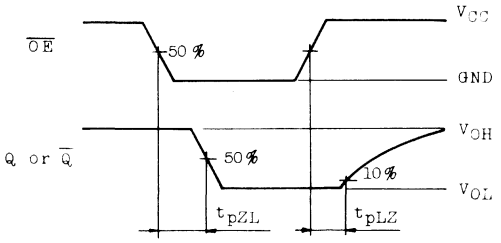
$$f_{MAX} = \frac{1}{T_{CK}}$$

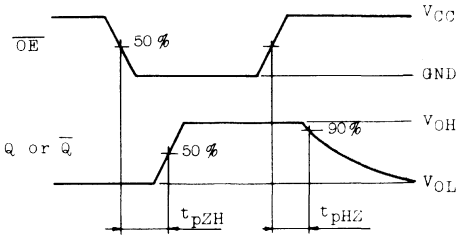
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

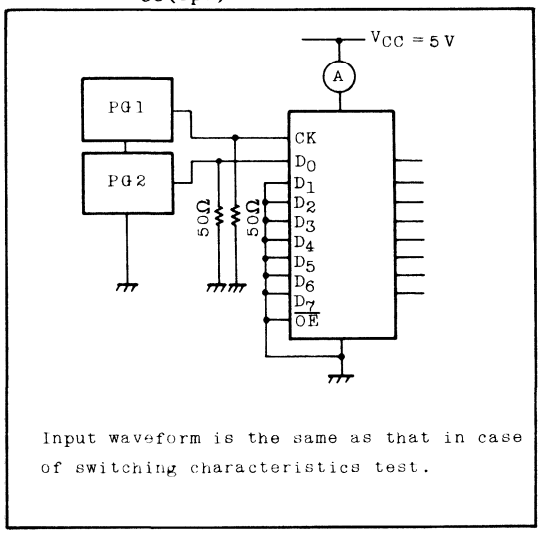
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HCT374P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT374P/F OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The TC74HCT374 is high speed CMOS OCTAL FLIP-FOLP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

This IC achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

This IC is controlled by a clock input (CK) and a output enable input ($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely to the logic state that were setup at the D inputs.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

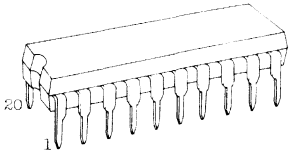
The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

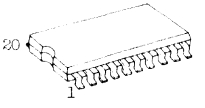
- High Speed ..... f_{MAX}=41MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Wide interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS374

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).



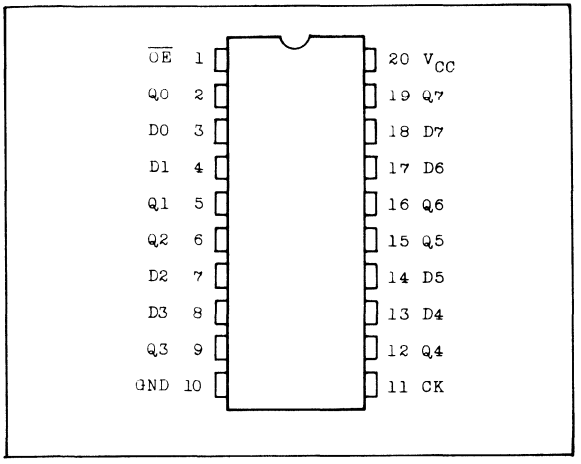
DIP20(3D20A-P)



MFP20(F20GA-P)

TC74HCT374P/F

PIN ASSIGNMENT



TRUTH TABLE

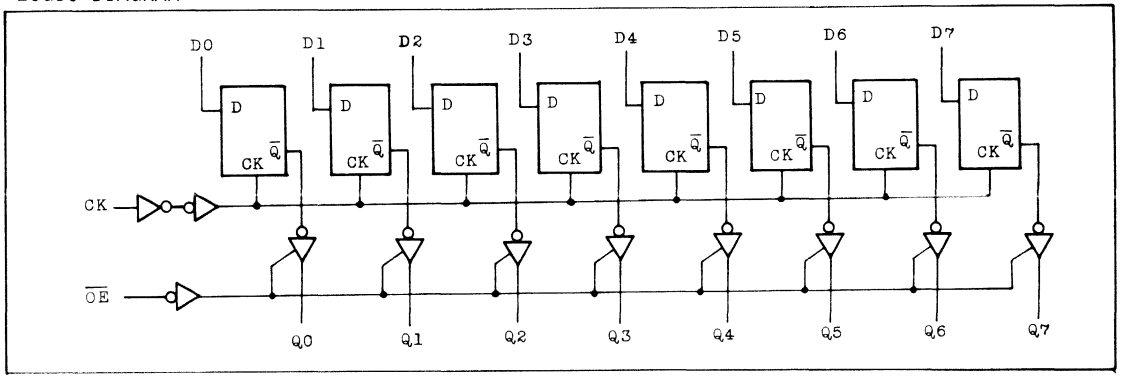
INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Qn: No change

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP)* 180 (MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

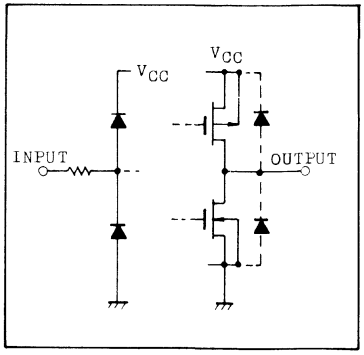
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HCT374P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL}; V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V; Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (CK - Q)	t_{pLH} t_{pHL}		4.5	-	26	40	-	50	ns
Maximum Clock Frequency	f_{MAX}		4.5	25	38	-	20	-	MHz
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		4.5	-	13	25	-	32	ns
Minimum Set-up Time	t_s		4.5	-	6	15	-	19	ns
Minimum Hodl Time	t_h		4.5	-	-	0	-	0	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	27	42	-	53	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	22	32	-	40	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	60	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

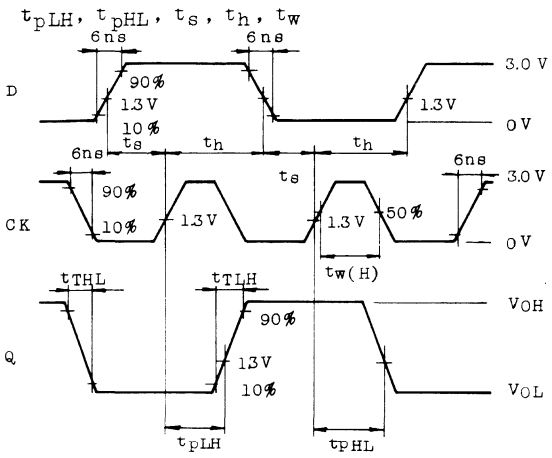
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Flip-Flop)}$$

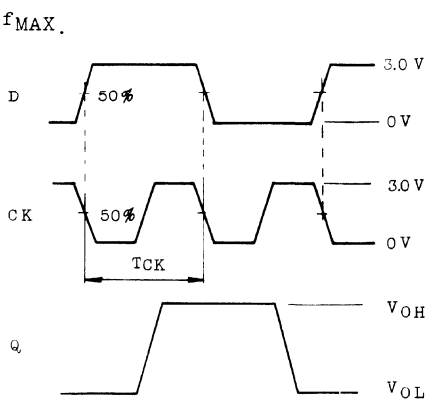
And the C_{PD} when n circuits of FLIP-FLOP operate, can be gained by the following equation.

$$C_{PD}(TOTAL)=42+18 \cdot n \text{ (pF)}$$

TC74HCT374P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM





Duty cycle of CK: 50%

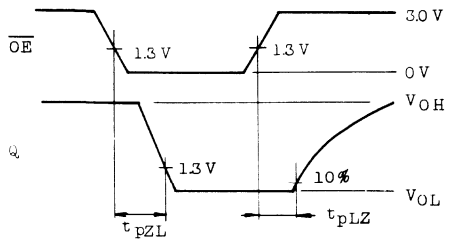
$$f_{MAX}=\frac{1}{T_{CK}}$$

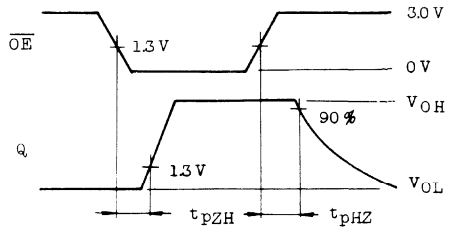
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

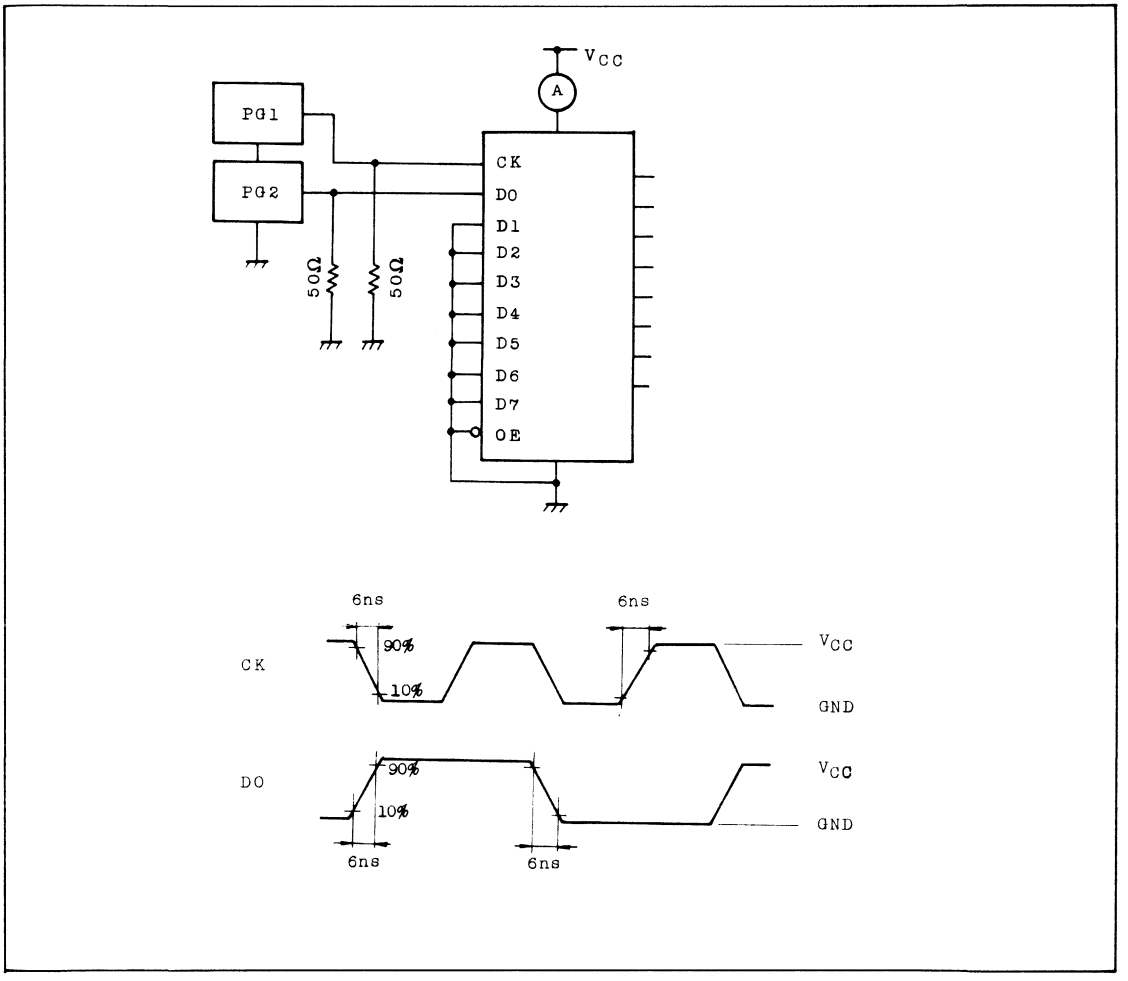
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input shuld be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ inputs is held low.





$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC375P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

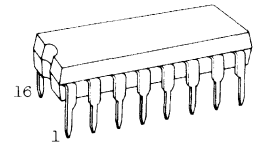
TC74HC375P/F 4-BIT D-TYPE LATCH

GENERAL DESCRIPTION

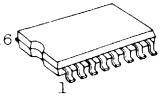
The TC74HC375 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contains two groups of 2-bit latches controlled by a enable input (G1·2 or G3·4). And those two latch groups can be used in the different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q thru 4Q and 1$\overline{Q}$ thru 4$\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at a time is re-tained at the outputs.
All inputs are equipped with protection circuits against static discharge of transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS375



DIP16(3D16A-P)



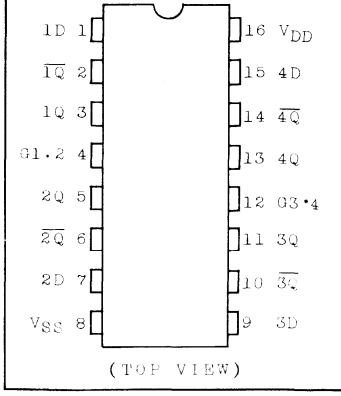
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

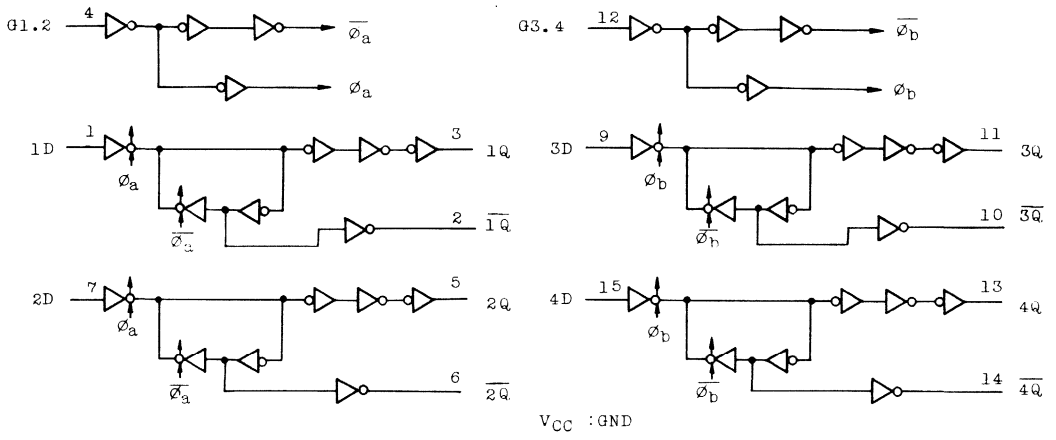
TC74HC375P/F

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\overline{Qn}$	LATCH

X : DON'T CARE

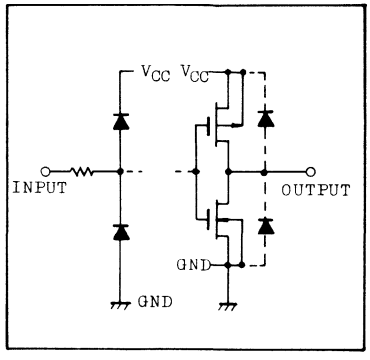
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC375P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Minimum Enable Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

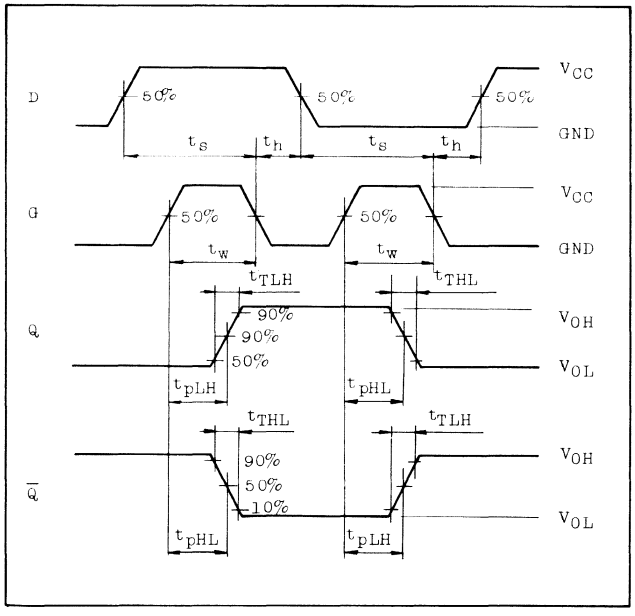
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	ns
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	48	-	-	-	

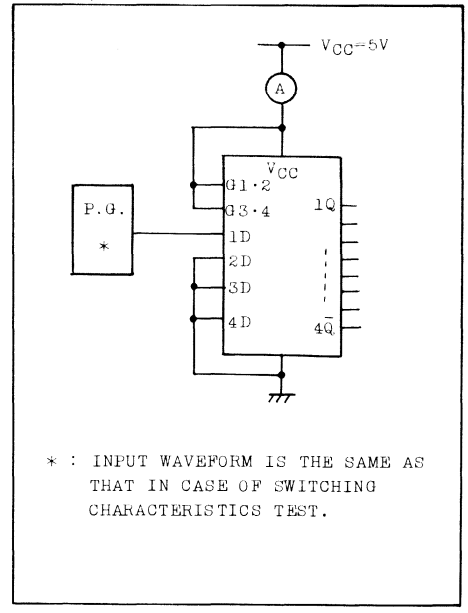
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC377P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC377P/F OCTAL D-TYPE FLIP-FLOP

The TC74HC377 is high speed CMOS D-TYPE FLIP-FLOP fabricated with silicon C^2MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS Low power dissipation.

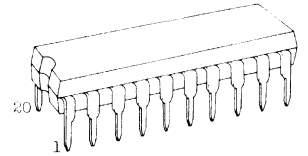
These eight flip-flops are controled by a clock input (CLOCK) and a enable input ($\overline{G}$). Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the enable input ($\overline{G}$) is held high, each Q outputs isn't changed.

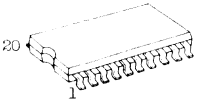
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL(74LS377)



DIP20(3D20A-P)



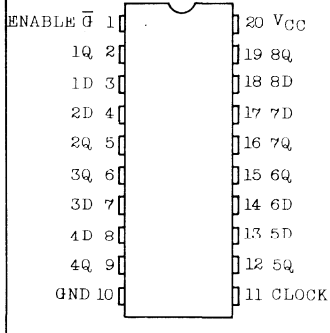
MFP20(F20GA-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



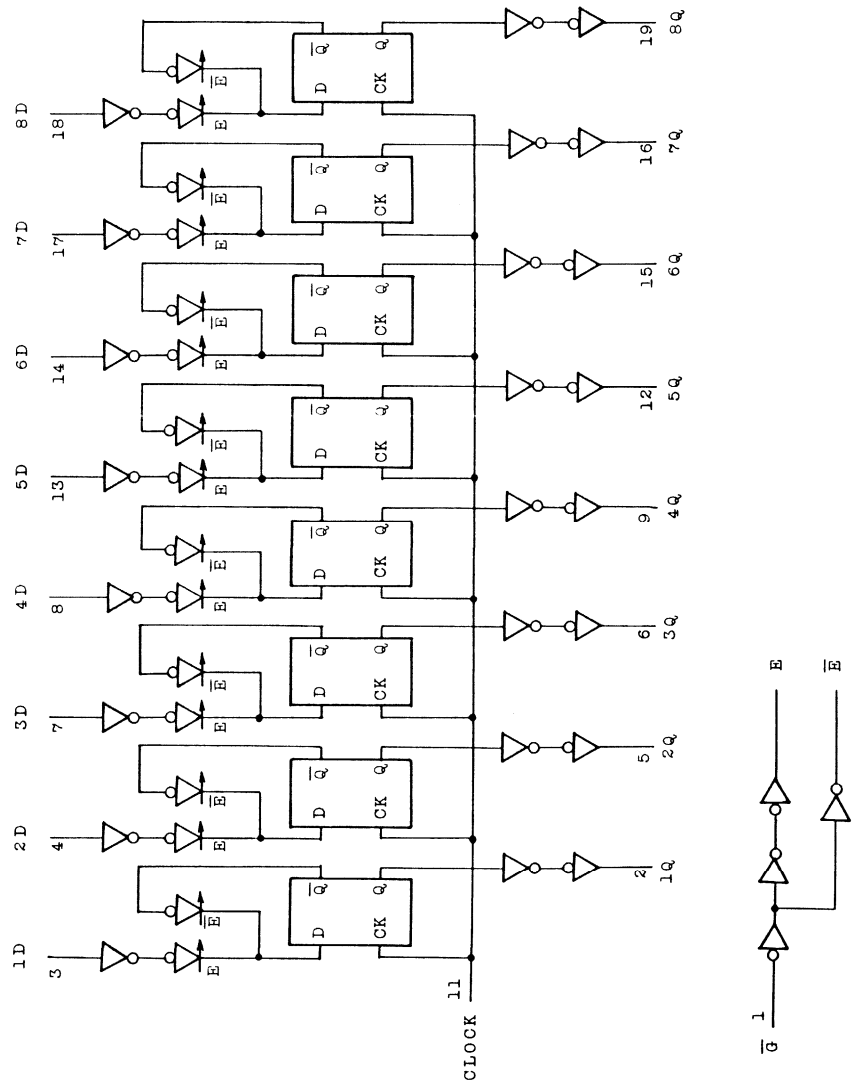
(TOP VIEW)

TC74HC377P/F

INPUTS			OUTPUTS
$\overline{G}$	CLOCK	DATA	Q
H	X	X	No Change
L	↑	L	L
L	↑	H	H
X	↓	X	No Change

X ; Don't care

LOGIC DIAGRAM

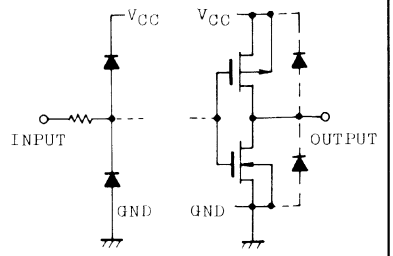


TC74HC377P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH}		2.0	-	80	160	-	200	
	t_{pHL}		4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	50	-	27	-	
			6.0	35	59	-	32	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (D - CK)	t_s		2.0	-	24	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set-up Time Enable ($\overline{G}$ - CK)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}				5	10		10	pF
Power Dissipation Capacitance	C_{PD}(1)				34				

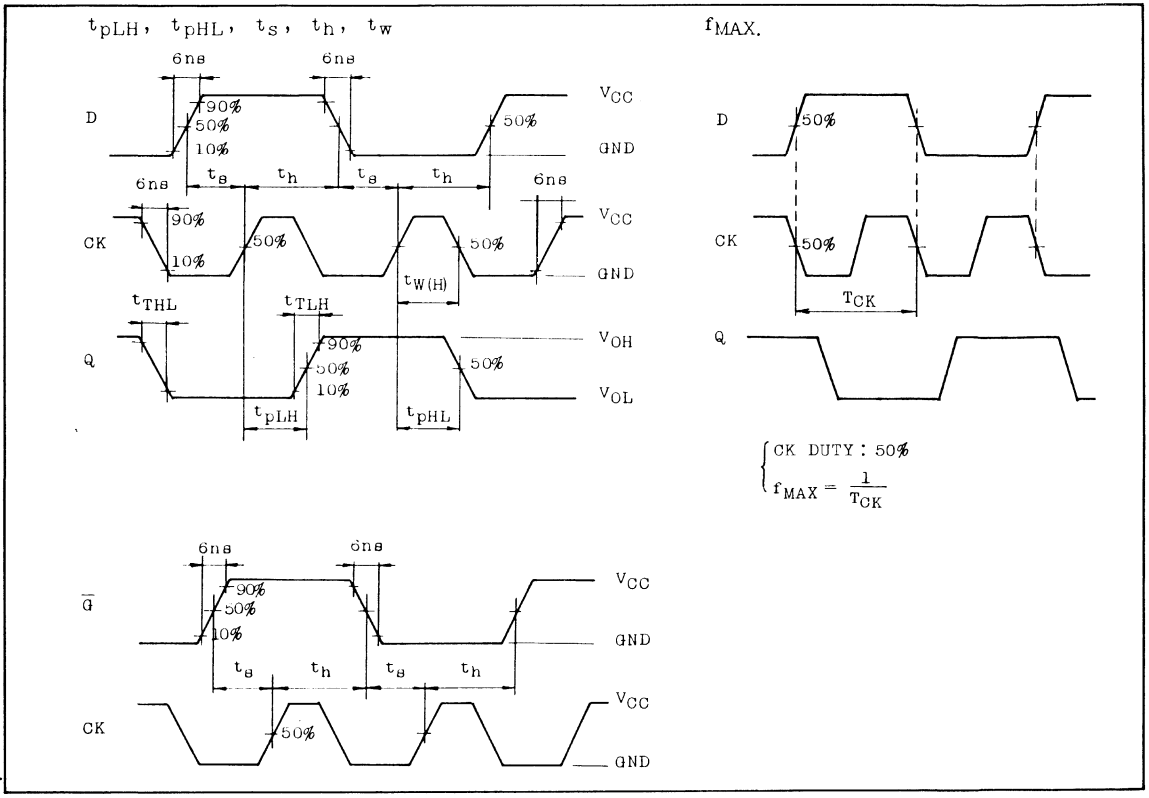
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$$

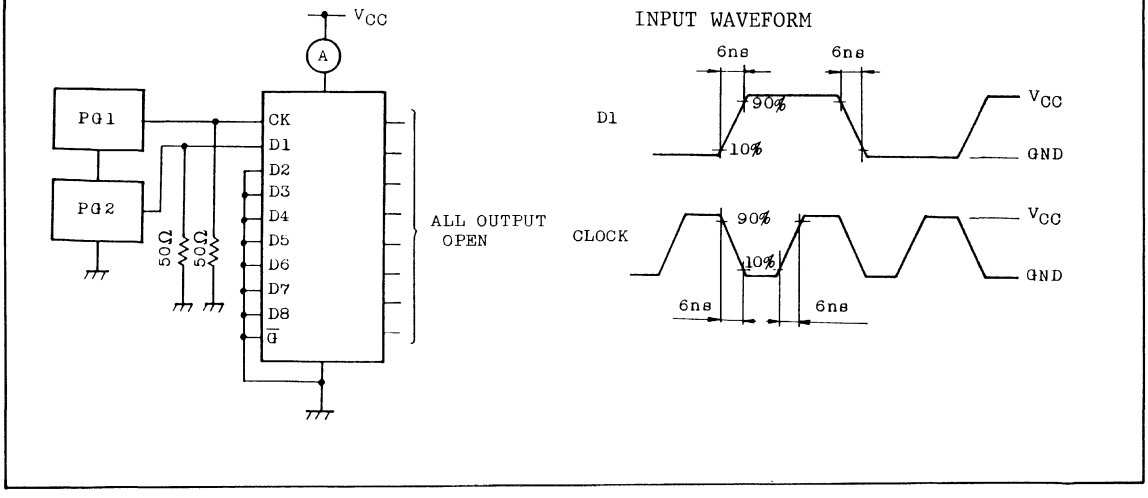
And the C_{PD} when n pcs of FLIP-FLOP operate, can be gained by following equation. $C_{PD}(TOTAL)=22+12\times n$ [pF]

TC74HC377P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC386P/F

TC74HC386P/F QUAD EXCLUSIVE-OR GATE

The TC74HC386 is a high speed CMOS EXCLUSIVE-OR GATE fabricated with silicon gate C²MOS technology.

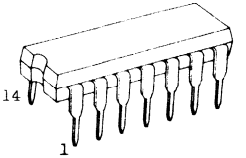
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Output buffer is equiped, which enables high noise immunity and stable output.

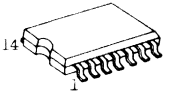
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS386

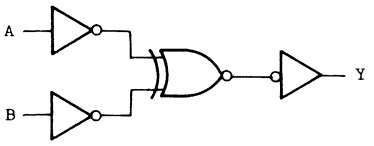


DIP14(3D14A-P)

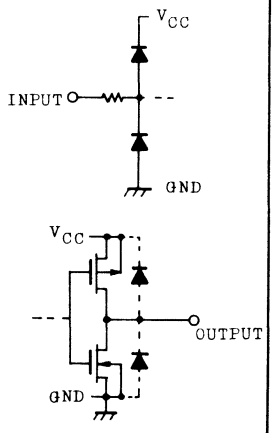


MFP14(F14GB-P)

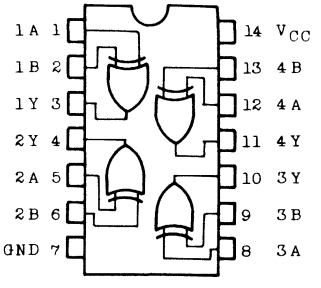
LOGIC DIAGRAM (PER GATE)



INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGMENT



(Top View)

TC74HC386P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

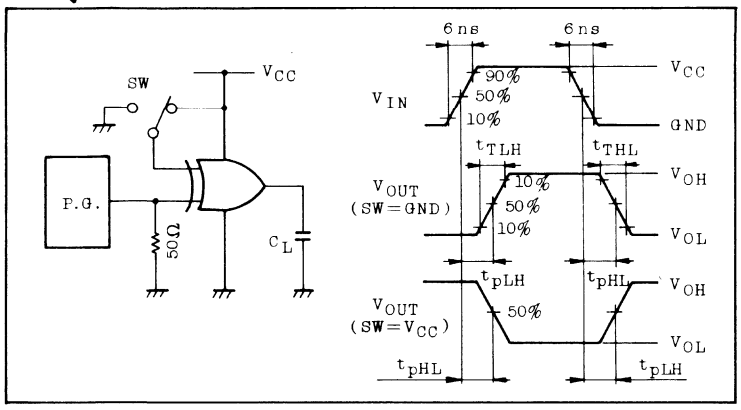
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	ns
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	33	-	-	-	

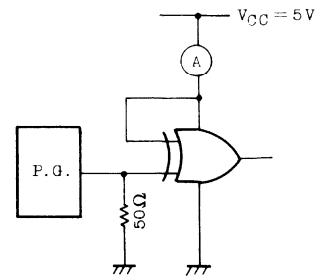
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

TC74HC386P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching chracteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

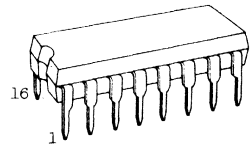
TC74HC390P/F

TC74HC390P/F DUAL DECADE COUNTER

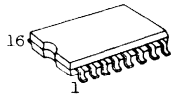
The TC74HC390P is a high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of two independent 4-bit counters, each composed of a divide-by-two and divide-by-five counter. A divide-by-two counter is incremented on the negative going transition of $\overline{\text{CLOCKA}}$. A divide-by-five counter is incremented on the negative going transition of $\overline{\text{CLOCKB}}$. The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, all Q outputs are set to low level independent of the clock input.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=63MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS390



DIP16(3D16A-P)



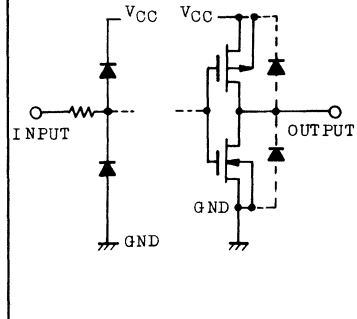
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

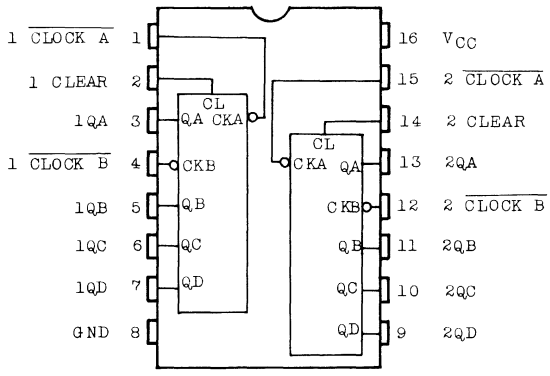
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



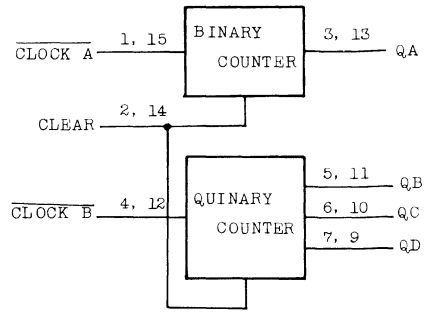
TC74HC390P/F

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



V_{CC} = 16, GND = 8

TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT*				BI-QUINARY**			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

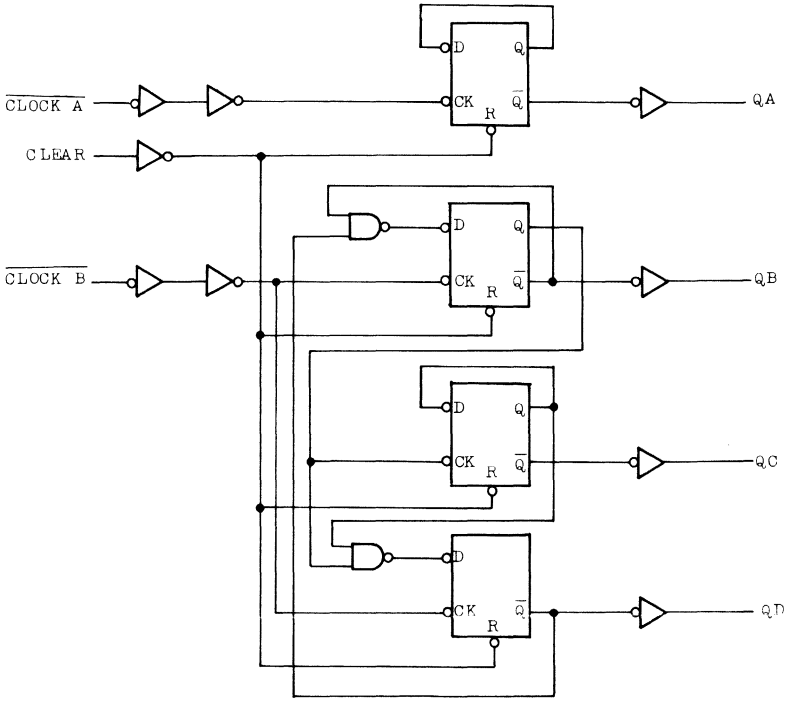
INPUTS			OUTPUTS			
$\overline{\text{CLOCK A}}$	$\overline{\text{CLOCK B}}$	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

X : DON'T CARE

NOTE * : OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$ FOR BCD COUNT.

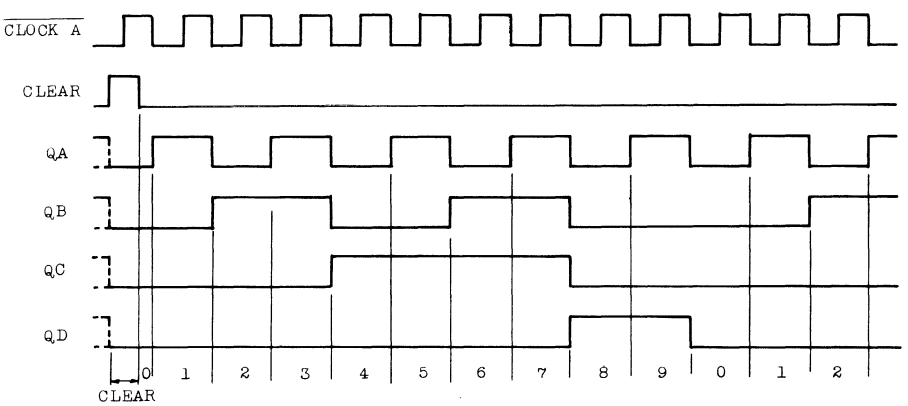
** : OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCK A}}$ FOR BI-QUINARY COUNT.

LOGIC DIAGRAM



TIMING CHART

(1) BCD COUNT SEQUENCE *

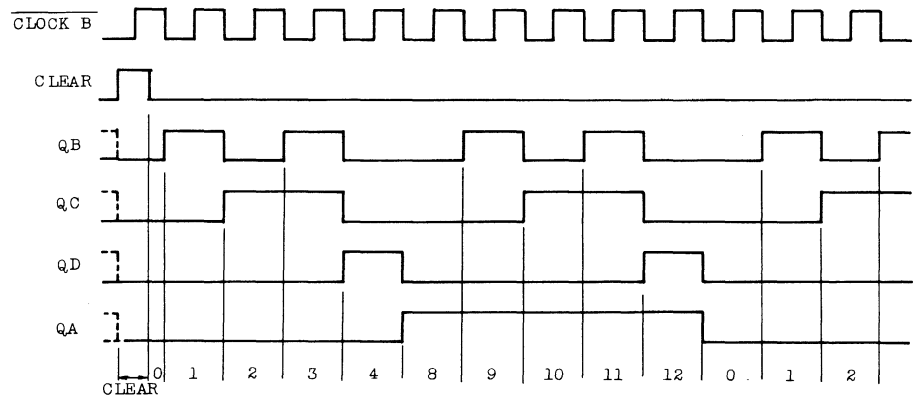


* OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$

TC74HC390P/F

TIMING CHART

(2) BI-QUINARY COUNT SEQUENCE **



** OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCKA}}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK\ A}$ - Q_A)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_B, Q_D)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_C)	t_{pLH} t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	

TC74HC390P/F

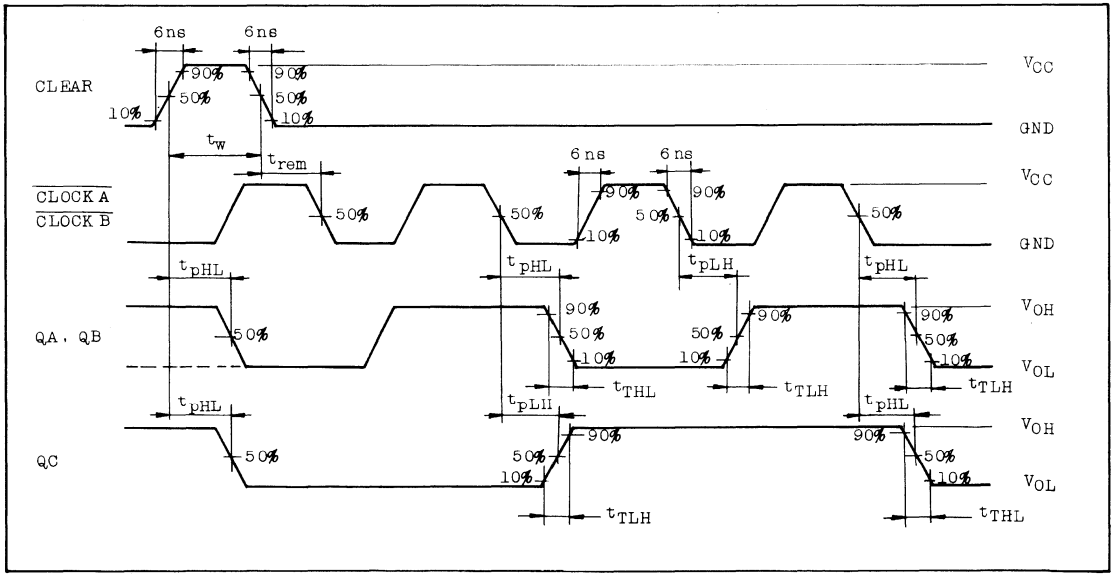
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Max. Clock Frequency $\overline{CLOCK\ A}$ - Q_A	f_{MAX}		2.0	6	15	-	5	-	MHz
			4.5	32	58	-	27	-	
			6.0	38	68	-	32	-	
Max. Clock Frequency $\overline{CLOCK\ B}$ - Q_B	f_{MAX}		2.0	5	10	-	4	-	
			4.5	27	41	-	22	-	
			6.0	32	48	-	26	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	44	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

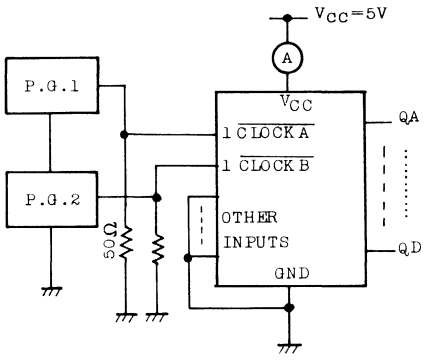
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

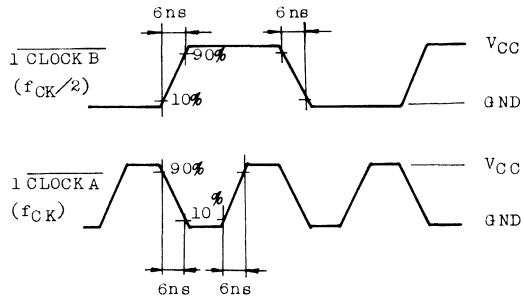


TC74HC390P/F

I_{CC}(opr.) TEST CIRCUIT



INPUT WAVEFORM



WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{Ca}{2} + \frac{f_{CK}}{2} \cdot V_{CC} \left(\frac{2Cb}{5} + \frac{Cc}{5} + \frac{Cd}{5} \right)$$

Ca ~ Cd ARE THE CAPACITANCE AT QA ~ QD OUTPUT.

TC74HC393P/F

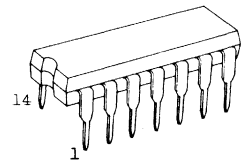
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC393P/F DUAL BINARY COUNTER

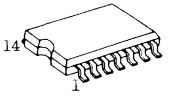
The TC74HC393 is a high speed CMOS DUAL 4-BIT BINARY COUNTER fabricated with silicon C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contain two independent circuits of counter with same functions in one package, counting or frequency division of eight binary bits can be achieved with one IC.
This device changes state on negative going transition of the clock pulse. The counter can be reset to "0" (Q0 ∿ Q3="L") by giving "H" level signal to CLEAR input regardless of other inputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=68MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS393



DIP14(3D14A-P)



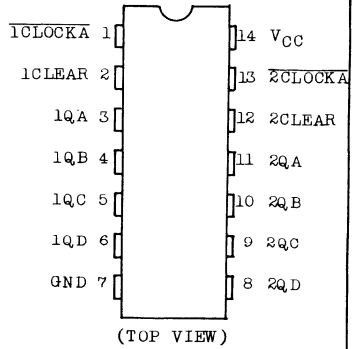
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

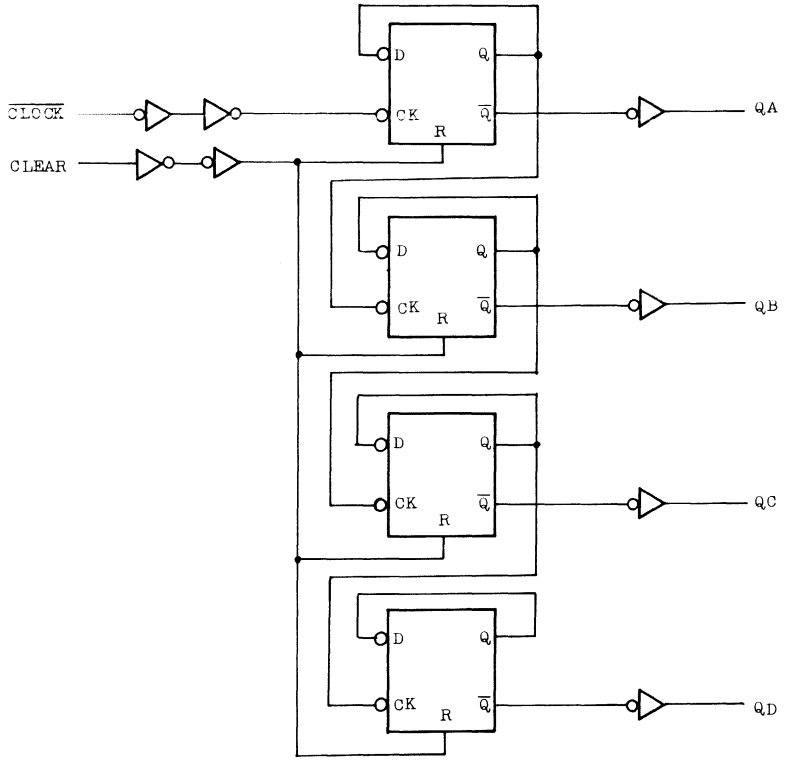
TC74HC393P/F

TRUTH TABLE

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

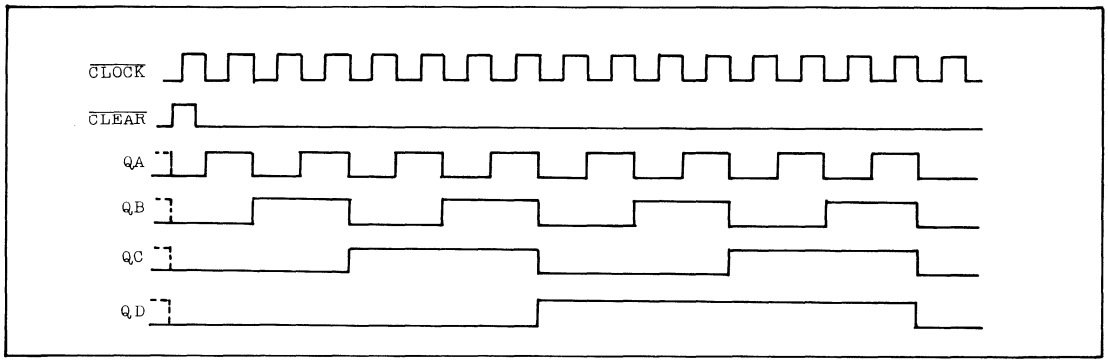
INPUTS		OUTPUTS			
$\overline{CLOCK}$	CLEAR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

LOGIC DIAGRAM



TC74HC393/F

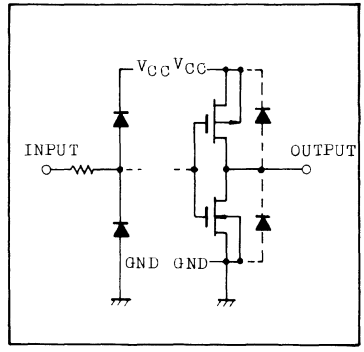
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	68	135	-	170	
($\overline{CLOCK}$ - QA)			4.5	-	17	27	-	34	
	t_{pHL}		6.0	-	14	23	-	29	
Propagation Delay Time	t_{pLH}		2.0	-	92	180	-	225	
($\overline{CLOCK}$ - QB)			4.5	-	23	36	-	45	
	t_{pHL}		6.0	-	20	31	-	38	
Propagation Delay Time	t_{pLH}		2.0	-	116	225	-	280	
($\overline{CLOCK}$ - QC)			4.5	-	29	45	-	56	
	t_{pHL}		6.0	-	25	38	-	48	
Propagation Delay Time	t_{pLH}		2.0	-	140	270	-	340	
($\overline{CLOCK}$ - QD)			4.5	-	35	54	-	68	
	t_{pHL}		6.0	-	30	46	-	58	
Propagation Delay Time	t_{pHL}		2.0	-	76	150	-	190	
(CLEAR - Qn)			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	16	-	5	-	MHz
			4.5	32	62	-	27	-	
			6.0	38	73	-	32	-	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	ns
($\overline{CLOCK}$)			4.5	-	8	15	-	19	
	$t_{w(L)}$		6.0	-	7	13	-	16	

TC74HC393P/F

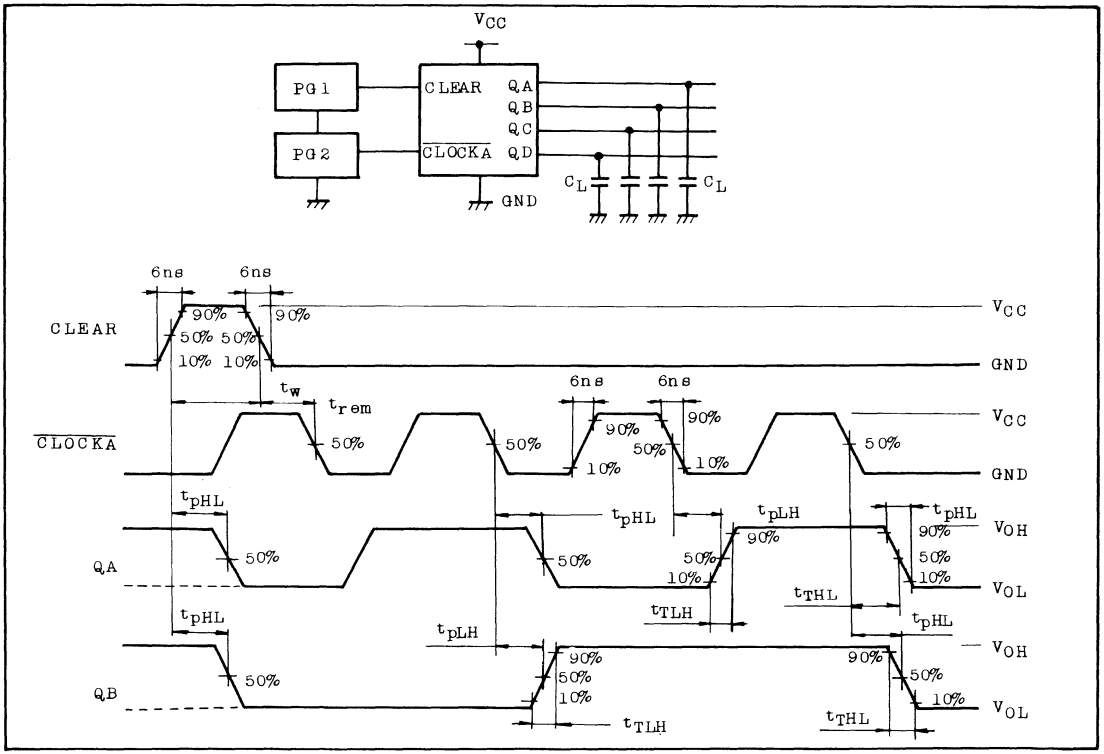
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	41	-	-	-	

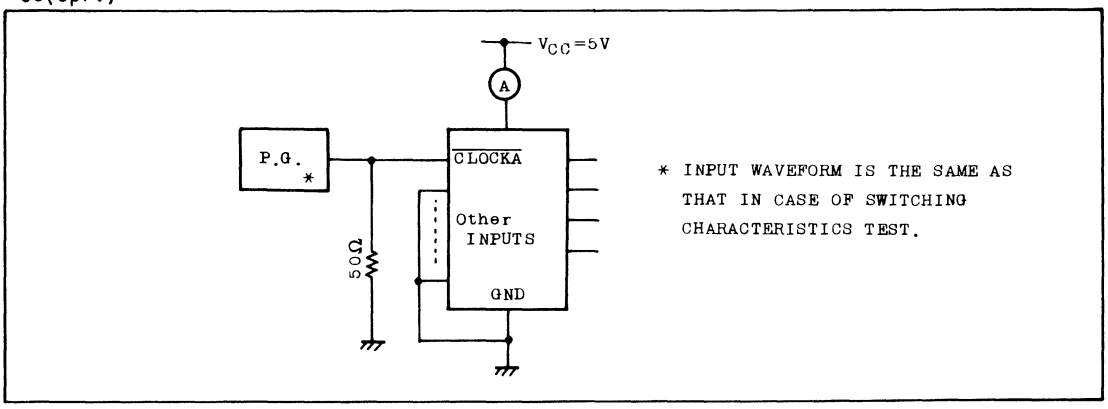
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr.) TEST CIRCUIT



TC74HC423P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC423P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC423 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is $\overline{A}$ INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... No limitation

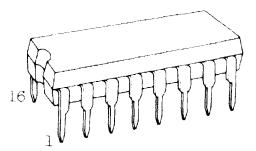
External resistor Rx ..... V_{CC} = 2.0V from 5KΩ to 1MΩ

$V_{CC} \geqq$ 3.0V from 1KΩ to 1MΩ

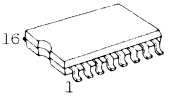
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=28ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range ... t_w(OUT)=120nS ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



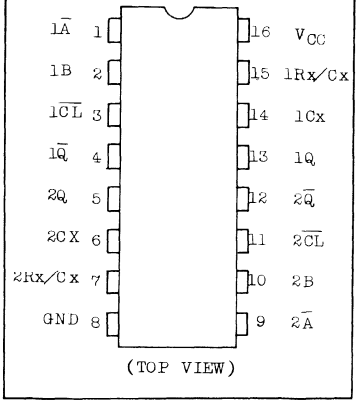
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



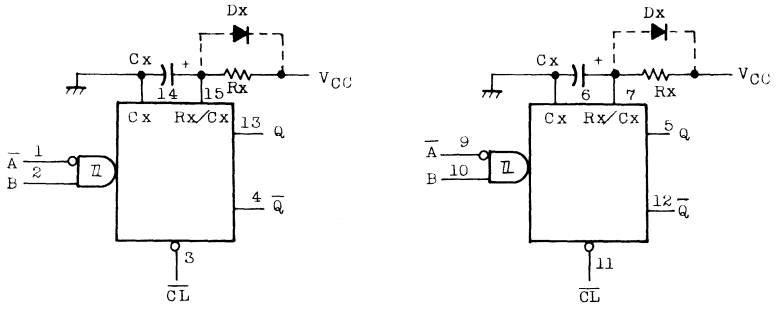
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

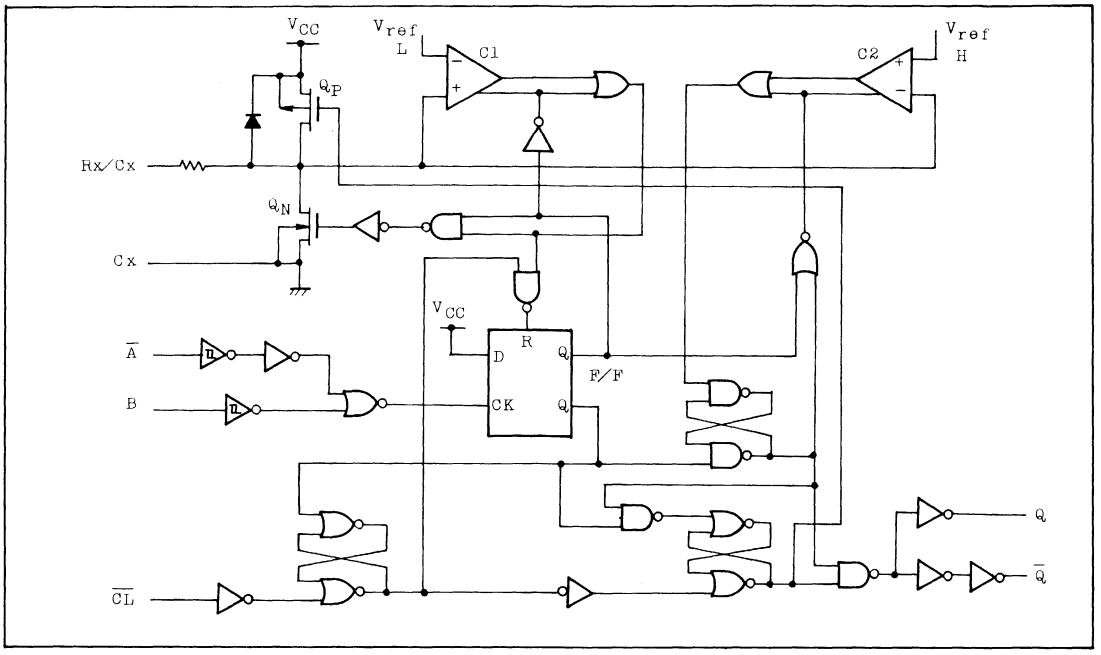
$$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning of to level of voltage supply becoming 0.4 V_{CC})

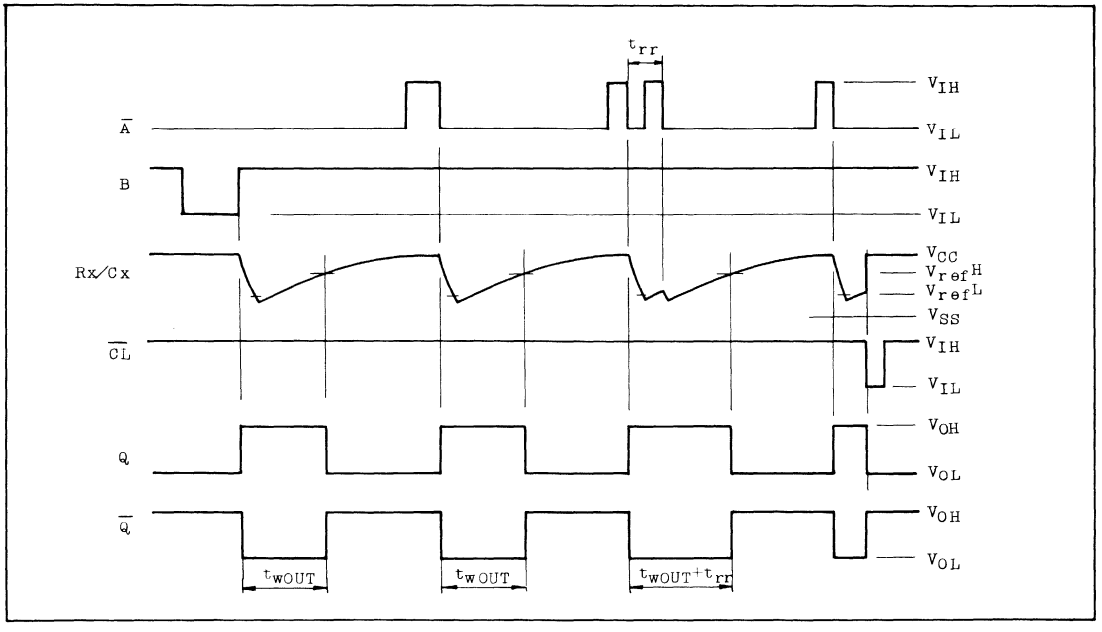
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

TC74HC423P/F

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition $\bar{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\bar{A}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.
After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.
By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.46 \quad Cx \; Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

(4) Reset operation

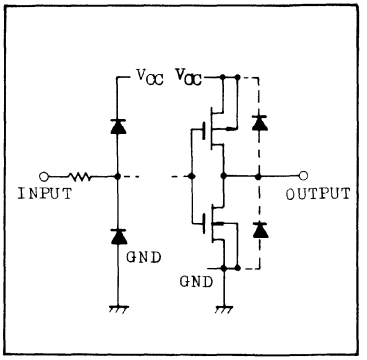
$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC423P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

* : Per Circuit

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Minimum Pulse Wdith ($\overline{A}$, B)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Pulse Width Error Between Circuits In Same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	ns
			6.0	-	63	-	-	-	
		Cx=0.01uF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	t_{wOUT} (MIN)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	t_{wOUT}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1uF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	113	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

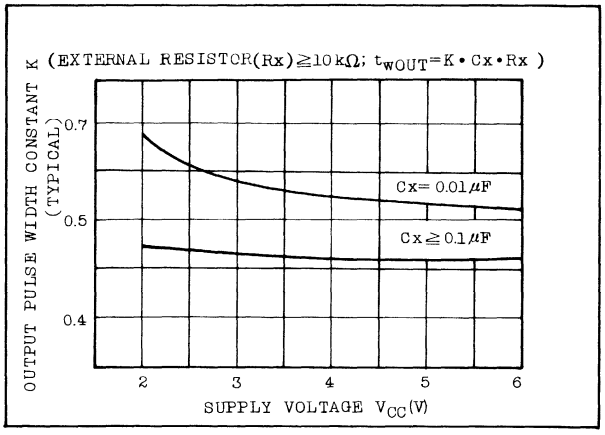
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2 \quad \text{(per monostable)}$$

(I_{CC}': Active Supply Current)

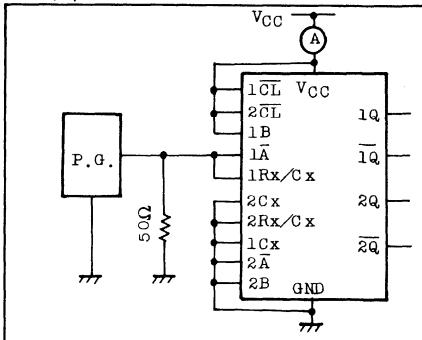
(Duty: %)

TC74HC423P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

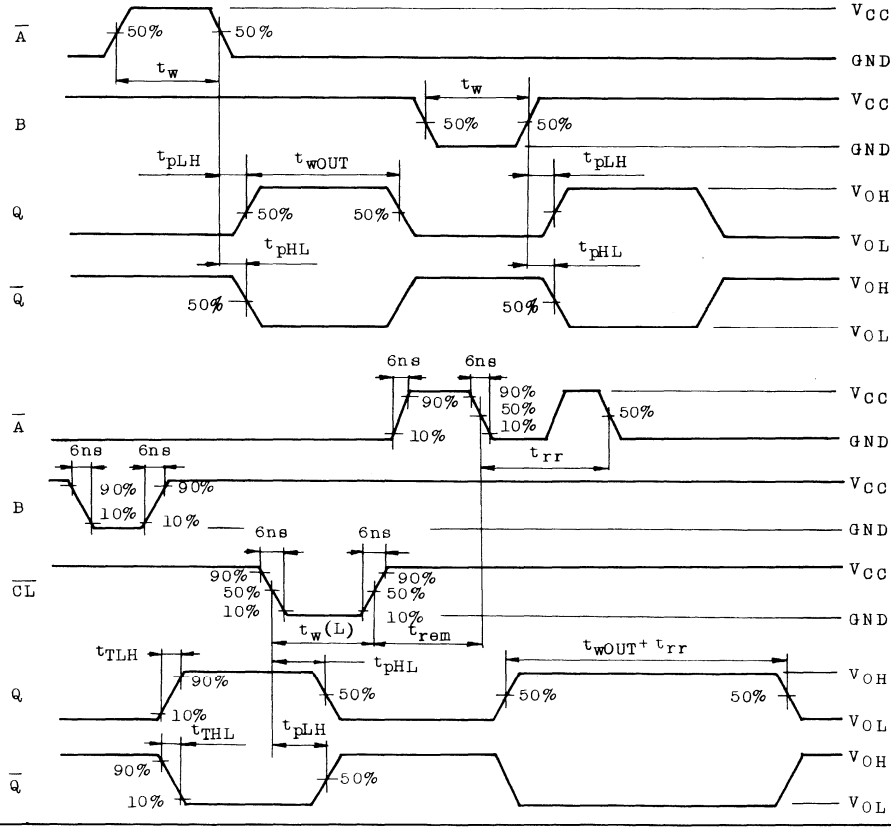


I_{CC}(opr.) TEST WAVEFORM

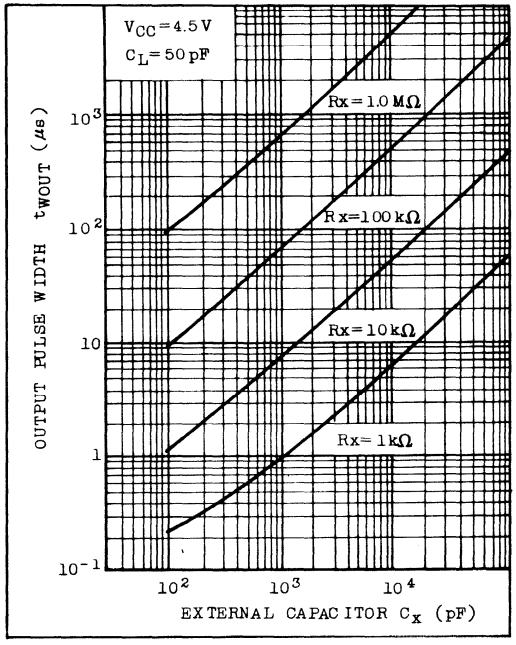


※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

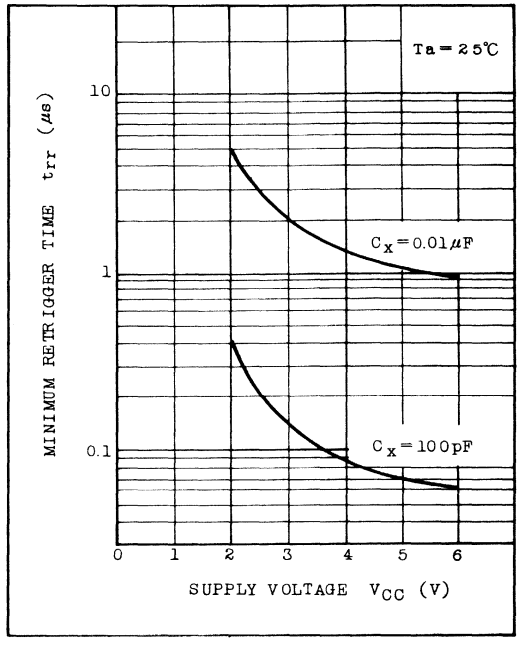
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)

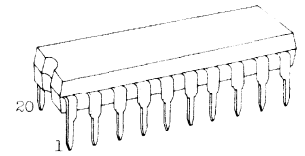


TC74HC540P/F
TC74HC541P/F

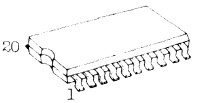
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC540P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HC541P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

The TC74HC540 and TC74HC541 are high speed CMOS OCTAL BUS BUFFER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC540 is non-inverting type. The TC74HC541 is inverting type. If either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)



MFP20(F20GA-P)

FEATURES:

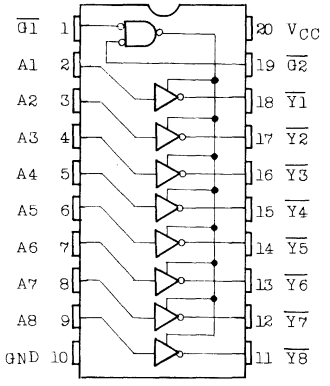
- High Speed ..... t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS540/541

NOTICE FOR APPLICATION

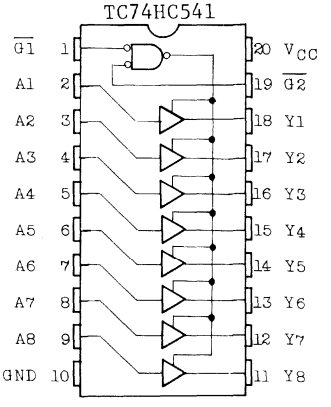
It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

PIN ASSIGNMENT (TOP VIEW)

TC74HC540



TC74HC541



TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: Don't Care

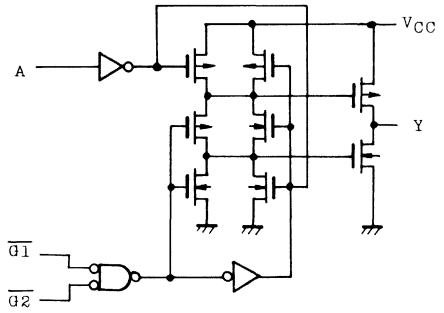
Z: High Impedance

*: Yn HC541
$\overline{Yn}$ HC540

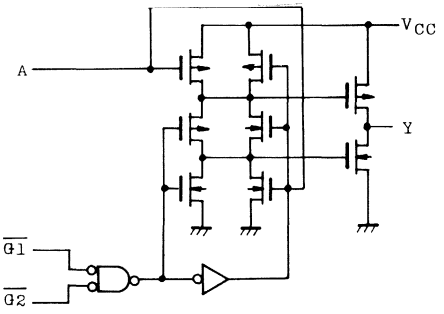
TC74HC540P/F
TC74HC541P/F

CIRCUIT DIAGRAM (Per Circuit)

TC74HC540



TC74HC541



ABSOLUTE MAXIMUM RATINGS

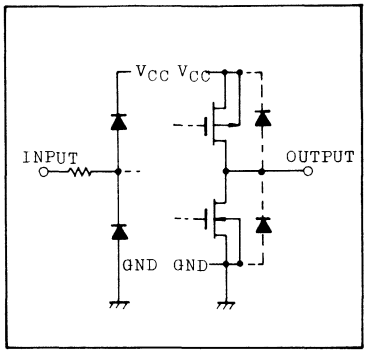
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	+20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC540P/F
TC74HC541P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HC540	2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HC541	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	

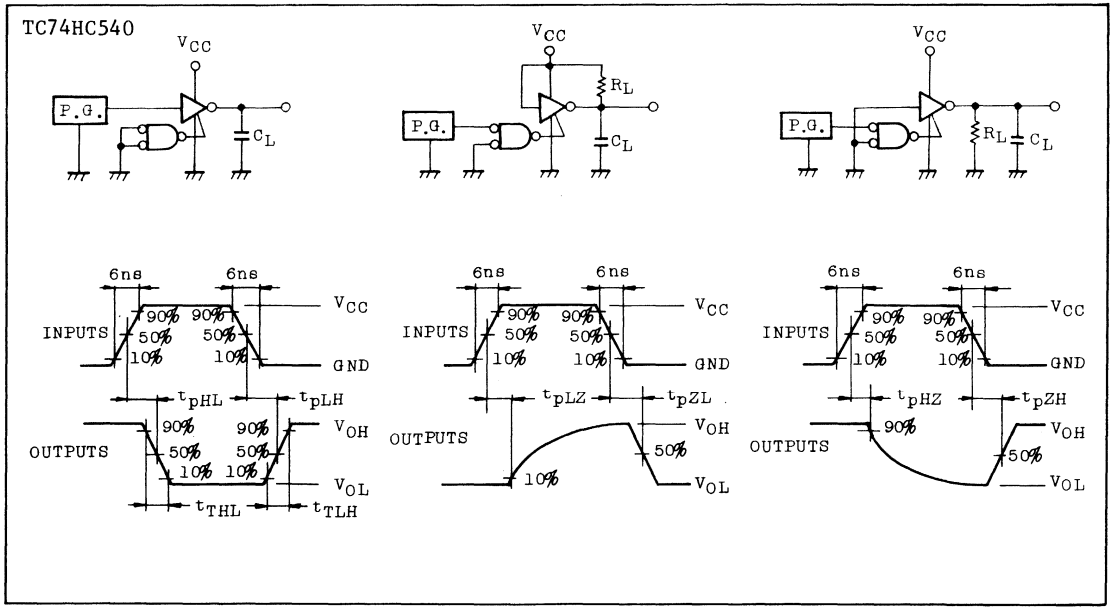
AC ELECTIRCAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Enable Time	t_{pLZ} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	88	160	-	200	
			4.5	-	22	32	-	40	
			6.0	-	19	27	-	34	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC540		-	33	-	-	-	
		TC74HC541		-	36	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Gate)}$$

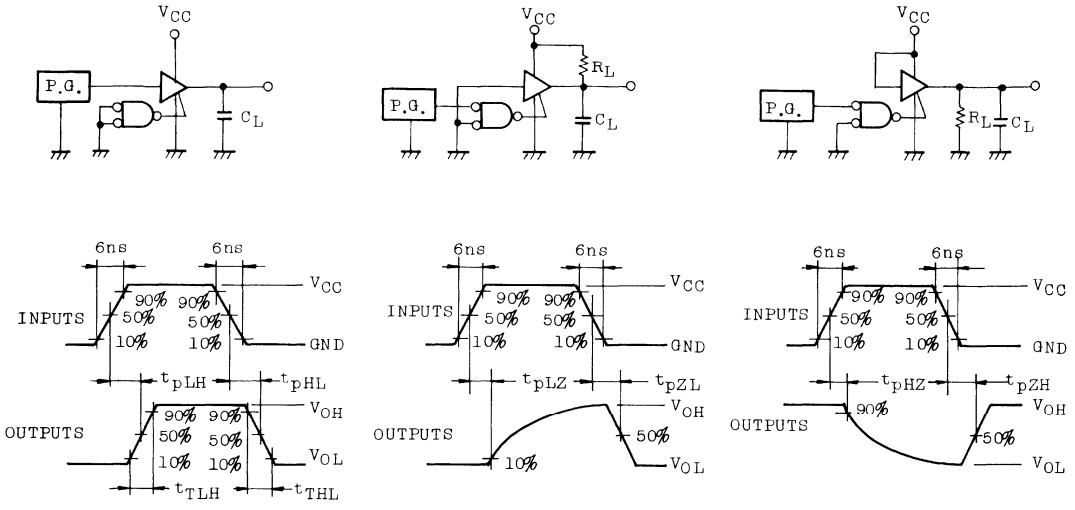
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM



TC74HC540P/F
TC74HC541P/F

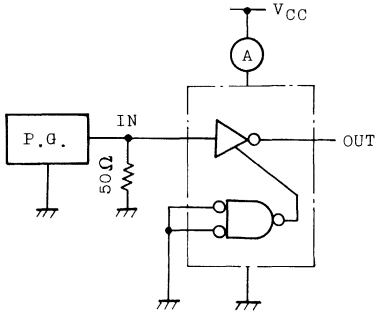
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM (Continued)

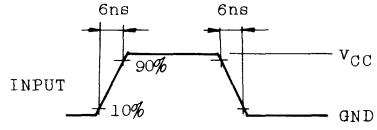
TC74HC541



$I_{CC(Opr.)}$ TEST CIRCUIT

TC74HC540





The other inputs are connected V_{CC} line or GND line.

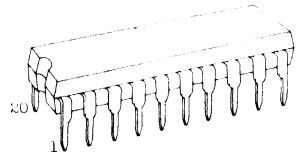
Test circuit of the TC74HC541 is the same as this.

TC74HCT540P/F
TC74HCT541P/F

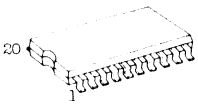
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT540P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HCT541P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

The TC74HCT540 and TC74HCT541 are high speed CMOS OCTAL BUS BUFFER fabricated with silicon gate C²MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT540 is non-inverting type. The TC74HCT541 is inverting type. If either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)



MFP20(F20GA-P)

FEATURES:

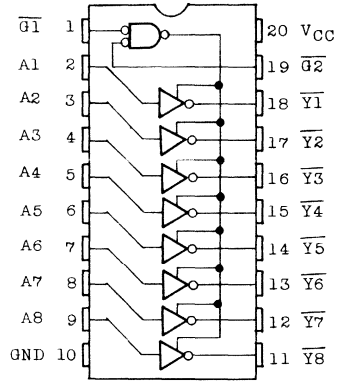
- High Speed ..... t_{pd}=13ns(T540) at V_{CC}=5V
  16ns(T541)
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS540/541

NOTICE FOR APPLICATION

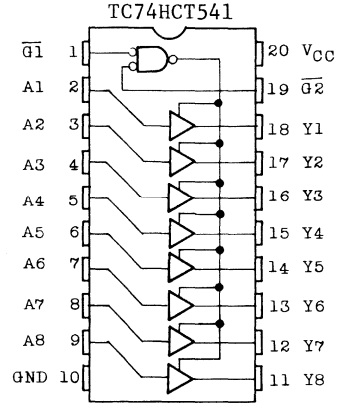
It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

PIN ASSIGNMENT (TOP VIEW)

TC74HCT540



TC74HCT541



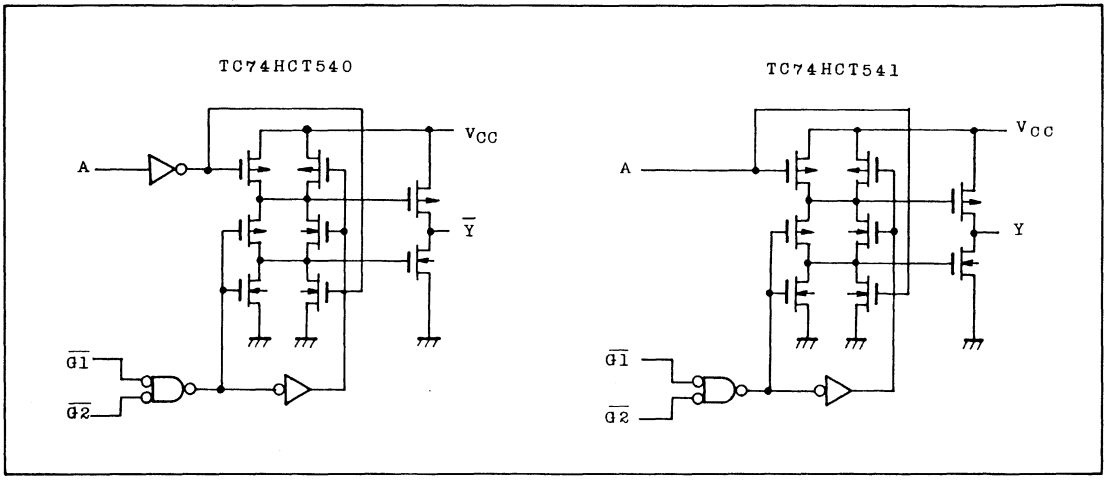
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: Don't Care
Z: High Impedance
*: Yn HCT541
$\overline{Yn}$ HCT540

TC74HCT540P/F
TC74HCT541P/F

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

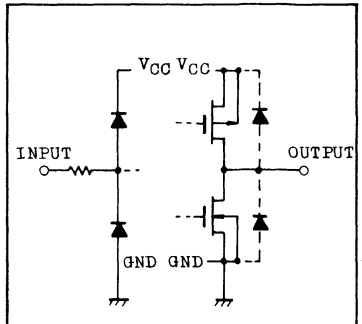
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT540P/F
TC74HCT541P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	
	I_C	Per Input: V_{IN}=2.4V or 0.5V Other Input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT540	4.5	-	16	26	-	32	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT541	4.5	-	19	30	-	36	
Output Enable Time	t_{pLZ} t_{pZH}	R_L=1kΩ	4.5	-	23	36	-	44	

TC74HCT540P/F
TC74HCT541P/F

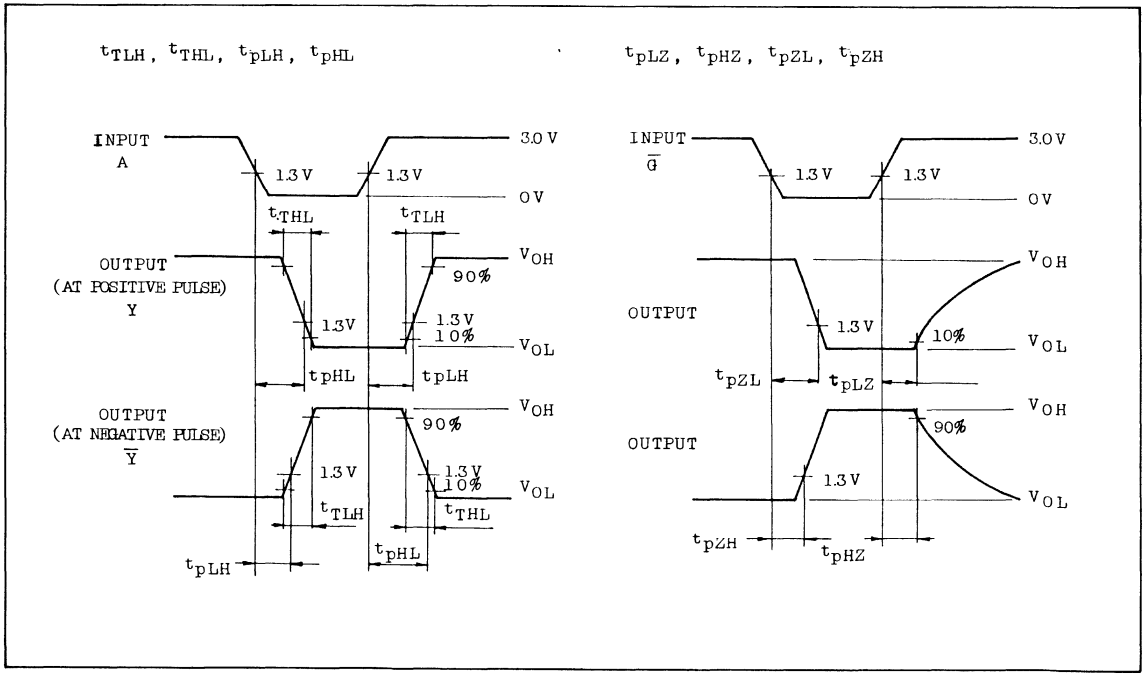
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	23	33	-	39	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HCT540		-	37	-	-	-	
		TC74HCT541		-	39	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

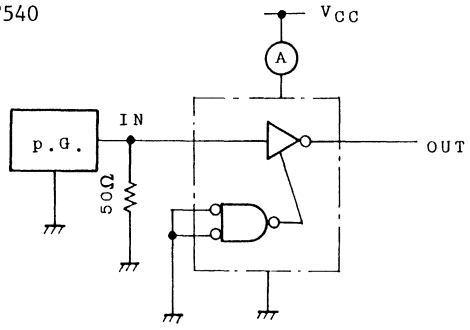
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Gate)}$$

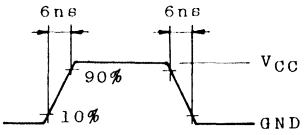
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT

TC74HCT540





The other inputs are connected V_{CC} line or GND line.

Test circuit of the TC74HCT541 is the same as this.

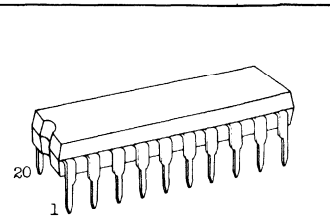
TC74HCT563P
TC74HCT573P

C²MOS DIGITAL INTEGRATED CIRCUIT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT563P INVERTING
TC74HCT573P NON-INVERTING

The TC74HCT563 and TC74HCT573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input(LE) and a output enable input($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs.
The three-state output configuration and the wide choice of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



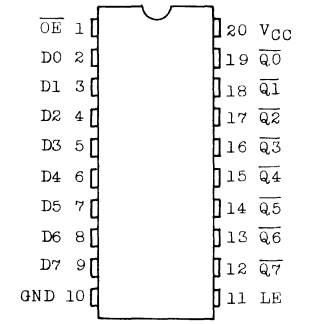
DIP20(3D20A-P)

FEATURES:

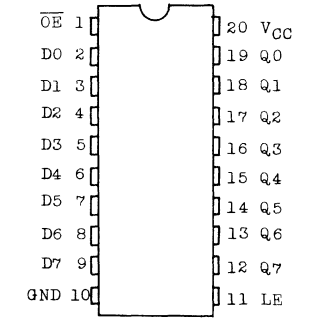
- High Speed ..... t_{pd}=20ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS563/573

PIN ASSIGNMENT (TOP VIEW)

TC74HCT563



TC74HCT573



TRUTH TABLE

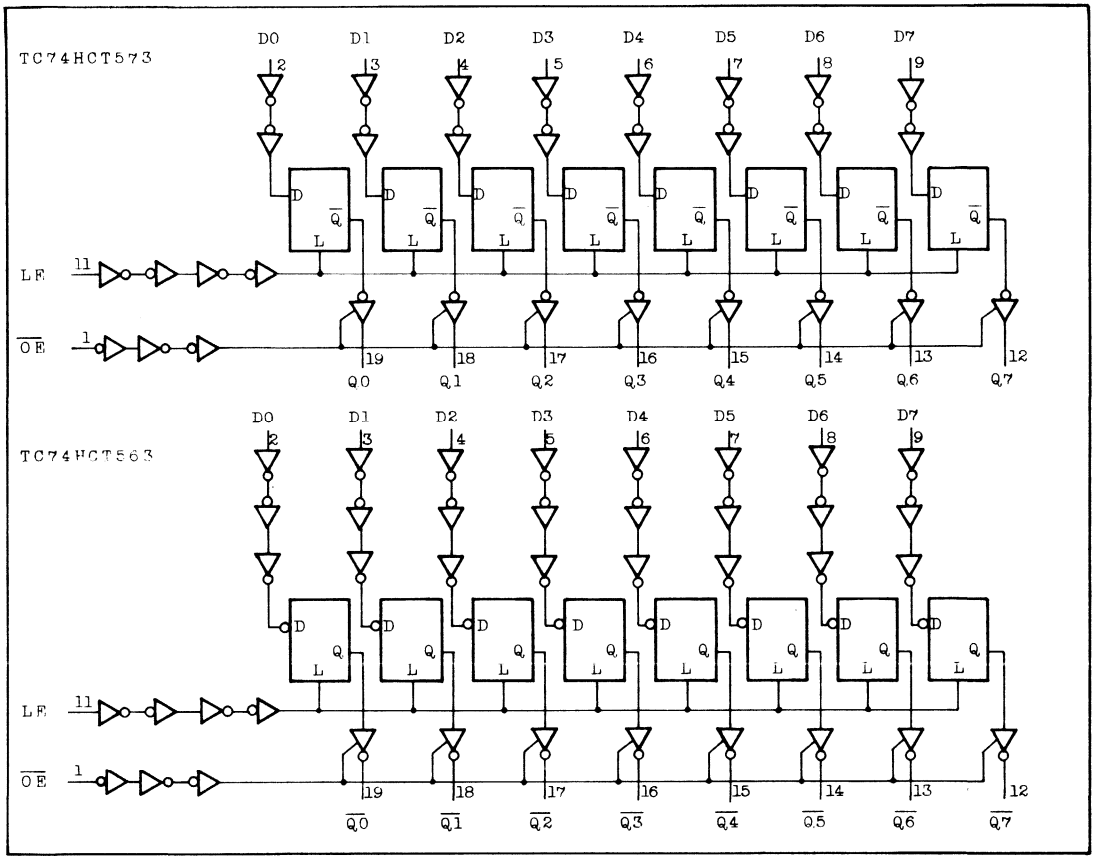
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HCT573)	$\overline{Q}$(HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	$\overline{Qn}$
L	H	L	L	H
L	H	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE

Qn : Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

TC74HCT563P
TC74HCT573P

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10 sec)	T_L	300	°C

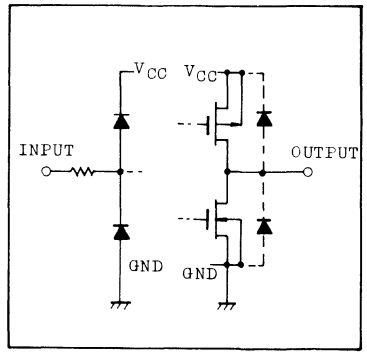
* 500mW in the range of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HCT563P
TC74HCT573P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500 (V_{CC}=4.5V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-		-		mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	19	ns
Propagation Delay Time (LE - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	24	35	-	44	
Propagation Delay Time (D - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	22	35	-	44	
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	
Minimum Set-up Time	t_s		4.5	-	2	10	-	13	
Minimum Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT563		-	41	-	-	-	
		TC74HCT573		-	41	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

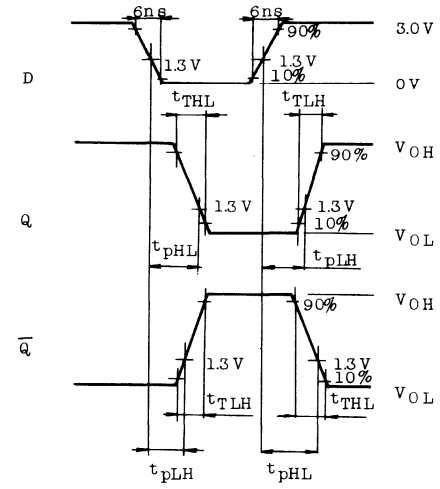
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

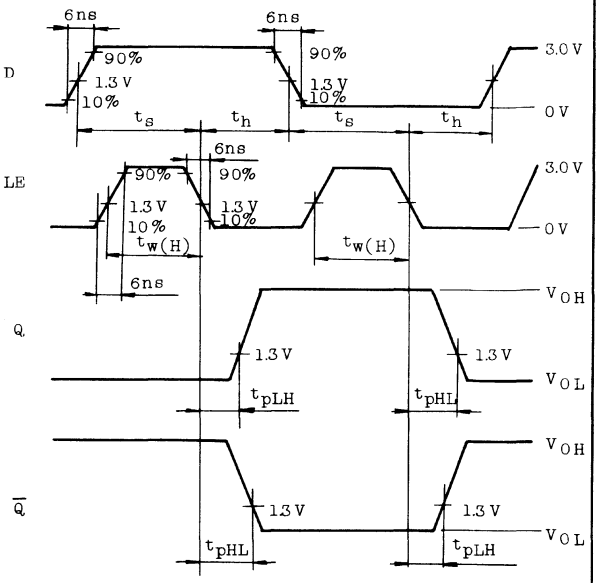
TC74HCT563P
TC74HCT573P

SWITCHING CHARACTERISTICS TEST WAVEFORM

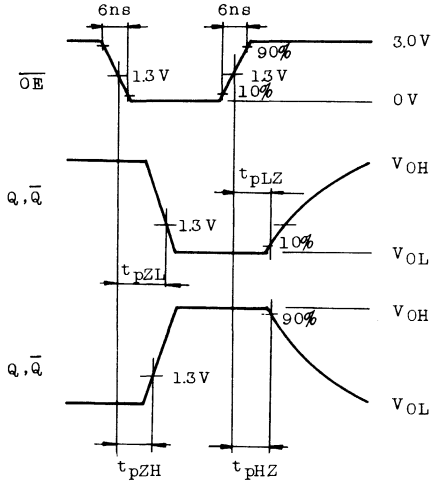
t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}

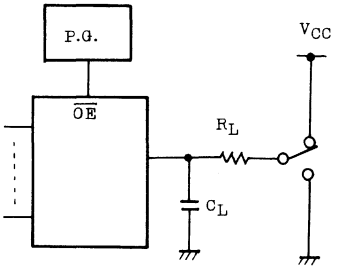


t_{pLH}, t_{pHL}(LE-Q,$\overline{Q}$), t_s, t_h, t_w



t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

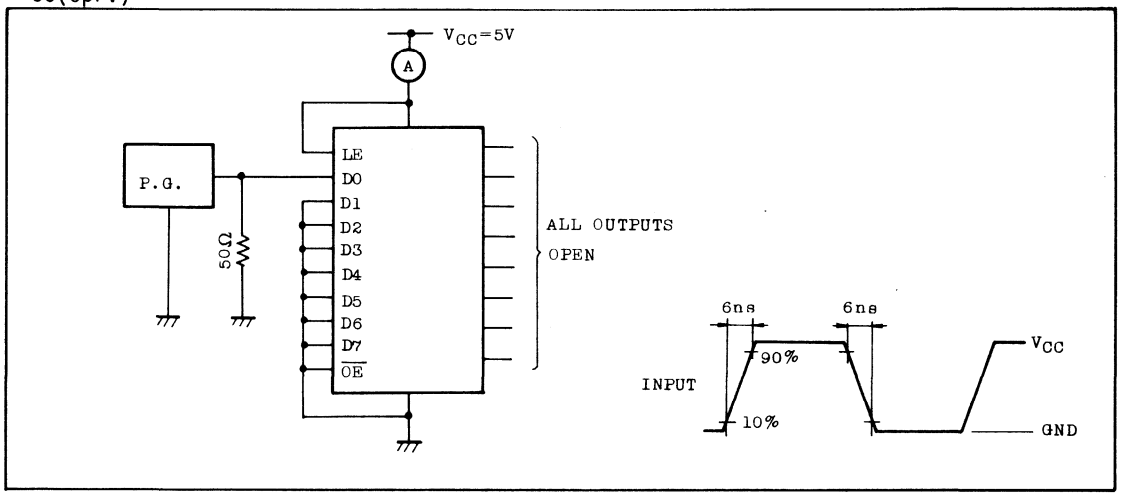




(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TC74HCT563P
TC74HCT573P

I_{CC}(Opr.) TEST CIRCUIT



TC74HCT564P
TC74HCT574P

C²MOS DIGITAL INTEGRATED CIRCUIT

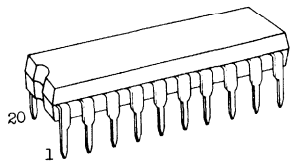
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT564P INVERTING
TC74HCT574P NON-INVERTING

The TC74HCT564 and TC74HCT574 are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology. These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These 8-bit D-type flip-flops are controlled by a clock input(CK) and a output enable input($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely (HCT574) or inversely (HCT564) to the logic state that were setup at the D inputs. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

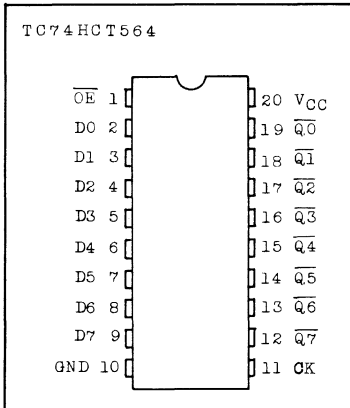
FEATURES:

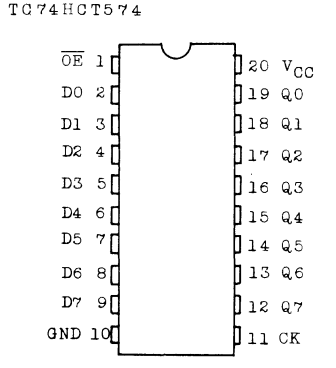
- High Speed ..... f_{MAX}=41MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
- Pin and Function Compatible with 74LS564/574



DIP20(3D20A-P)

PIN ASSIGNMENT (TOP VIEW)





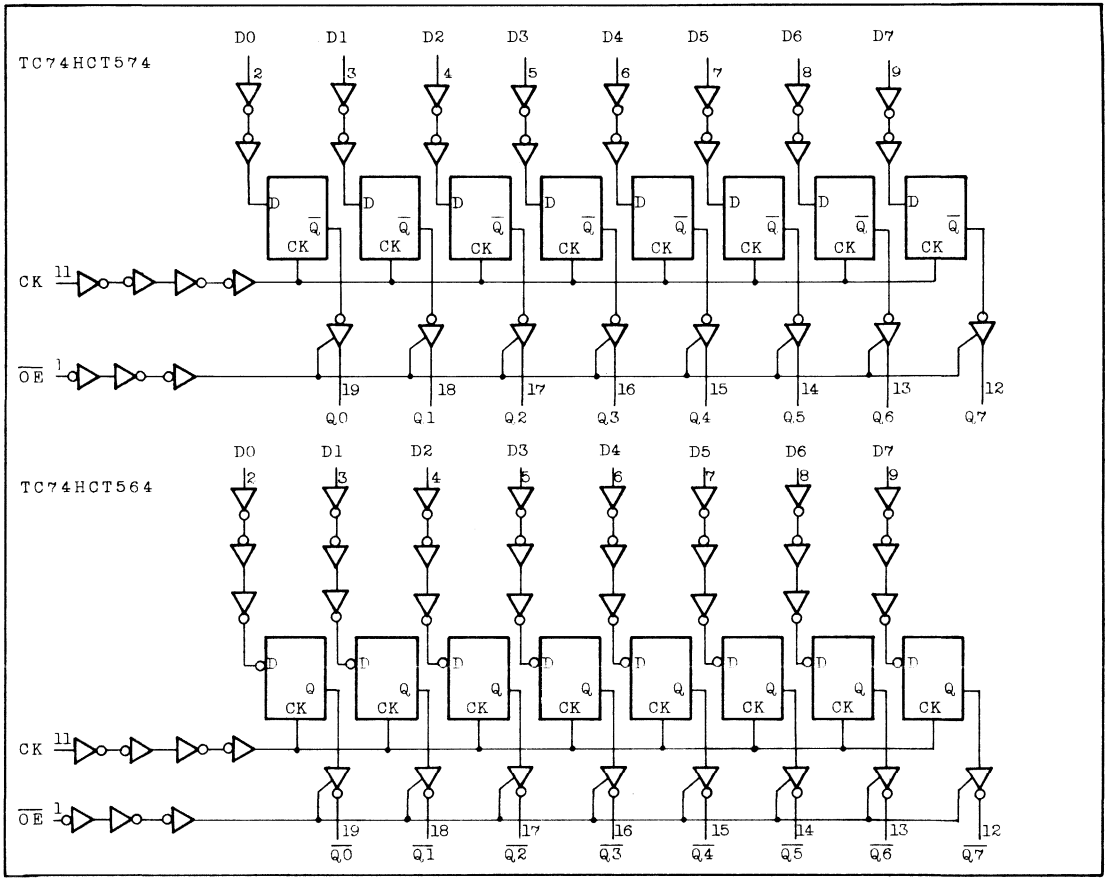
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(HCT574)	$\overline{Q}$(HCT564)
H	X	X	HZ	HZ
L	↑	X	Qn	Qn
L	↓	L	L	H
L	↓	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE
Qn : NO CHANGE

TC74HCT564P
TC74HCT574P

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10 sec)	T_L	300	°C

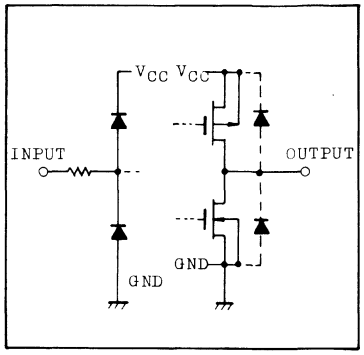
* 500mW in the ragne of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HCT564P
TC74HCT574P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-		-		mA

TC74HCT564P
TC74HCT574P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		4.5	-	26	41	-	51	ns
Maximum Clock Frequency	f_{MAX}		4.5	25	38	-	20	-	MHz
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		4.5	-	8	15	-	19	ns
Minimum Set-up Time	t_s		4.5	-	1	10	-	13	ns
Minimum Hold Time	t_h		4.5	-	-	5	-	5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Quiescent Supply Current	C_{PD}(1)	TC74HCT564		-	60	-	-	-	pF
		TC74HCT574		-	57	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Flip-Flop)}$$

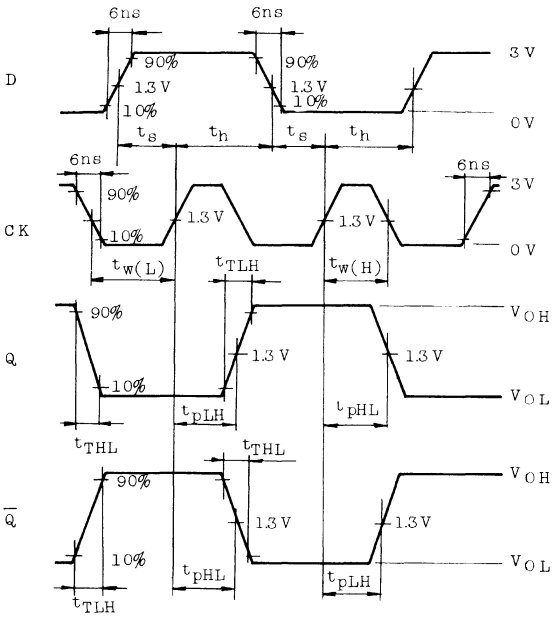
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation.

$C_{PD}(TOTAL)=40+20\times N$ [pF] (TC74HCT564)
$C_{PD}(TOTAL)=37+20\times N$ [pF] (TC74HCT574)

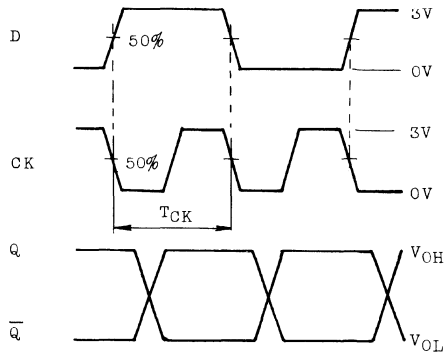
TC74HCT564P
TC74HCT574P

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



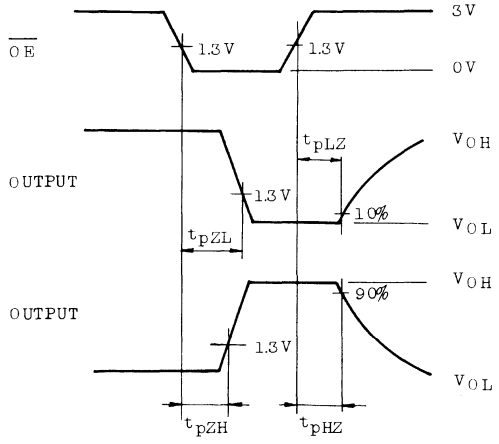
f_{MAX}.

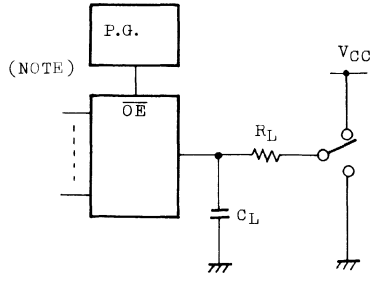


{CLOCK DUTY : 50%

$f_{MAX} = \frac{1}{T_{CK}}$

t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



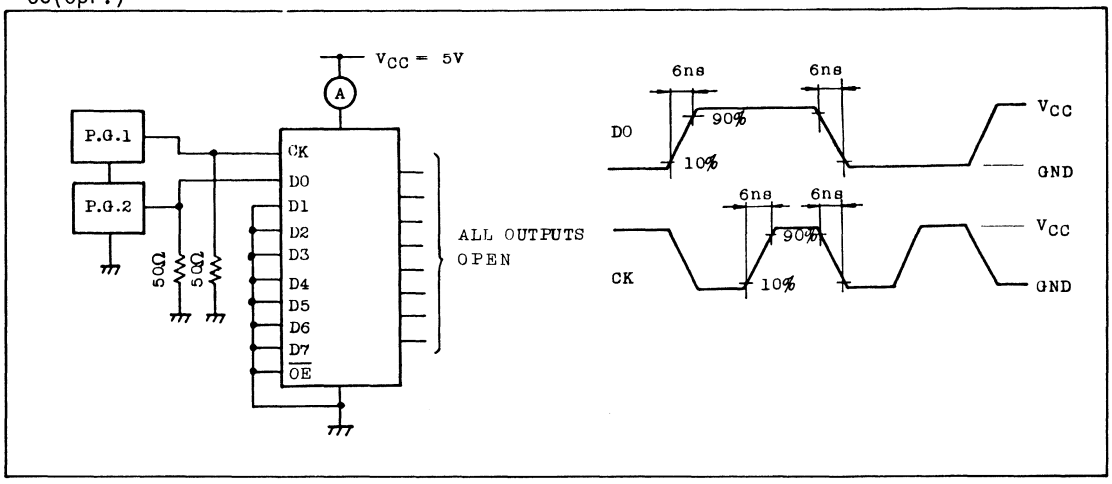


(NOTE)

EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TC74HCT564P
TC74HCT574P

I_{CC}(Opr.) TEST CIRCUIT



TC74HC590P

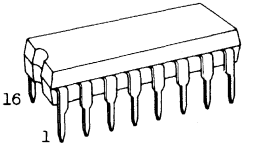
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC590P 8-BIT BINARY COUNTER/REGISTER WITH 3-STATE OUTPUTS

The TC74HC590 is a high speed CMOS 8-bit counter/register fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level. If Counter Clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronous to clock. Data of the internal counter are loaded to register at positive edge of Register Clock (RCK) and Outputs are controlled by Enable Control ($\overline{G}$). All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .... 10 LSTTL Loads (For RCO)
  15 LSTTL Loads (For QA ∿ QH)
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ∿ QH Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For RCO Output
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL(74LS590)



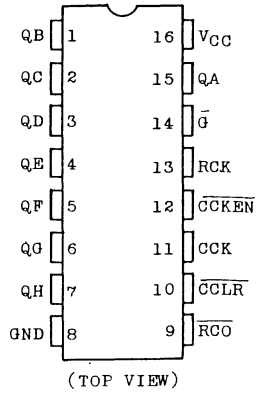
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 for QA∿QH ±20 for $\overline{RCO}$	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{STG}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

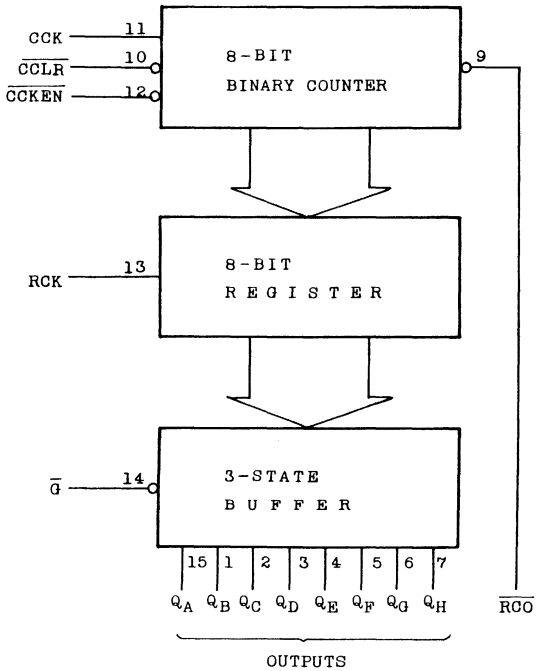
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↓	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	↑	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↓	ADVANCE ONE COUNT.
X	X	H	L	↑	NO COUNT
X	X	H	H	X	NO COUNT

X: Don't care

$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

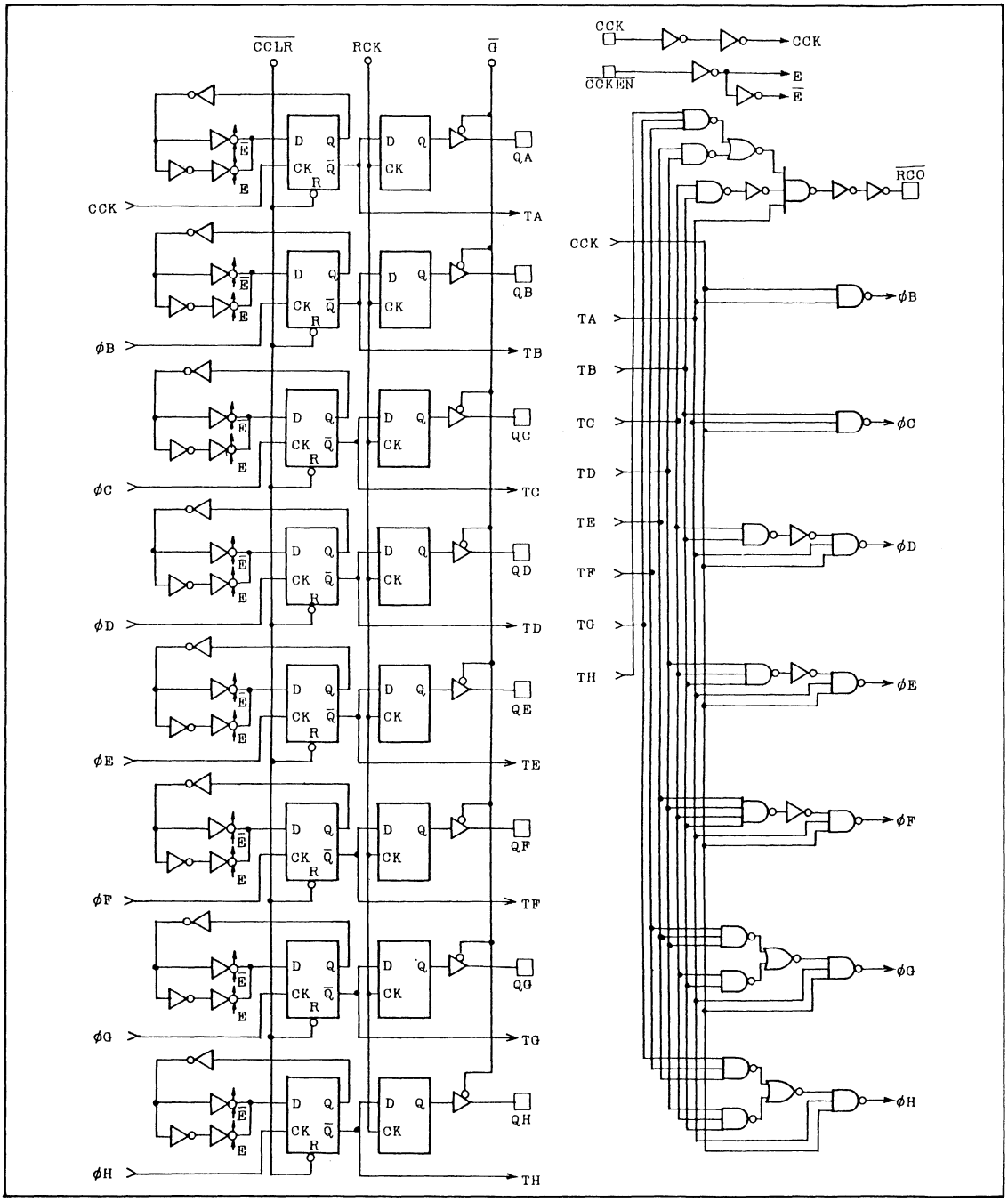
(QA' ∿ QH': Internal outputs of the counter)

BLOCK DIAGRAM



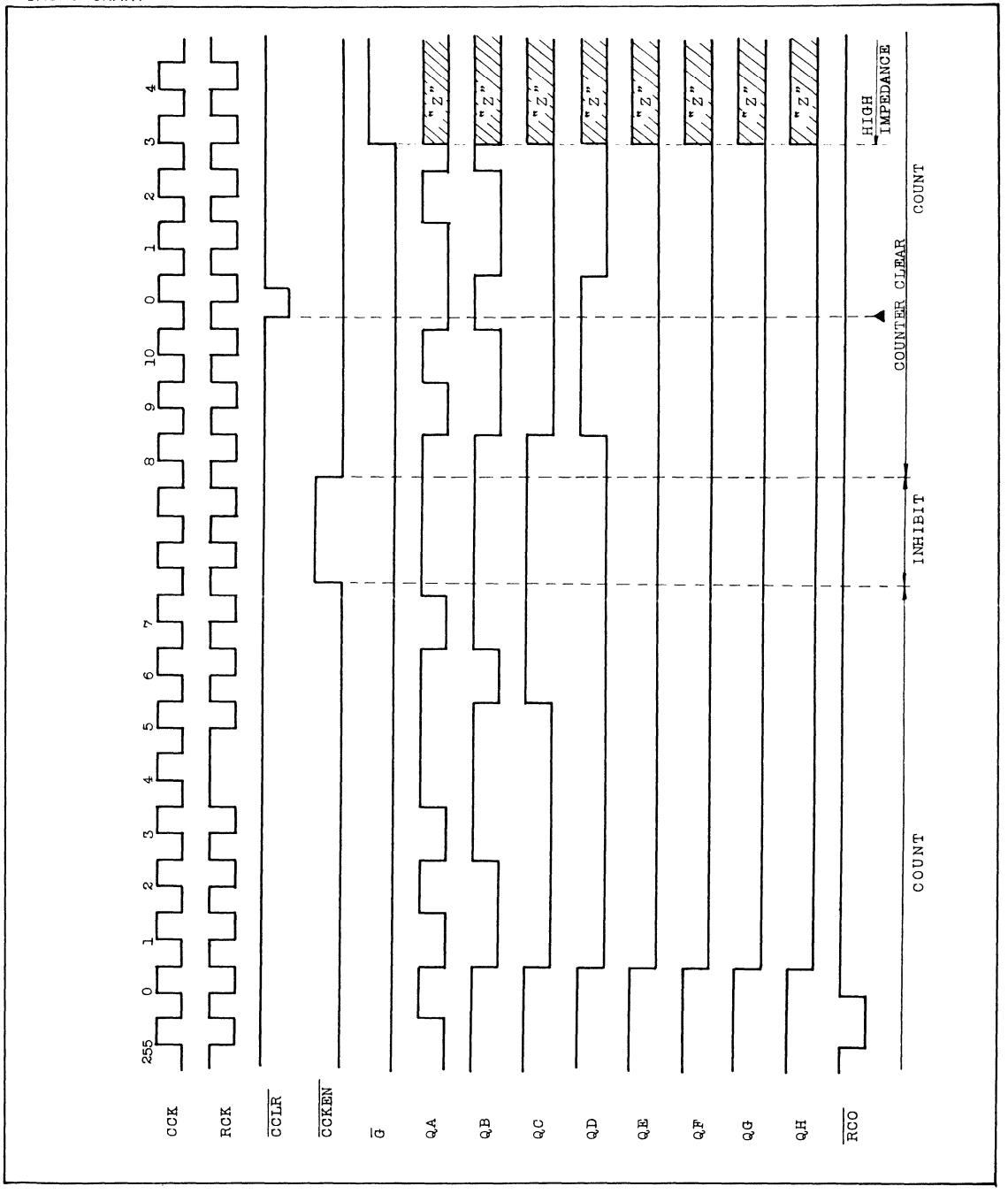
TC74HC590P

LOGIC DIAGRAM



TC74HC590P

TIMING CHART

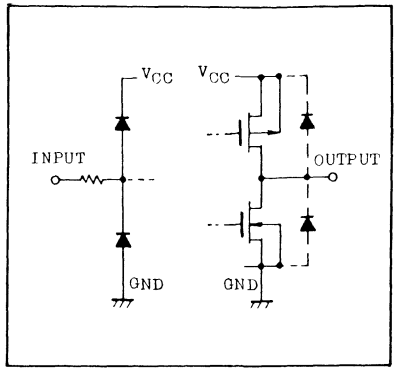


TC74HC590P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	-.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (CCLR - $\overline{RCO}$)	t_{pLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	32	-	16	-	
			6.0	24	38	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	48	125	-	160	ns
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	92	200	-	250	
			4.5	-	23	40	-	50	
			6.0	-	20	34	-	43	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Minimum Hold Time	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	RL=1kΩ	2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	RL=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	

TC74HC590P

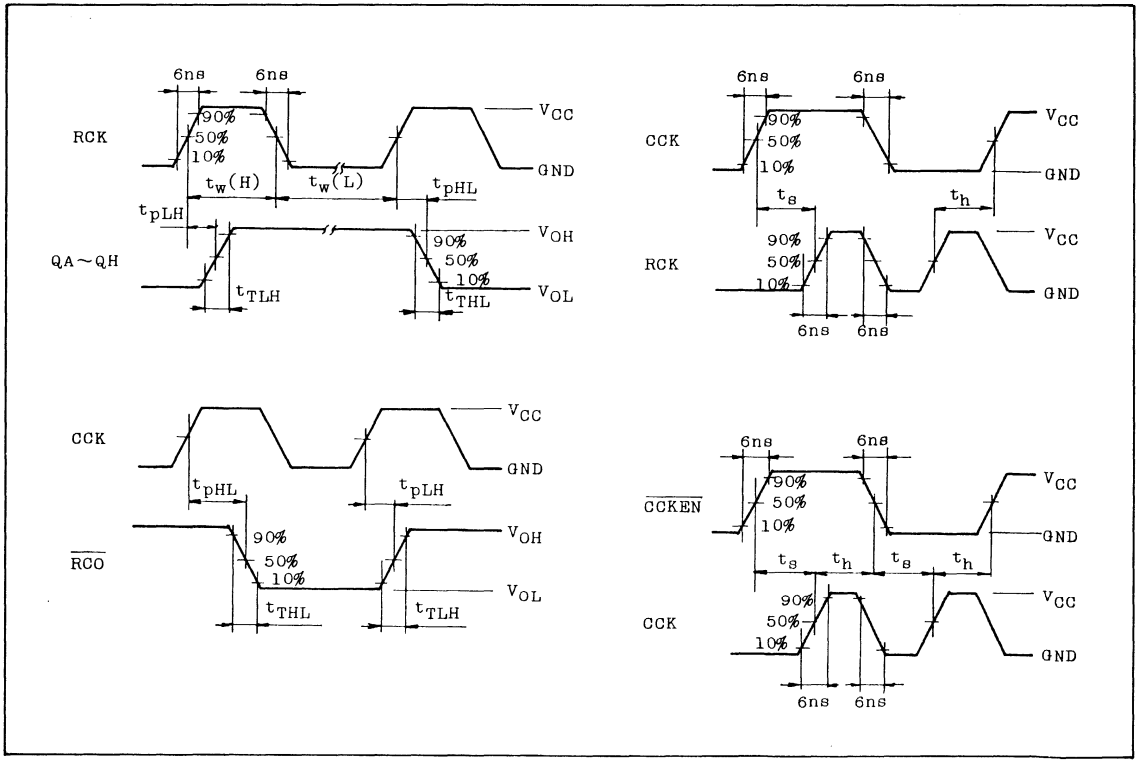
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40∿85°C		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}		-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$		-	95	-	-	-	

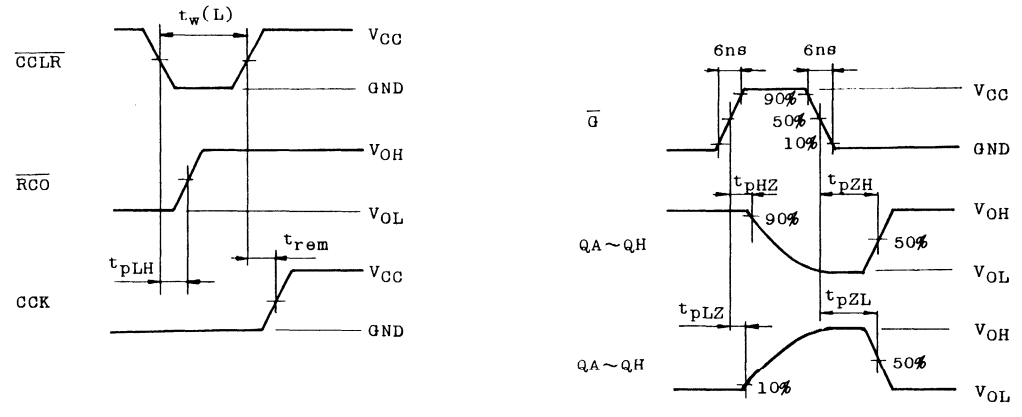
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

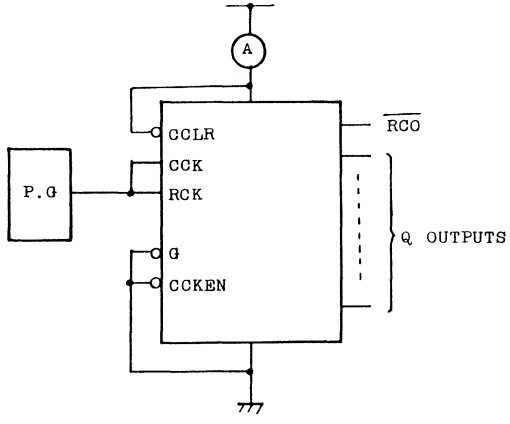
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST WAVEFORM



TC74HC592P

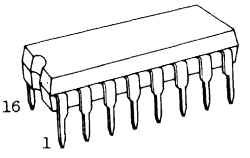
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC592P 8-BIT BINARY COUNTER WITH INPUT REGISTER

The TC74HC592 is a high speed CMOS 8-bit register/counter fabricated with silicon gate C^2MOS technology.
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level.
If Counter clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronous to clock.
Input A∿H are loaded to register at positive edge of Register Clock (RCK), and register outputs are loaded to Counter when Counter Load ($\overline{CLOAD}$) is held "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=38MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with LSTTL(74LS592)



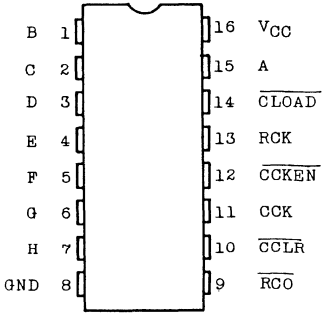
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC592P

TRUTH TABLE

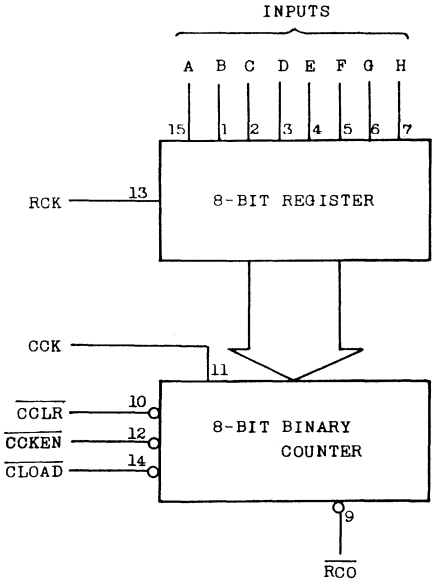
INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	REGISTER DATA IS LOADED INTO COUNTER.
X	H	L	X	X	COUNTER CLEAR
↑	H	H	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
↓	H	H	X	X	REGISTER STATE IS NOT CHANGED.
X	H	H	L	↑	COUNTER ADVANCES THE COUNT.
X	H	H	L	↓	NO COUNT
X	H	H	H	X	NO COUNT

X: Don't care

$\overline{RCO}=\overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

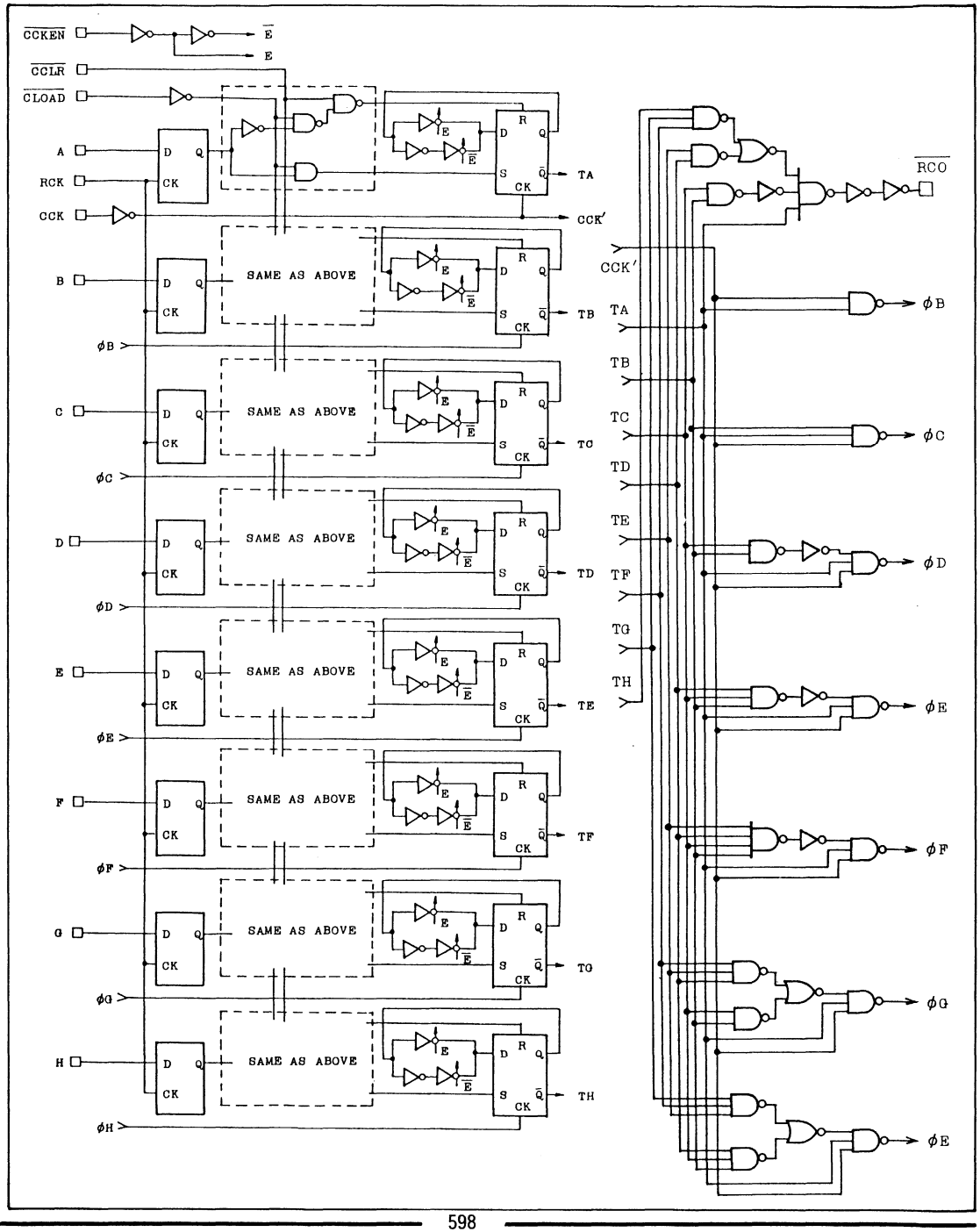
(QA' ∿ QH'; Internal outputs of the counter)

BLOCK DIAGRAM



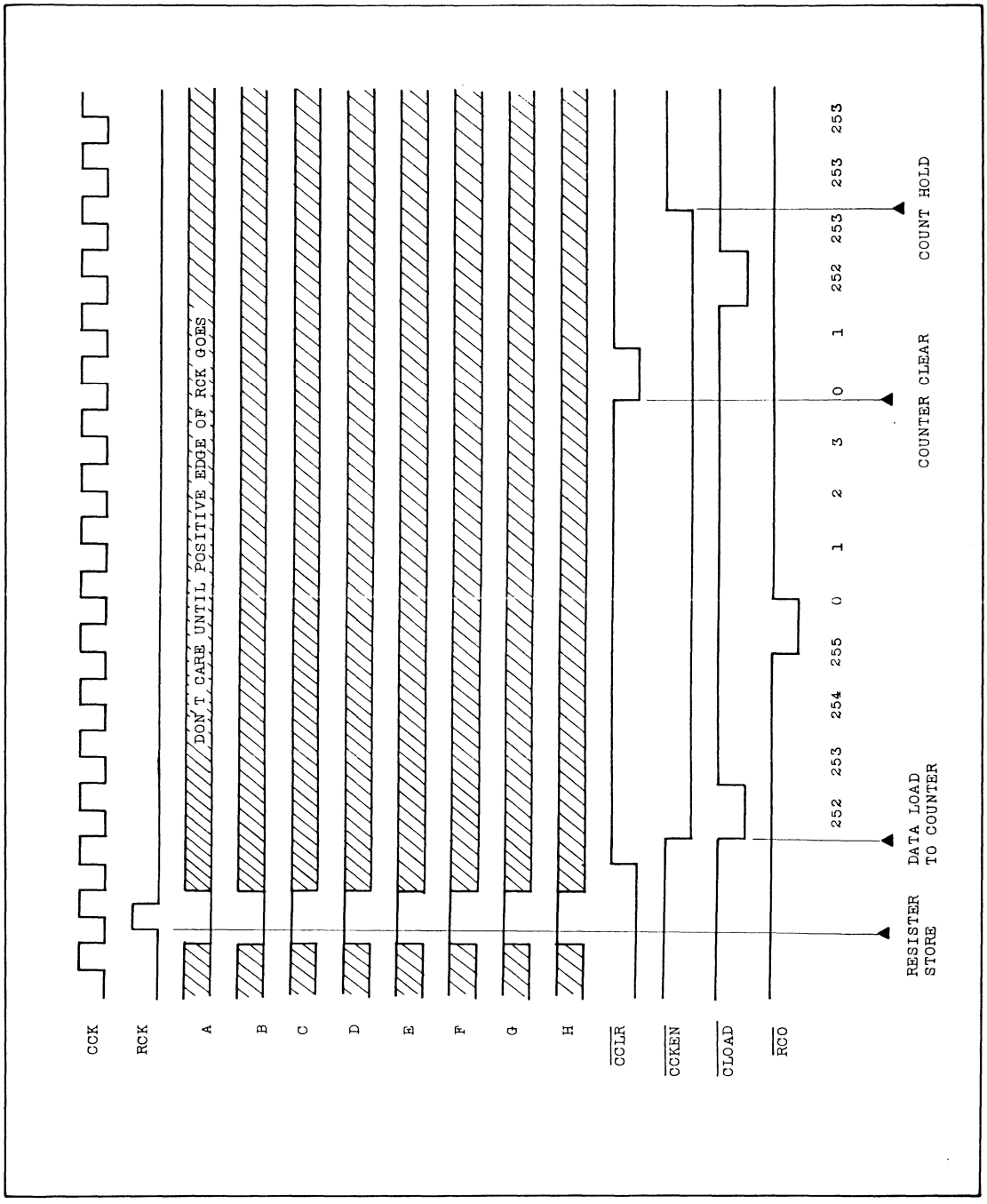
TC74HC592P

LOGIC DIAGRAM



TC74HC592P

TIMING CHART

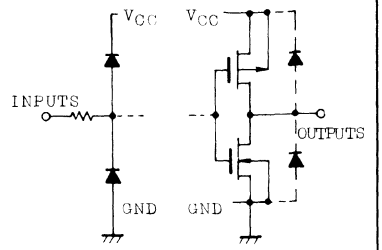


TC74HC592P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CLOAD}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	164	315	-	395	
			4.5	-	41	63	-	79	
			6.0	-	35	54	-	67	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (RCK - $\overline{RCO}$)	t_{pLH} t_{pHL}	$\overline{CLOAD}$="L"	2.0	-	188	360	-	450	
			4.5	-	47	72	-	90	
			6.0	-	40	61	-	77	
Maximum Clock Frequency	f_{MAX}		2.0	4	9	-	3.5	-	MHz
			4.5	22	34	-	18	-	
			6.0	26	42	-	21	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Pulse Width ($\overline{CLOAD}$)	$t_{w(L)}$		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Removal Time ($\overline{CLOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	t_s		2.0	-	32	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	17	-	16	
Minimum Set-up Time (RCK - $\overline{CLOAD}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Set-up Time (A∿H - RCK)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

TC74HC592P

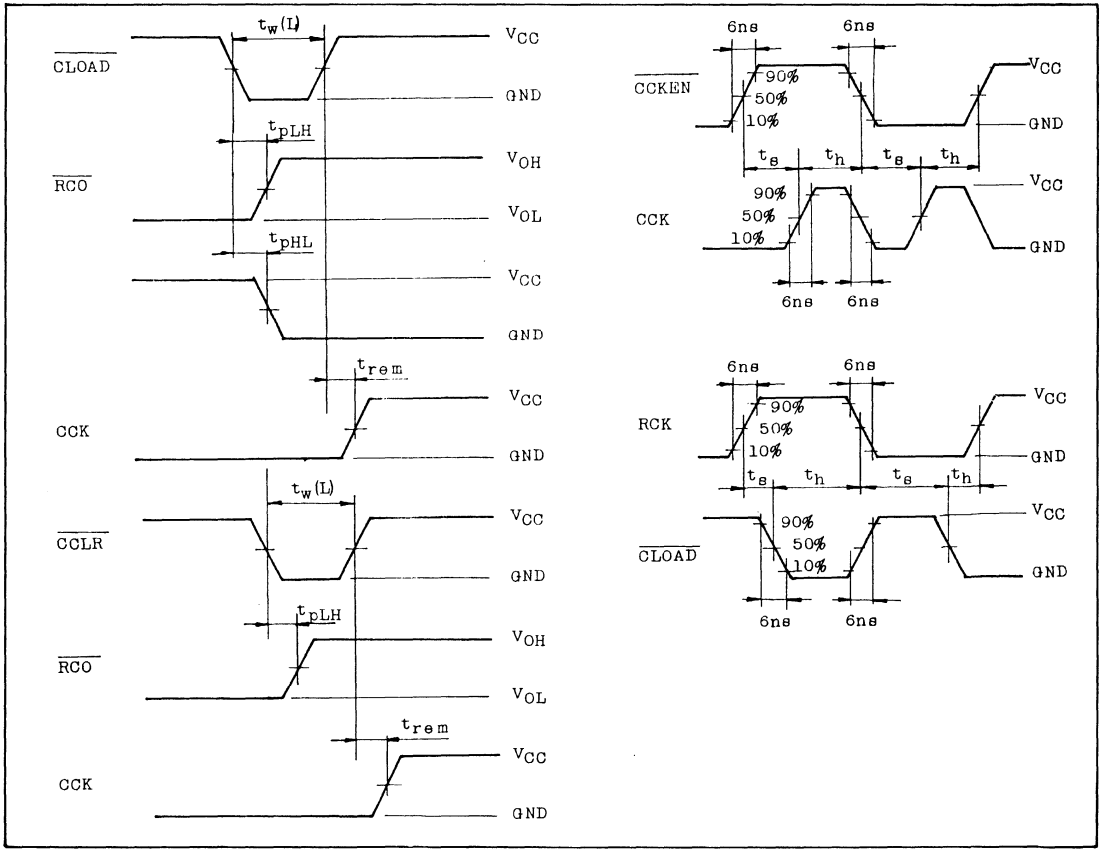
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Hold Time	t_h		2.0	-	-	25	-	30	ns
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	44	-	-	-	

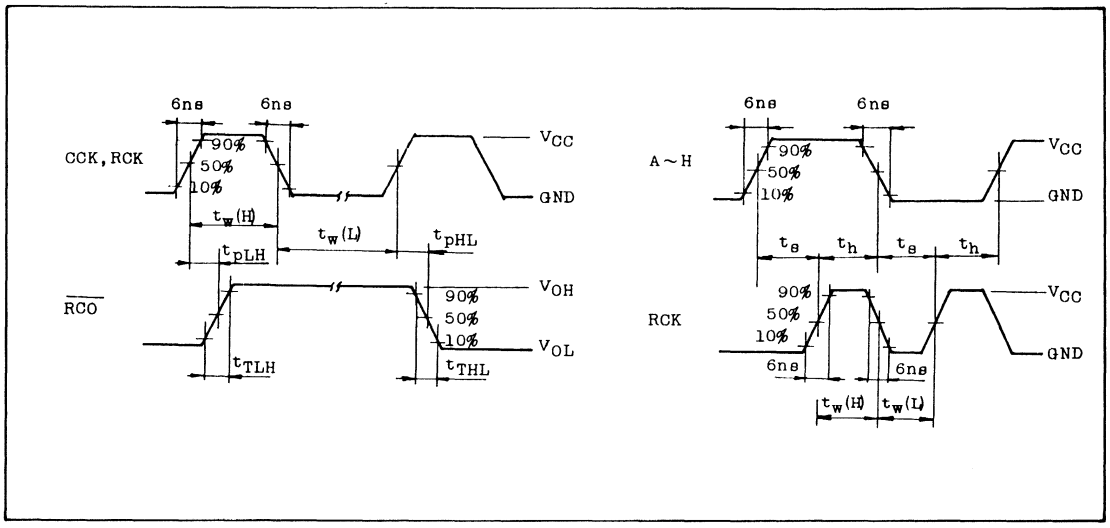
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

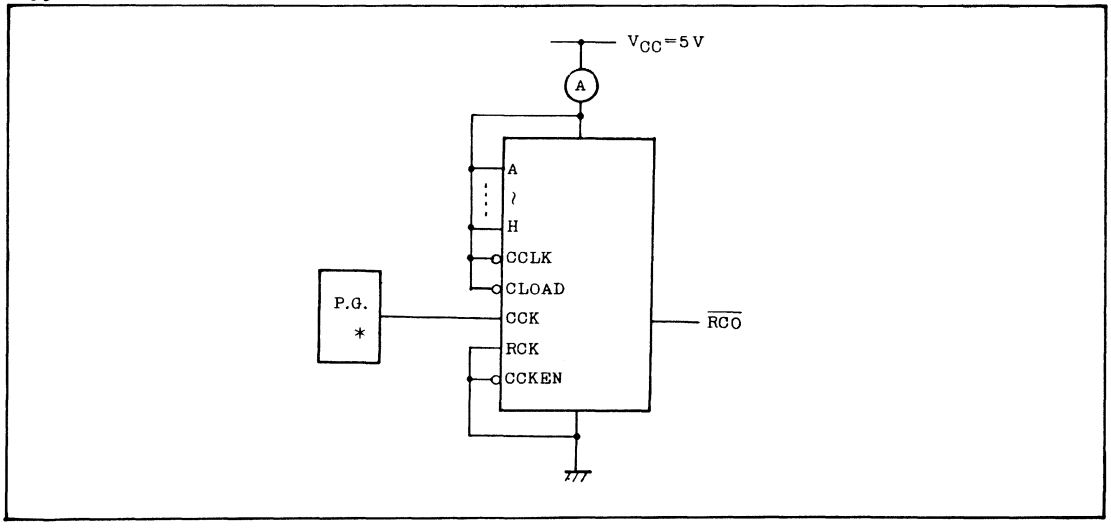
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT



TC74HC595P

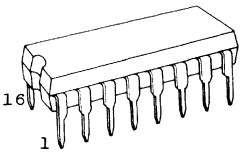
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC595P 8-BIT SHIFT REGISTER/LATCH (3-STATE)

The TC74HC595 is a high speed CMOS 8-BIT SHIFT REGISTER 1 LATCH fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC595P contains an 8-bit static shift register which feeds an 8-bit storage register. Shift operation is accomplished with the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independently, parallel outputs can be held a stable data during the shift operation. And, since the parallel outputs have 3-state construction, it can be directly connnected to 8-bit busline. This register can be applied to serial-to-parallel conversion, data receivers, etc. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ... 15 LSTTL Loads For QA ∿ QH
  10 LSTTL Loads For QH'
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.) For QA ∿ QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QH'
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS595



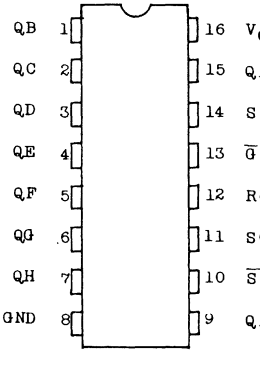
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current(QH')	I_{OUT}	±25	mA
DC Output Current(QA ∿ QH)	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{STG}	-65 ∿ 150	°C
Lead Temperature (10sec)	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



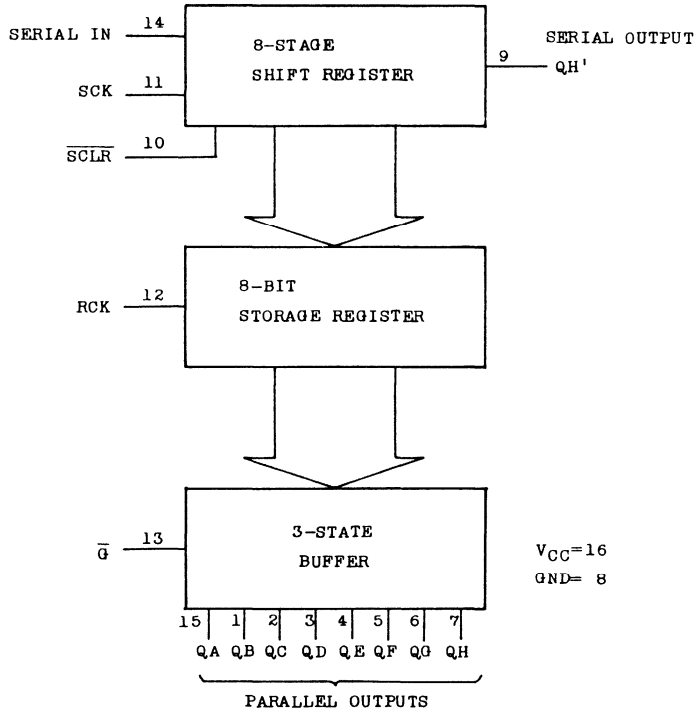
(TOP VIEW)

TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

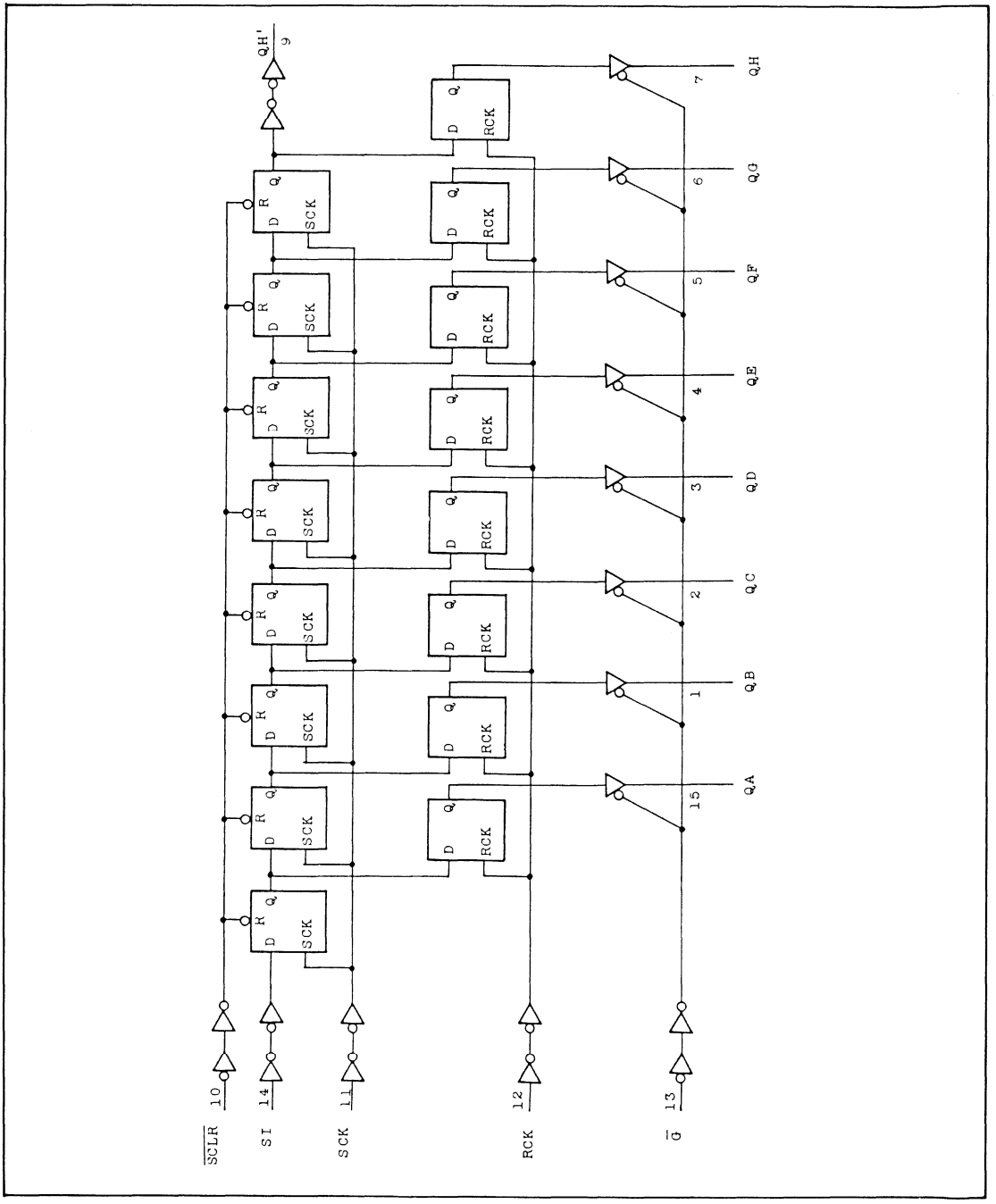
X : DON'T CARE

BLOCK DIAGRAM

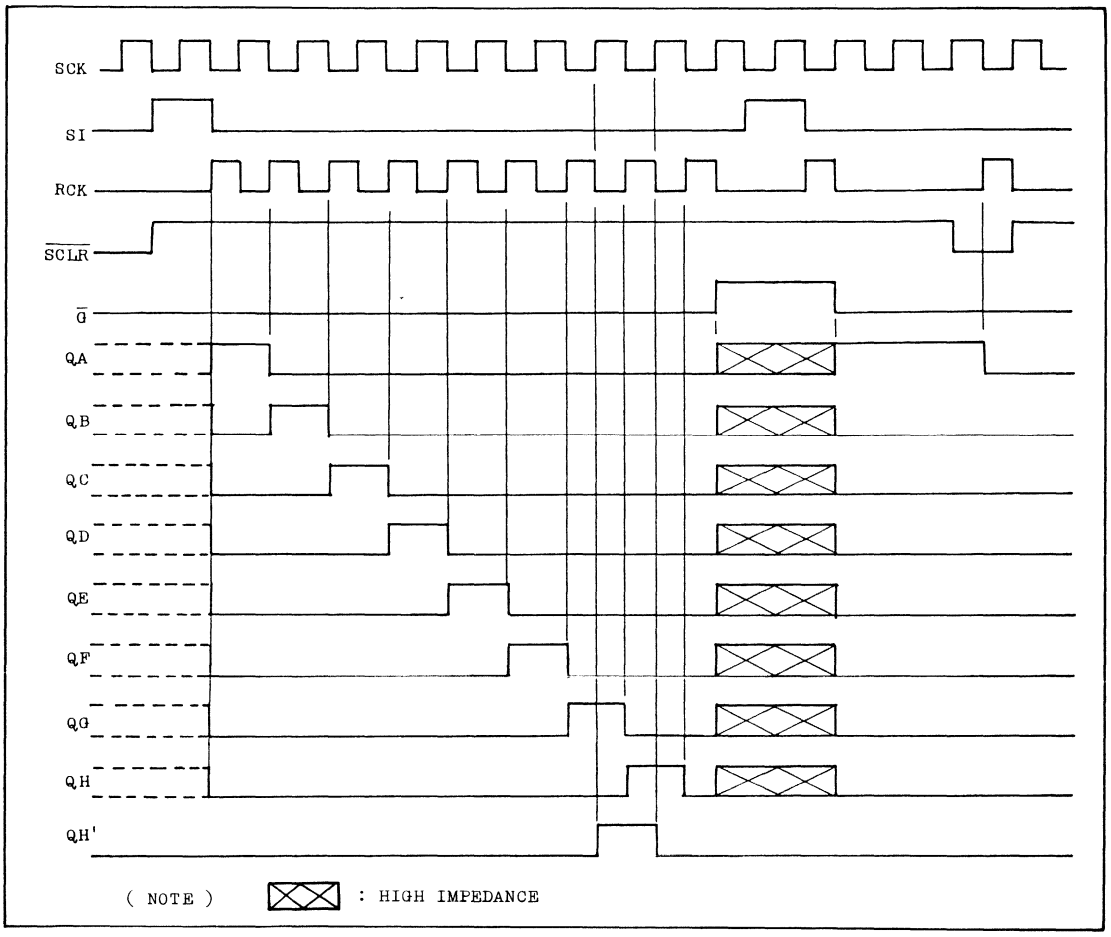


TC74HC595P

LOGIC DIAGRAM



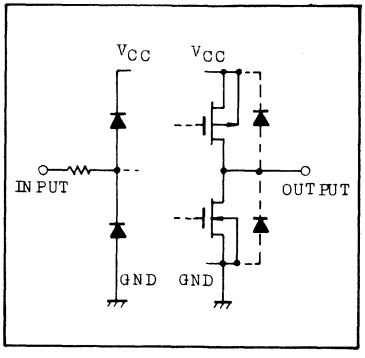
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC595P

DC ELECTRICAL CHARACTERITICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		QH'	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		QH'	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Bus Terminal 3-State Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Qn)	t_{TLH}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
	t_{THL}		6.0		6	10	-	13	
Output Transition Time (QH')	t_{TLH}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (SCK - QH')	t_{pLH}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
	t_{pHL}		6.0	-	17	27	-	34	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Propagation Delay Time ($\overline{SCLR}$ - QH')	t_{pHL}		2.0	-	88	175	-	220	ns
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (RCK - Qn)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	25	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (SCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (SI - SCK)	t_s		2.0	-	20	50	-	65	
			4.5	-	5	10	-	13	
			6.0	-	4	9	-	11	
Minimum Set-up Time (SCK - RCK)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time ($\overline{SCLR}$ - RCK)	t_s		2.0	-	44	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Clear Removal Time	t_{rem}		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	64	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	

TC74HC595P

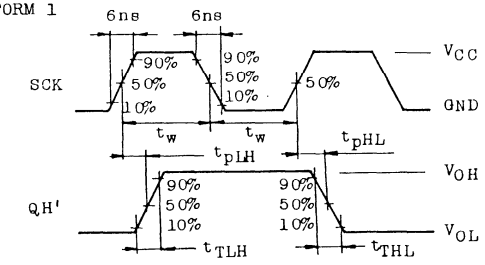
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40~85°C		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}		-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}		-	254	-	-	-	

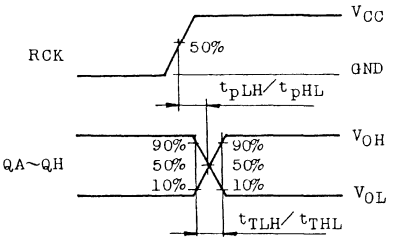
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

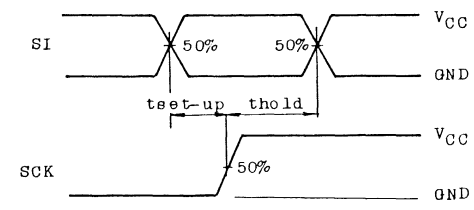
WAVEFORM 1



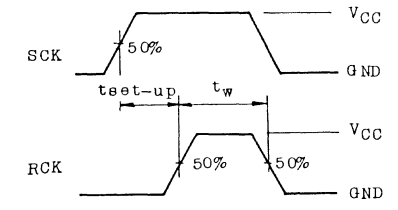
WAVEFORM 2



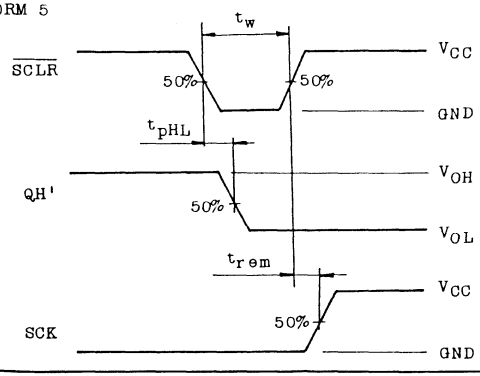
WAVEFORM 3



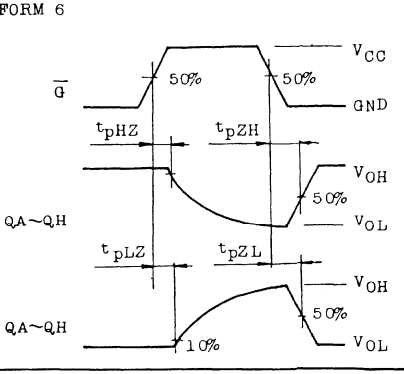
WAVEFORM 4



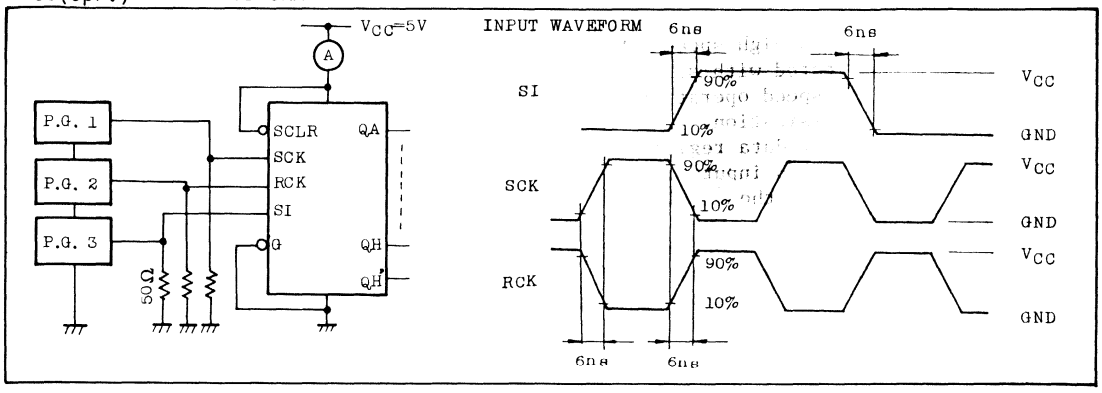
WAVEFORM 5



WAVEFORM 6



I_{CC}(Opr.) TEST WAVEFORM



TC74HC597P/F

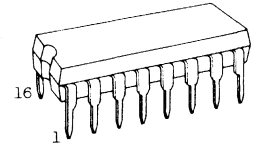
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC597P/F 8-BIT LATCH/SHIFT REGISTER

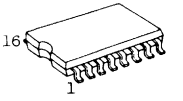
The TC74HC597 is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of an 8-bit data register feeding an 8-bit shift register.
The parallel data of A∿H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{SLOAD}$ input is held low, the input register data is stored into shift register. When $\overline{SLOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear inputs sets 8-bit shift register to zero.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balnaced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS597



DIP16(3D16A-P)



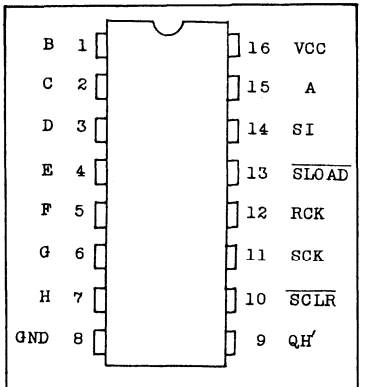
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



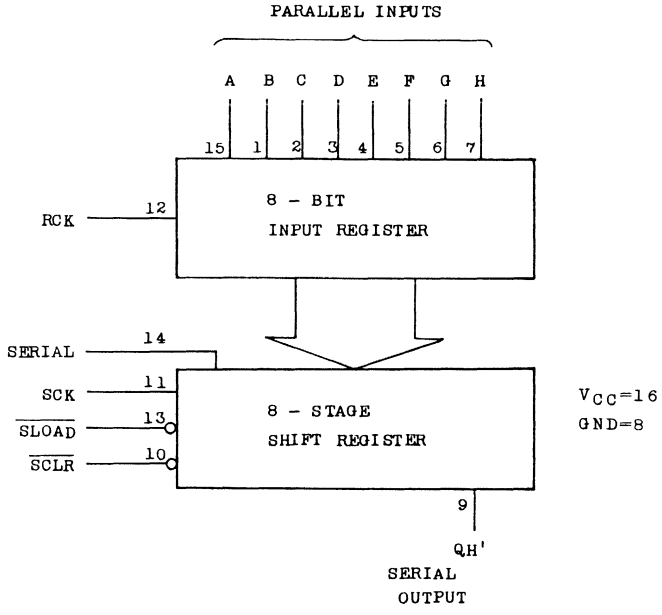
(TOP VIEW)

TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S.R.
L	↑	H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	H	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	H	X	State of S.R. is not changed.
X	X	X	X	↑	Input data on A~H line is stored into input register
X	X	X	X	↓	Storage register state is not changed.

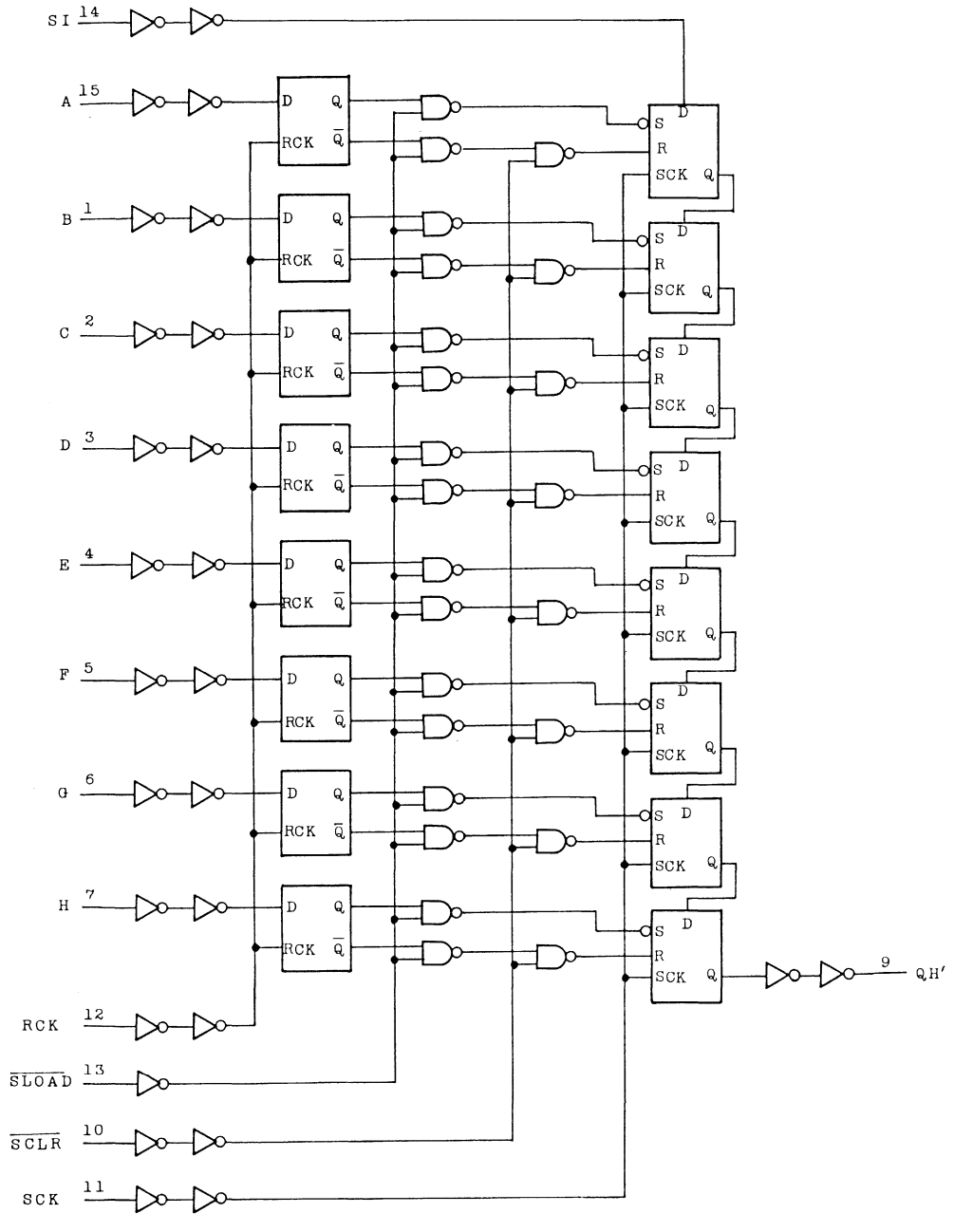
X; Don't Care

BLOCK DIAGRAM



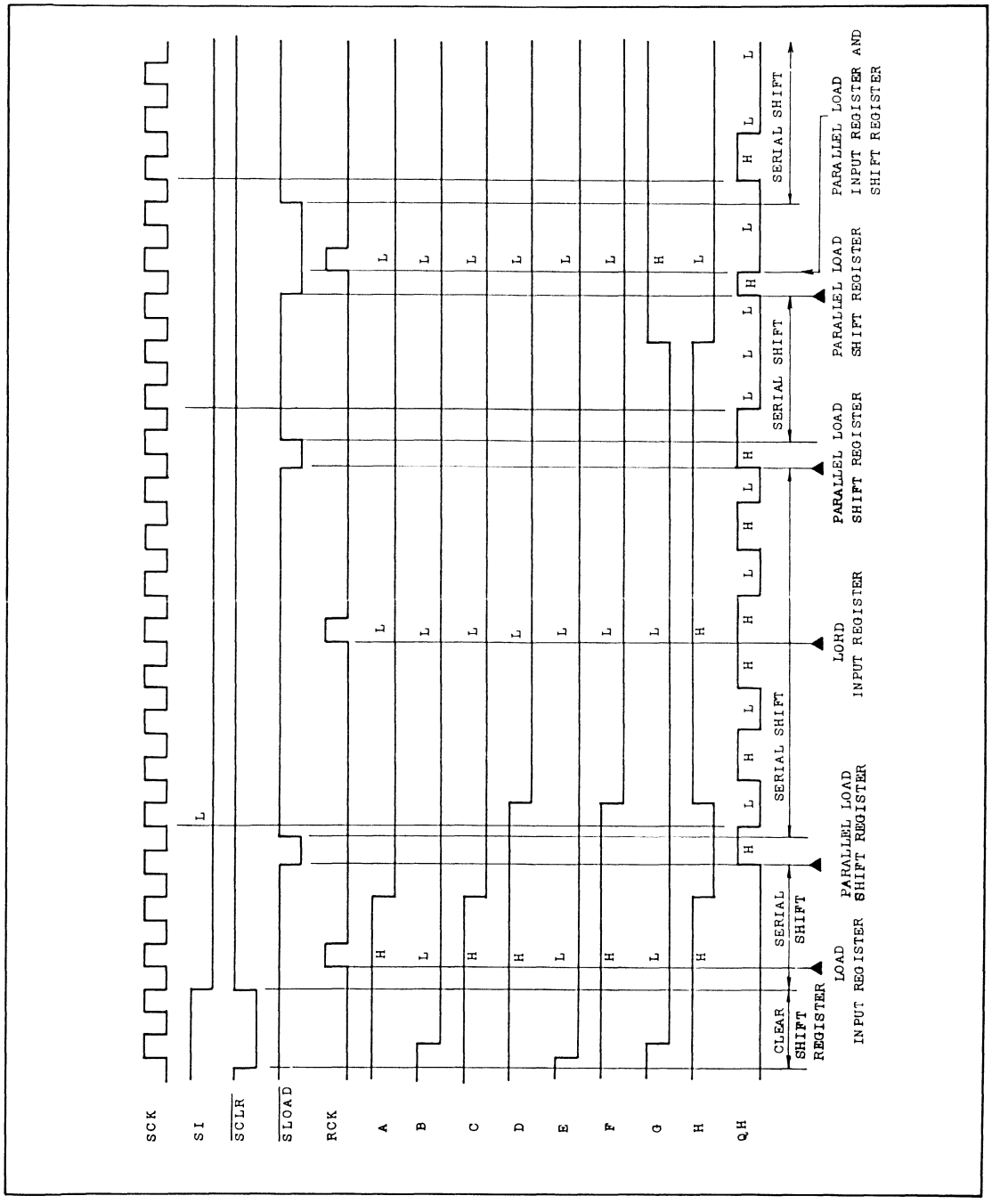
TC74HC597P/F

LOGIC DIAGRAM



TC74HC597P/F

TIMING CHART

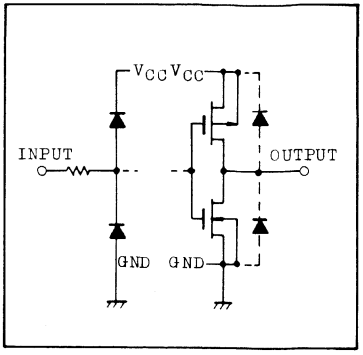


TC74HC597P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (SCK - QH')	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{SCLR}$ - QH')	t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Propagation Delay Time ($\overline{SLOAD}$ - QH')	t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (RCK - QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$="L"	2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width (SCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SLOAD}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (RCK - $\overline{SLOAD}$)	t_s		2.0	-	50	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Minimum Set-up Time (SI - SCK)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (A ... H - RCK)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{SCLR}$, $\overline{SLOAD}$)	t_{rem}		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	

TC74HC597P/F

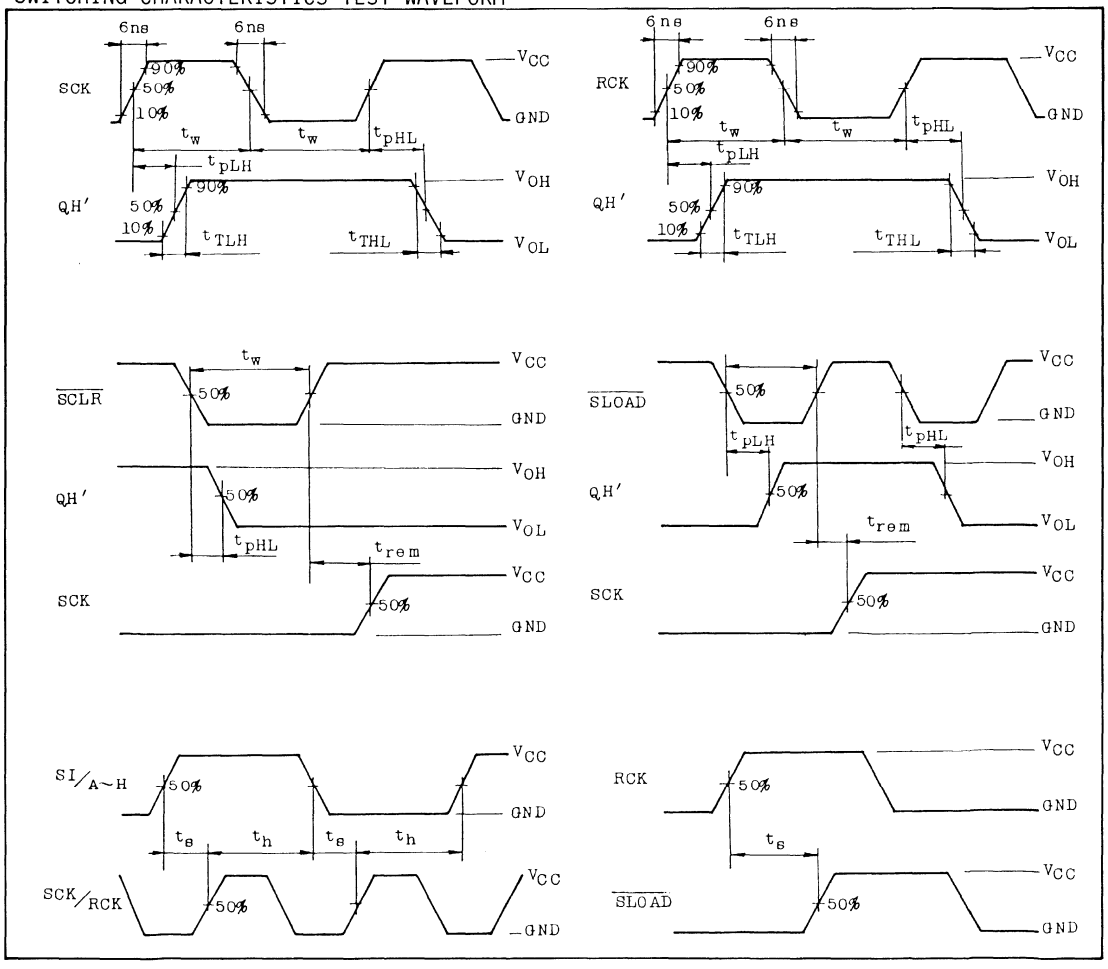
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	76	-	-	-	

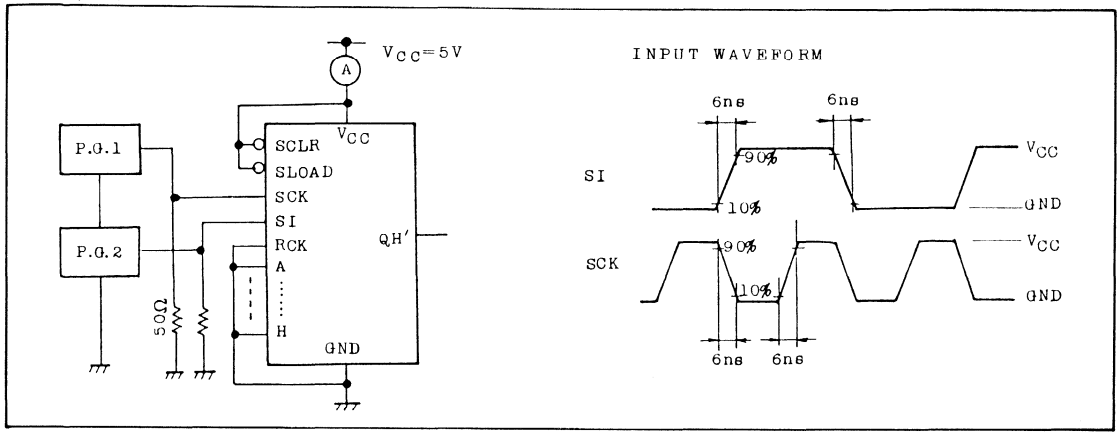
Note 1 C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT

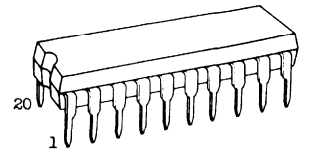


TC74HC620P
TC74HC623P

C²MOS DIGITAL INTEGRATED CIRCUIT

OCTAL BUS TRANCEIVER
TC74HC620P 3-STATE, INVERTING
TC74HC623P 3-STATE, NON-INVERTING

The TC74HC620 and TC74HC623 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by GAB, $\overline{GBA}$, GAB and $\overline{GBA}$ inputs are equipped with protection circuits against static discharge or transient excess voltage.



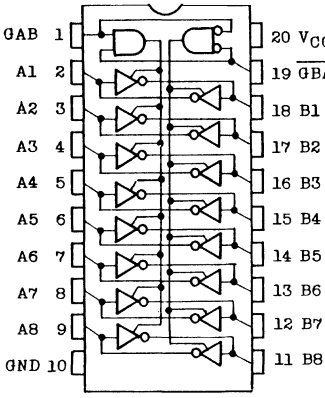
DIP20(3D20A-P)

FEATURES:

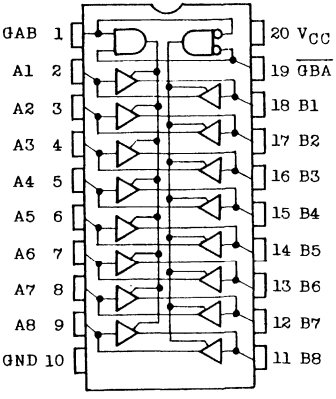
- High Speed ..... t_{pd}=10ns[620], t_{dp}=8ns[623] (Typ.) at V_{CC}=5V
- Low Power Disspation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .. $|I_{OH}|=I_{OL}$=6mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS620/623

PIN ASSIGNMENT (TOP VIEW)

TC74HC620



TC74HC623



NOTICE FOR APPLICATION

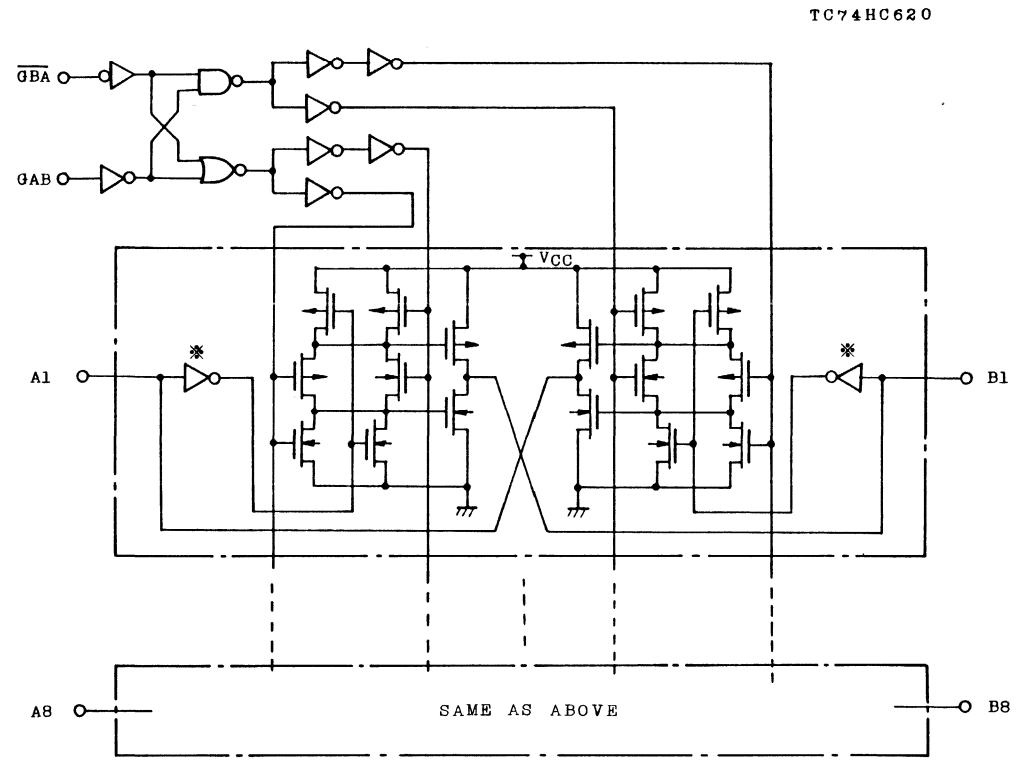
It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TC74HC620P
TC74HC623P

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A Bus	B Bus	HC620	HC623
L	L	Output	Input	$A = \overline{B}$	A = B
H	H	Input	Output	$B = \overline{A}$	B = A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

LOGIC DIAGRAM



Note: In case of TC74HC623, input inverters marked ✱ at A bus and B bus are eliminated respectively.

TC74HC620P
TC74HC623P

ABSOLUTE MAXIMUM RATINGS

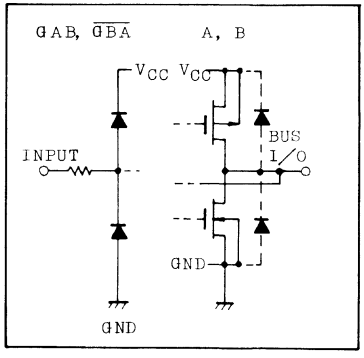
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
Bus Terminal Voltage	$V_{I/O}$	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Bus Terminal Voltage	$V_{I/O}$	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

TC74HC620P
TC74HC623P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Bus Terminal 3-State Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Lekage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to GAB, $\overline{GBA}$ input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time *	t_{pLH}		2.0	-	48	100	-	125	
	t_{pHL}		4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Dealy Time **	t_{pLH}		2.0	-	40	85	-	105	
	t_{pHL}		4.5	-	10	17	-	21	
			6.0	-	9	14	-	18	
3-State Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	74	150	-	190	
	t_{pZH}		4.5	-	19	30	-	38	
			6.0	-	10	26	-	33	
3-State Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	100	180	-	225	
	t_{pHZ}		4.5	-	25	36	-	45	
			6.0	-	21	31	-	38	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC620		-	40	-	-	-	
		TC74HC623		-	35	-	-	-	

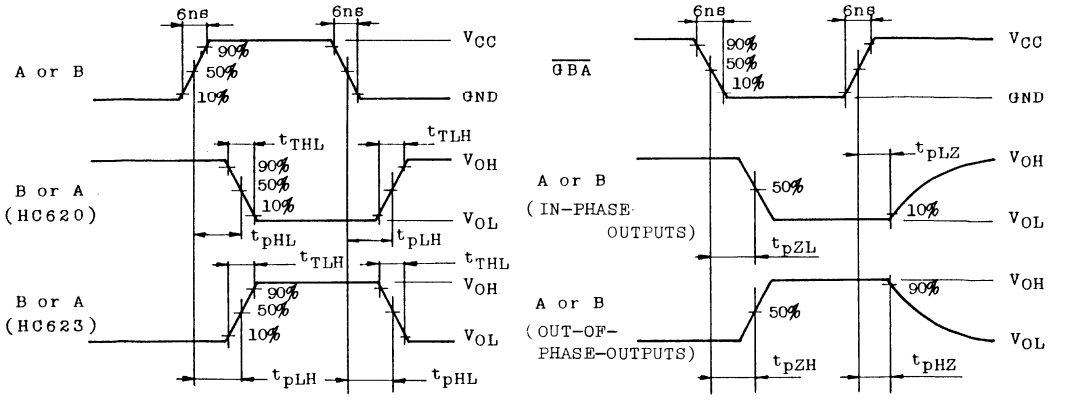
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN}$$

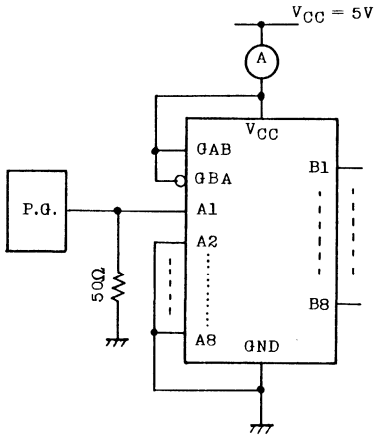
(2) * TC74HC620 ** TC74HC623

TC74HC620P
TC74HC623P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

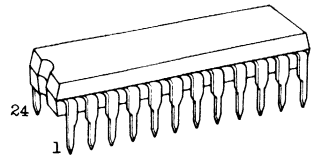
At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC646P
TC74HC648P

C²MOS DIGITAL INTEGRATED CIRCUIT

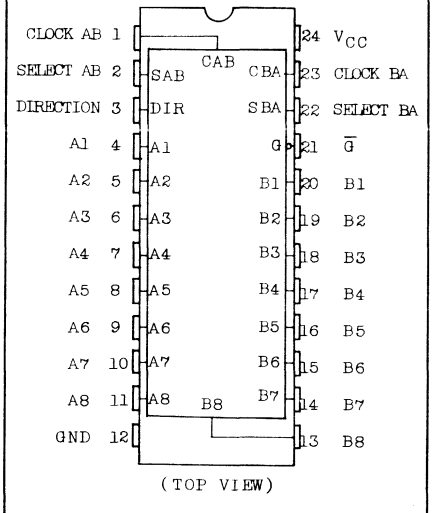
TC74HC646P OCTAL BUS TRANSCEIVER/REGISTER
TC74HC648P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)

The TC74HC646/648 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are bus tranceiver with 3-state outputs, D type flip-flops, and control circuitry arranged for multiplexed transmission of data directrly from the input bus or from the internal registers. If DIR input is held "H", A1 thru 8 become inputs and B1 thru 8 become outputs. If DIR input is held "L", A1 thru 8 become outputs.
Enable input $\overline{G}$ is held "H", both of A bus and B bus become high impedance.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of internal flip-flops. These flip-flops change state state on positive going transition of the clock pulse (CAB, CBA).
The TC74HC646 is non-inverting output type while the TC74HC648 is inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS646/648

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

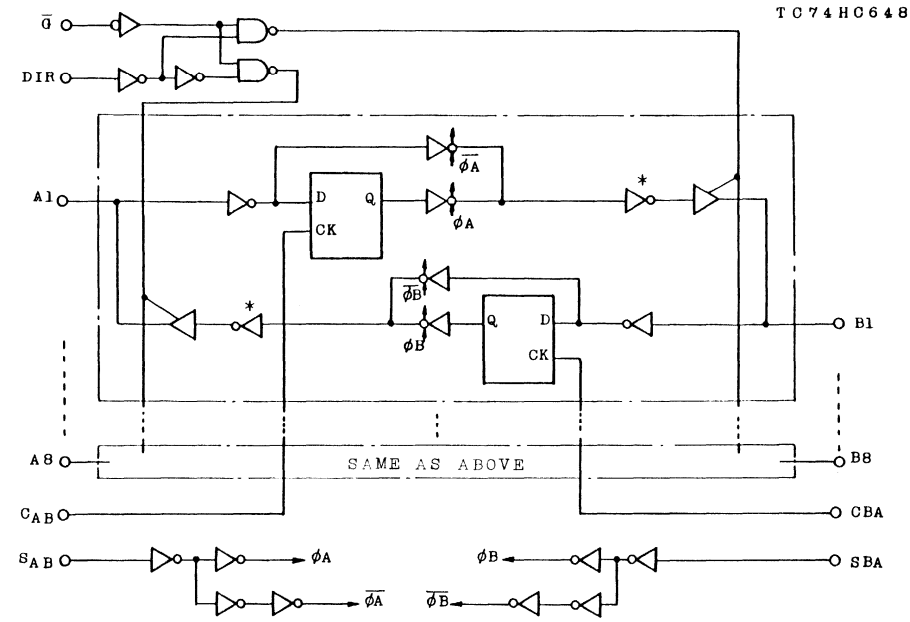
TC74HC646 (The truth table for TC74HC648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the A bus displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
L	L					OUTPUTS	INPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the B bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

Note: X; Don't Care
Qn; The data stored to the internal flip-flops by most recent low to high transition of the clock inputs.
Z; High Impedance
* The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

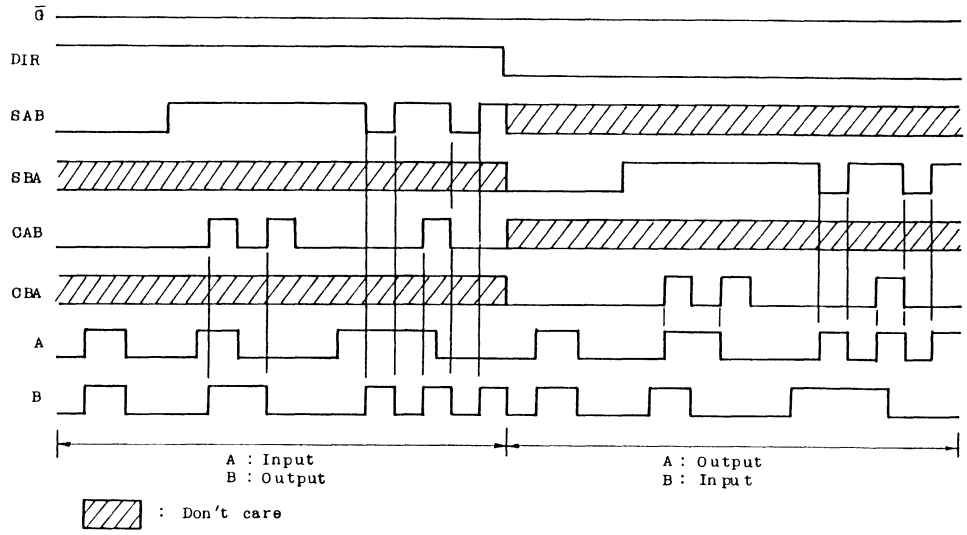
TC74HC646P
TC74HC648P

LOGIC DIAGRAM



Note: In case of TC74HC646 output inverter maked * at A bus and B bus are eliminated.

TIMING CHART



TC74HC646P
TC74HC648P

ABSOLUTE MAXIMUM RATINGS

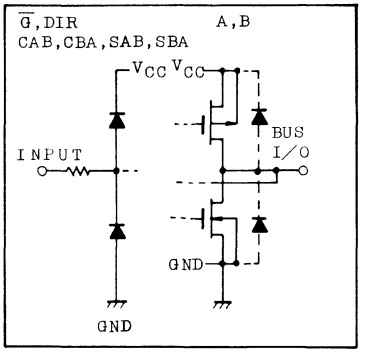
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
Bus Terminal Voltage	$V_{I/O}$	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Bus Terminal Voltage	$V_{I/O}$	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (BUS - BUS)	t_{pLH}		2.0	-	92	180	-	225	
	t_{pHL}		4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - BUS)	t_{pLH}		2.0	-	124	240	-	300	
	t_{pHL}		4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (SELECT - BUS)	t_{pLH}		2.0	-	112	220	-	275	
	t_{pHL}		4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Data Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	

TC74HC646P
TC74HC648P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
3-State Output Enable Time ($\overline{G}$, DIR)	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	104	205	-	250	ns
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
3-State Output Disable Time ($\overline{G}$, DIR)	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	104	210	-	250	
			4.5	-	29	42	-	50	
			6.0	-	25	36	-	43	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

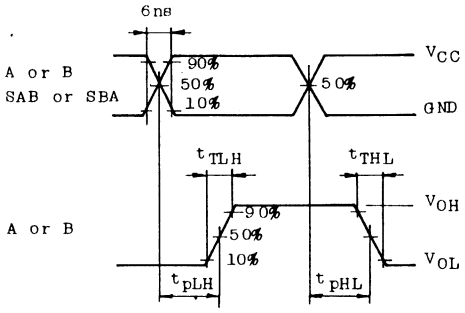
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

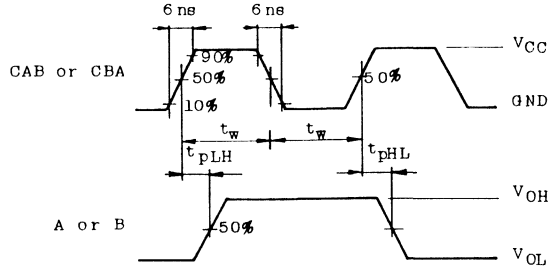
TC74HC646P
TC74HC648P

SWITCHING CHARACTERISTICS TEST WAVEFORM

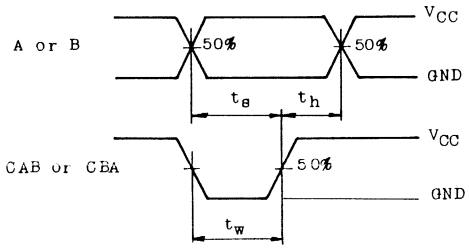
WAVEFORM 1



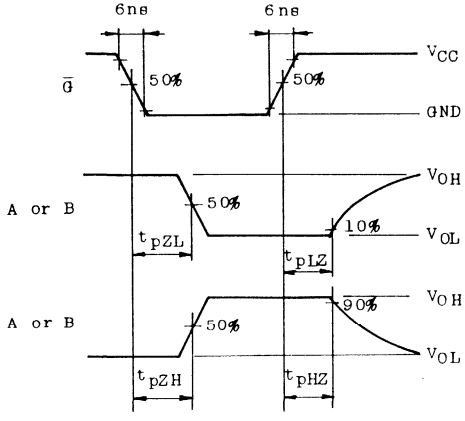
WAVEFORM 2



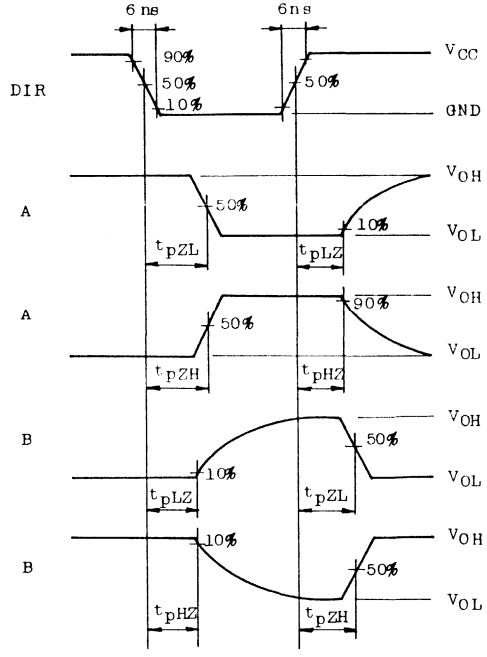
WAVEFORM 3



WAVEFORM 4

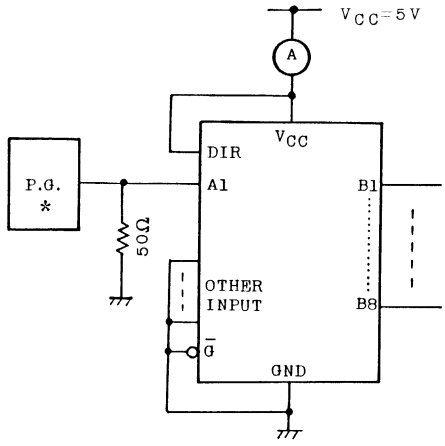


WAVEFORM 5



TC74HC646P
TC74HC648P

I_{CC}(Opr.) TEST CIRCUIT



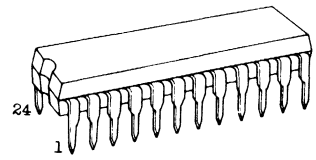
* Input transition time is the same as that in case of switching characteristics test.

TC74HCT646P
TC74HCT648P

C²MOS DIGITAL INTEGRATED CIRCUIT

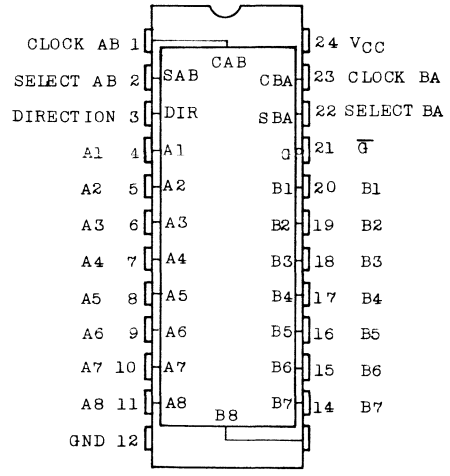
TC74HCT646P OCTAL BUS TRANSCEIVER/REGISTER
TC74HCT648P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)

The TC74HCT646/648 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These devices are bus tranceiver with 3-stete outputs, D type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If DIR input is held "H", A1 thru 8 become inputs and B1 thru 8 become outputs. If DIR input is held "L", A1 thru 8 become outputs.
Enable input $\overline{G}$ is held "H", both of A bus and B bus become high impedance.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of internal flip-flops. These flip-flops change state on positive going transition of the clock pulse (CAB, CBA).
The TC74HCT646 is non-inverting output type while the TC74HCT648 is inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.. I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL output ..... V_{IH}=2V(Min.) V_{IL}=0.8V(Max.)
- Output Drive Capability .....15 LSTTL Loads
- Symmetrical Output Impedance .$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

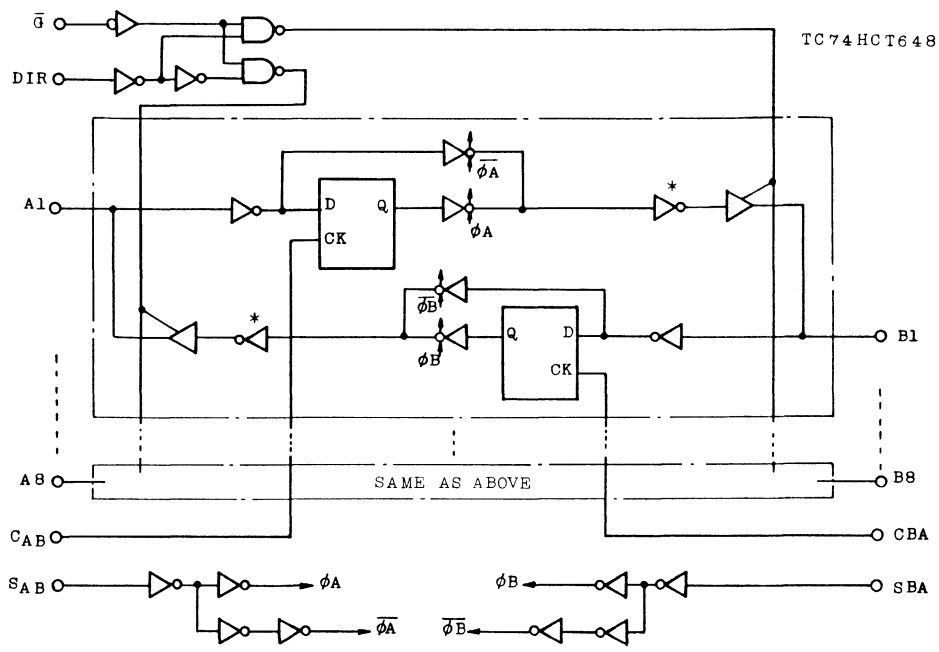
TC74HCT646 (The truth table for TC74HCT648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the A bus displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
L	L					OUTPUTS	OUTPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flop-flops are displayed at the B bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

Note: X; Don't care
Qn; The data stored to the internal flip-flops by most recent low to high transition of the clock inputs.
Z; High Impedance
* The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

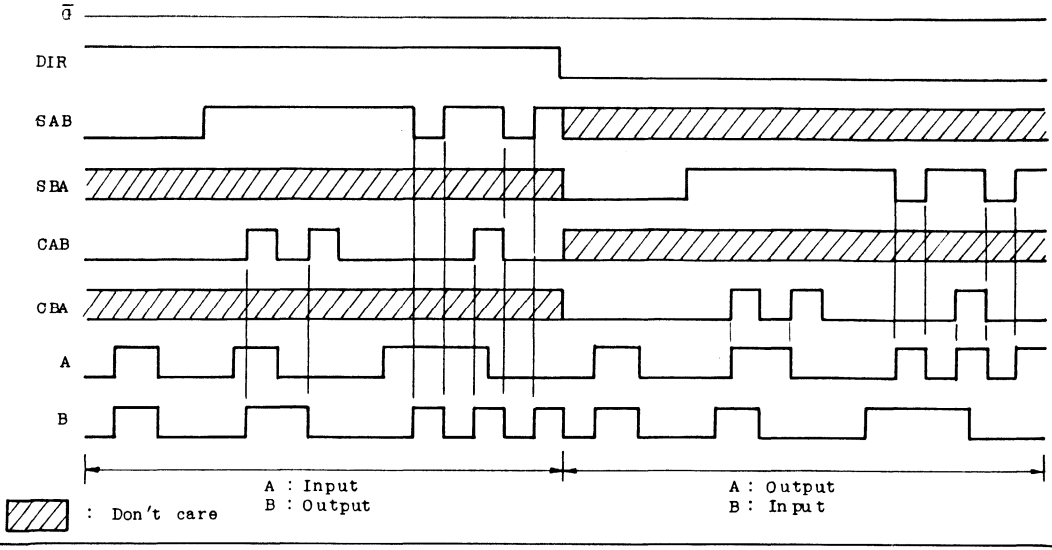
TC74HCT646P
TC74HCT648P

LOGIC DIAGRAM



Note: In case of TC74HCT646, output inverter marked * at A bus and B bus are eliminated.

TIMING CHART (TC74HCT646P)



TC74HCT646P
TC74HCT648P

ABSOLUTE MAXIMUM RATINGS

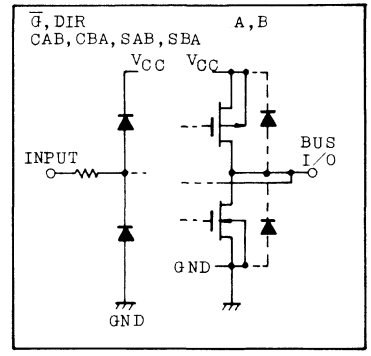
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C and from Ta=65°C up to 85°C derating factor of 10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	V_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	4.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (BUS - BUS)	t_{pLH} t_{pHL}		4.5	-	20	31	-	39	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		4.5	-	30	46	-	58	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		4.5	-	31	48	-	60	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		4.5	-	11	20	-	25	
Minimum Data Set-up Time	t_s		4.5	-	4	10	-	13	
Minimum Data Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time ($\overline{G}$ - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	26	38	-	48	
3-State Output Disable Time ($\overline{G}$ - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	38	-	48	

TC74HCT646P
TC74HCT648P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time (DIR - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	28	40	-	50	ns
3-State Output Disable Time (DIR - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	28	40	-	50	ns
Input Capacitance	C_{IN}	*		-	5	10	-	10	pF
Output Capacitance	C_{OUT}	An, Bn		-	13	-	-	-	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC646		-	55	-	-	-	pF
		TC74HC648		-	52	-	-	-	pF

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

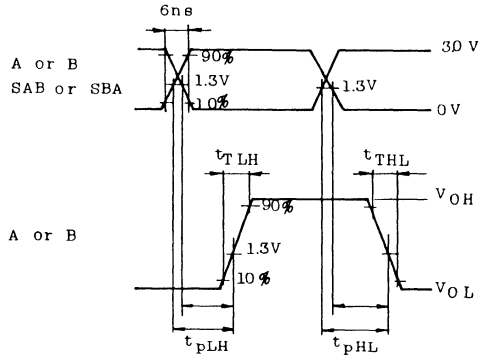
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

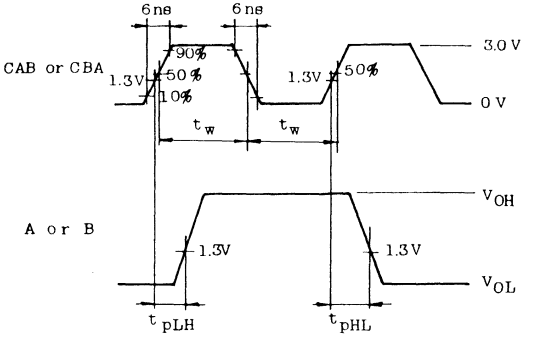
TC74HCT646P
TC74HCT648P

SWITCHING CHARACTERISTICS TEST WAVEFORM

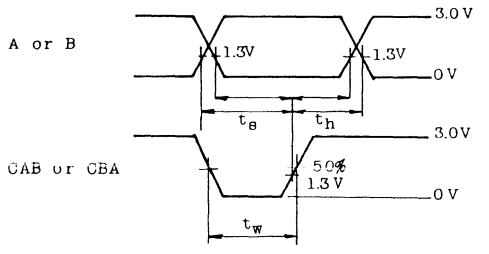
WAVEFORM 1



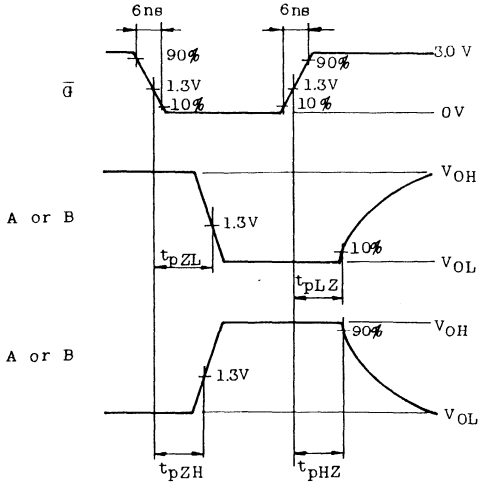
WAVEFORM 2



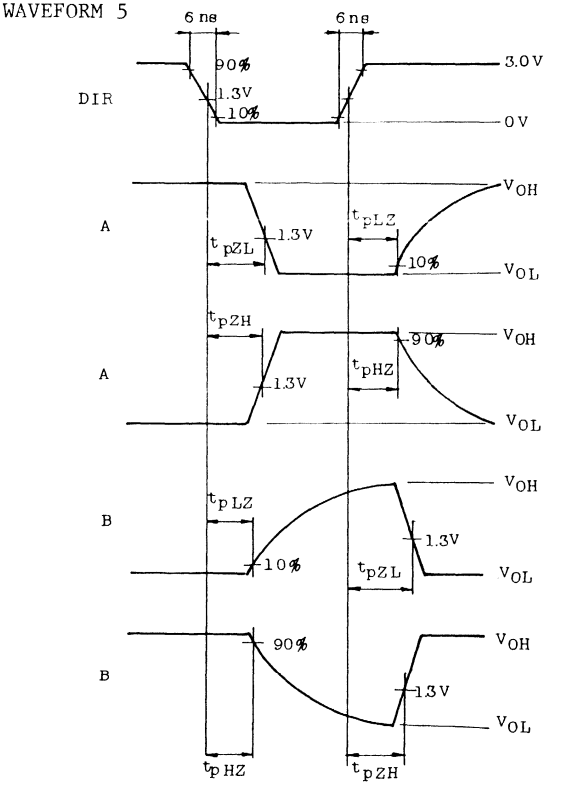
WAVEFORM 3



WAVEFORM 4

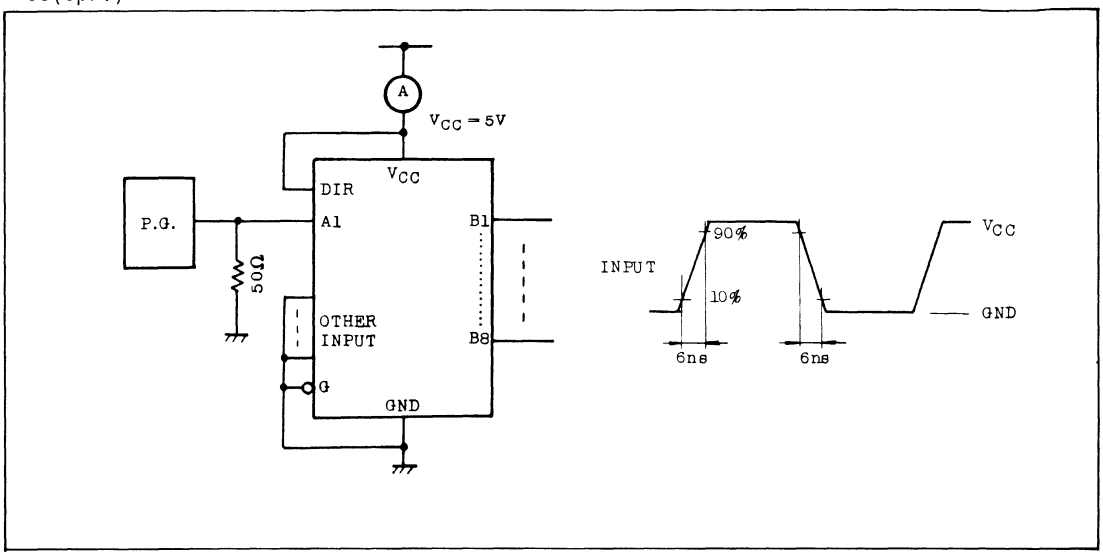


WAVEFORM 5



TC74HCT646P
TC74HCT648P

I_{CC}(Opr.) TEST CIRCUIT

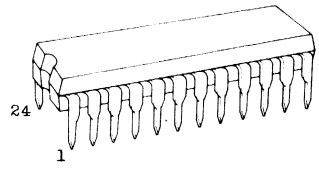


TC74HC651P
TC74HC652P

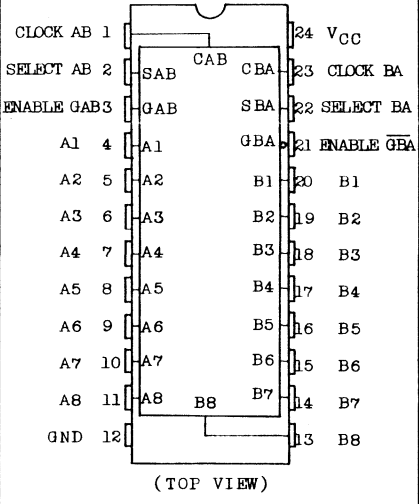
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC651P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)
TC74HC652P OCTAL BUS TRANSCEIVER/REGISTER

The TC74HC651 and TC74HC652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are bus tranceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If enable inputs GAB and $\overline{GBA}$ are held "H", A bus are inputs and B bus are outputs, and if GAB and $\overline{GBA}$ are held "L", B bus are inputs and A bus are outputs.
Enable input GAB is held "L" and either $\overline{GBA}$ is held "H", respectively, A bus and B bus are isolated.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of the internal flip-flops. These flip-flops change state on positive going transition of the clock pulses (CAB, CBA). The TC74HC651 is inverting output type while the TC74HC652 is non-inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance.. $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ....V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS651/652

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

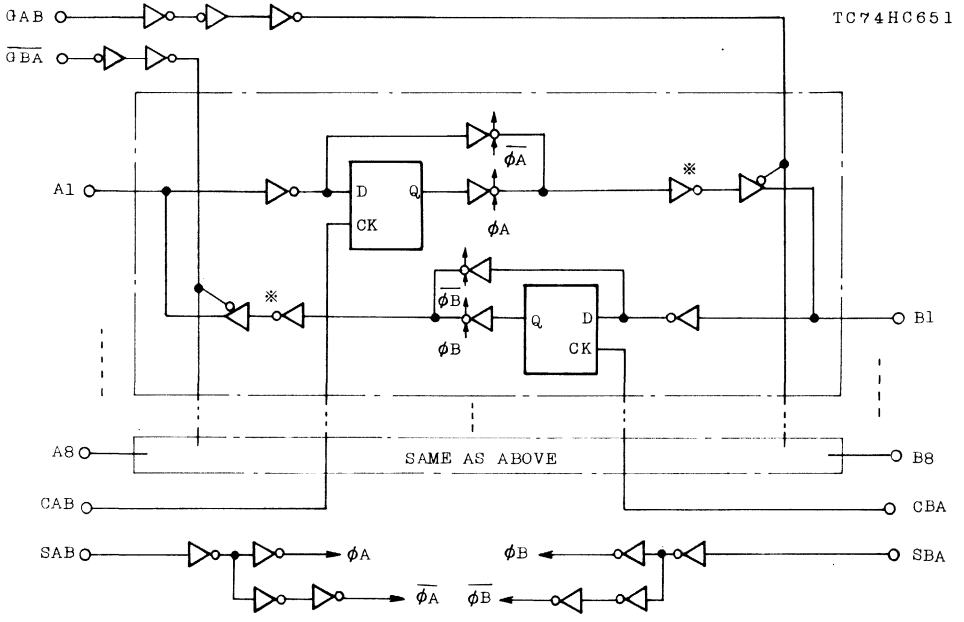
TC74HC652 (The truth table for TC74HC651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to internal Flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus.
		X*	↓	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↓	↓	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively.

X: Don't Care Qn: The data stored to the internal flip-flops by most recent low to high transition of the clock inputs. Z: High Impedance *: The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

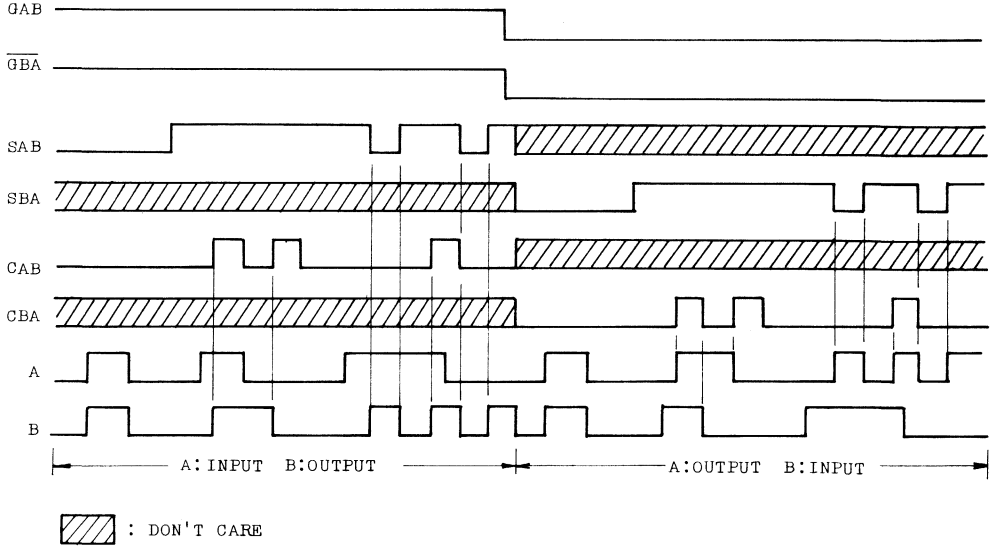
TC74HC651P
TC74HC652P

LOGIC DIAGRAM



NOTE. IN CASE OF TC74HC652 OUTPUT INVERTER MARKED ※ AT A BUS AND B BUS ARE ELIMINATED

TIMING CHART



TC74HC651P
TC74HC652P

ABSOLUTE MAXIMUM RATINGS

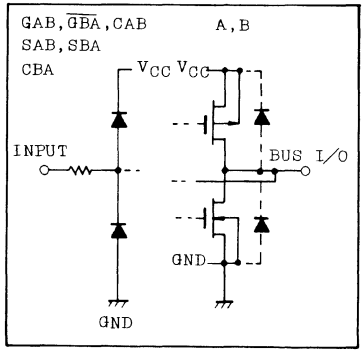
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC651P
TC74HC652P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current*	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Suppy Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable onlt to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (BUS - BUS)	t_{pHL} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Data Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	

TC74HC651P
TC74HC652P

AC CHARACTERISTICS (Continued)

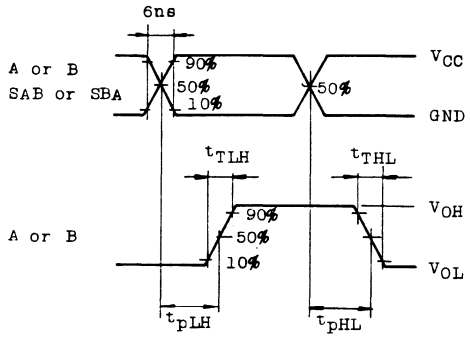
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	100	180	-	225	ns
			4.5	-	25	36	-	45	
			6.0	-	21	31	-	38	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	88	170	-	215	
			4.5	-	22	34	-	43	
			6.0	-	19	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

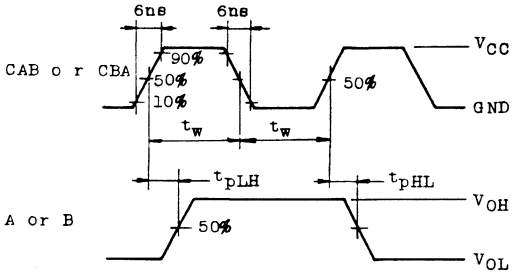
TC74HC651P
TC74HC652P

SWITCHING CHARACTERISTICS TEST WAVEFORM

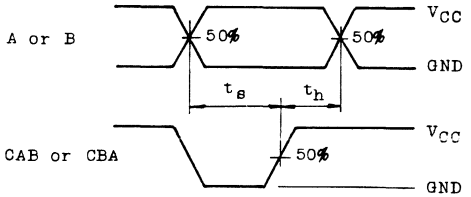
WAVEFORM 1



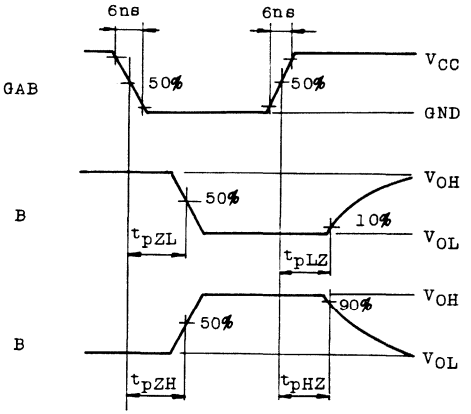
WAVEFORM 2



WAVEFORM 3

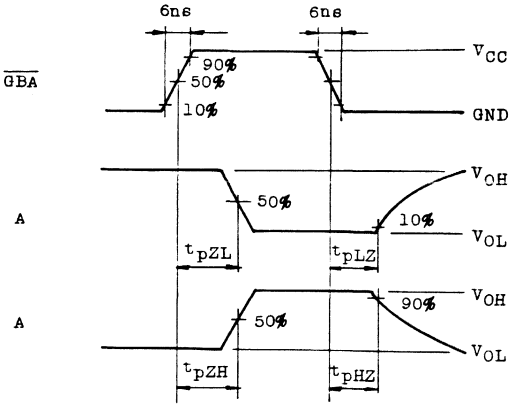


WAVEFORM 4



$\overline{GBA}$= "H"

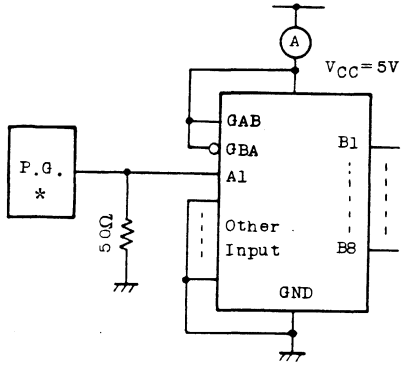
WAVEFORM 5



GAB= "L"

TC74HC651P
TC74HC652P

$I_{CC(Opr.)}$ TEST WAVEFORM



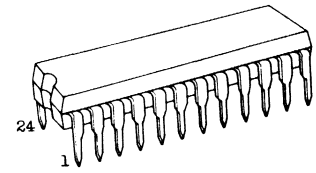
* Input transition time is the same as that in case of switching characteristics test.

TC74HCT651P
TC74HCT652P

C²MOS DIGITAL INTEGRATED CIRCUIT

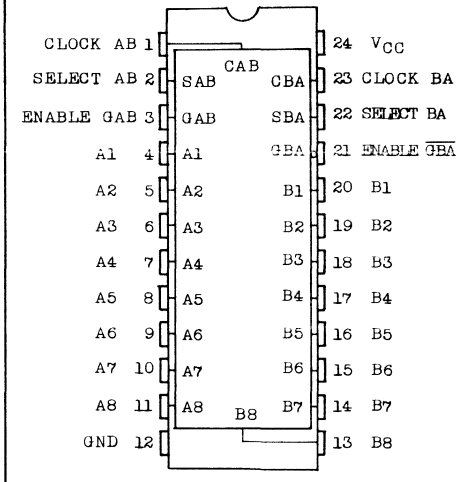
TC74HCT651P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)
TC74HCT652P OCTAL BUS TRANSCEIVER/REGISTER

The TC74HCT651 and TC74HCT652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These devices are bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If enable inputs GAB and $\overline{GBA}$ are held "H", A bus are inputs and B bus are outputs, and if GAB and $\overline{GBA}$ are held "L", B bus are inputs and A bus are outputs.
Enable input GAB is held "L" and either $\overline{GBA}$ is held "H", respectively, A bus and B bus are isolated.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of the internal flip-flops. These flip-flops change state on positive going transition of the clock pulses (CAB, CBA). The TC74HCT651 is inverting output type while the TC74HCT652 is non-inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL Output ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability .....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS651/652

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

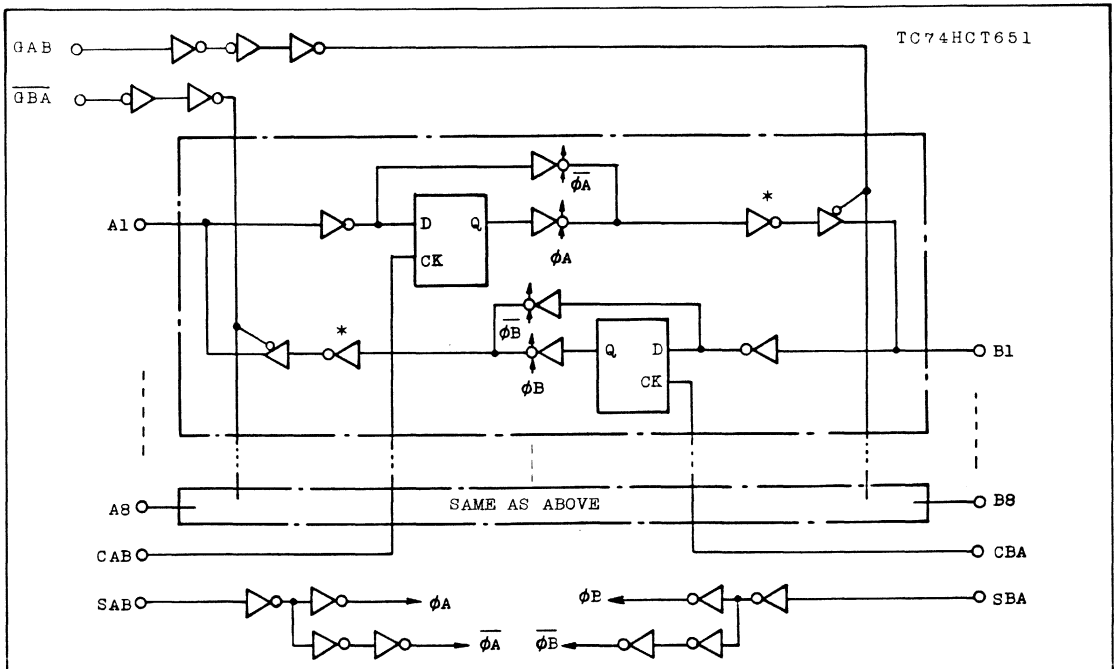
TC74HCT652 (The truth table for TC74HCT651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to internal Flip-flops. The data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↑	↑	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively.

X: Don't care Qn: The data stored to the internal flip-flops by most recent low to high transition of the clock inputs. Z: High Impedance *: The data at the A and B bus will be stored to the internal flip-flops on every low to high trnsition of the clock inputs.

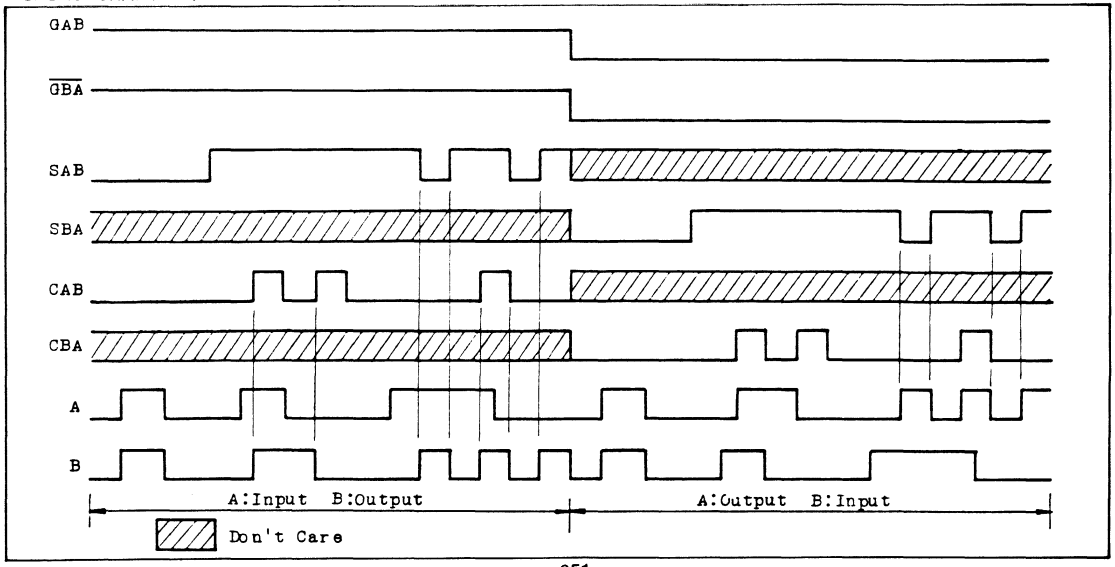
TC74HCT651P
TC74HCT652P

LOGIC DIAGRAM



Note: In case of TC74HCT652, Output inverter marked * at A bus and B bus are eliminated.

TIMING CHART (TC74HCT652P)



TC74HCT651P
TC74HCT652P

ABSOLUTE MAXIMUM RATINGS

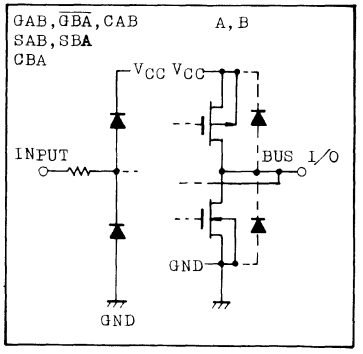
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied unitl 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT tr=tf=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (BUS - BUS)	t_{pLH} t_{pHL}		4.5	-	20	31	-	39	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		4.5	-	30	47	-	59	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		4.5	-	31	48	-	60	
Minimum Clock Pulse Widht	$t_{w(H)}$ $t_{w(L)}$		4.5	-	11	20	-	25	
Minimum Data Set-up Time	t_s		4.5	-	4	10	-	13	
Minimum Data Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time ($\overline{GBA}$ - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	21	30	-	38	
3-State Output Disable Time ($\overline{GBA}$ - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	38	-	48	

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TC74HCT652P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time(GAB -BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	25	36	-	45	ns
3-State Output Disable Time(GAB - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	25	36	-	45	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HCT651		-	52	-	-	-	
		TC74HCT652		-	52	-	-	-	

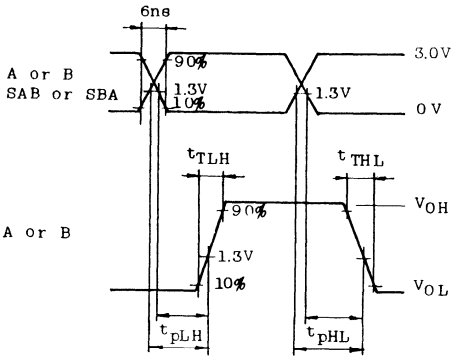
* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

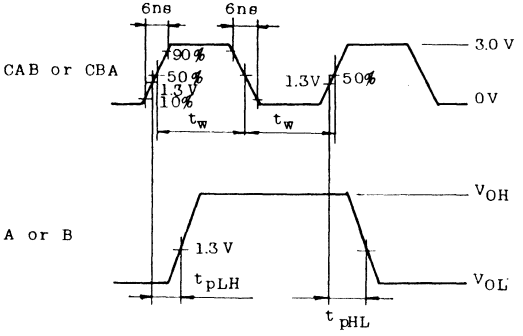
$$I_{PD(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

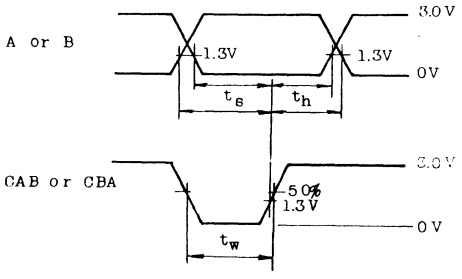
WAVEFORM 1



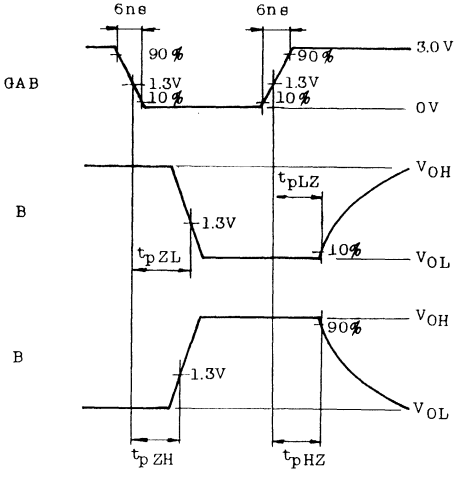
WAVEFORM 2



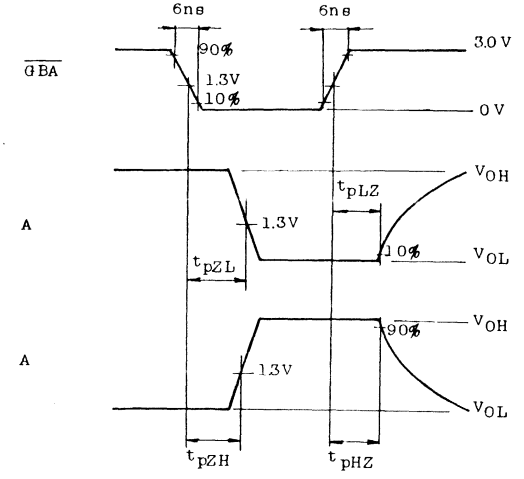
WAVEFORM 3



WAVEFORM 4 $\overline{GBA}$="H"

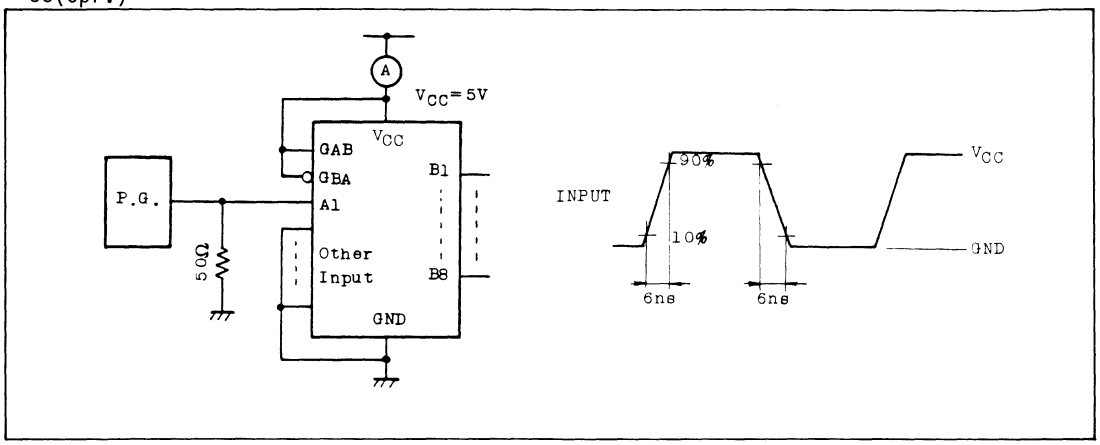


WAVEFORM 5 GAB="L"



TC74HCT651P
TC74HCT652P

$I_{CC(Opr.)}$ TEST WAVEFORM



TC74HC670P

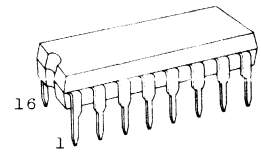
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC670P 4-WORD x 4-BIT REGISTER FILE (3-STATE)

The TC74HC670 is a high speed CMOS 4-WORD × 4-BIT REGISTER FILE fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.
Four data inputs are avairable which are used to supply the 4-bit word to be stored. Location of the word is determined by the A and B inputs. When the WRITE-ENABLE input is "H", the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the READ-ENABLE input "H", the data outputs are inhibited and go into the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS670



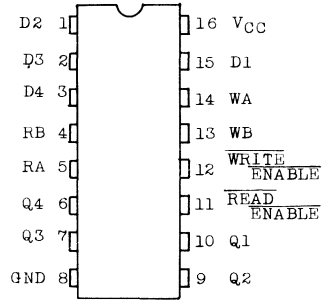
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC670P

TRUTH TABLE

WRITE FUNCTION TABLE

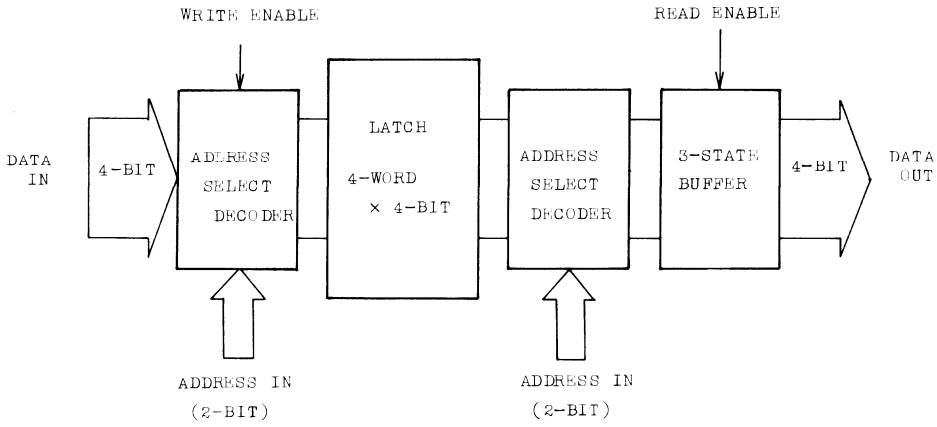
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

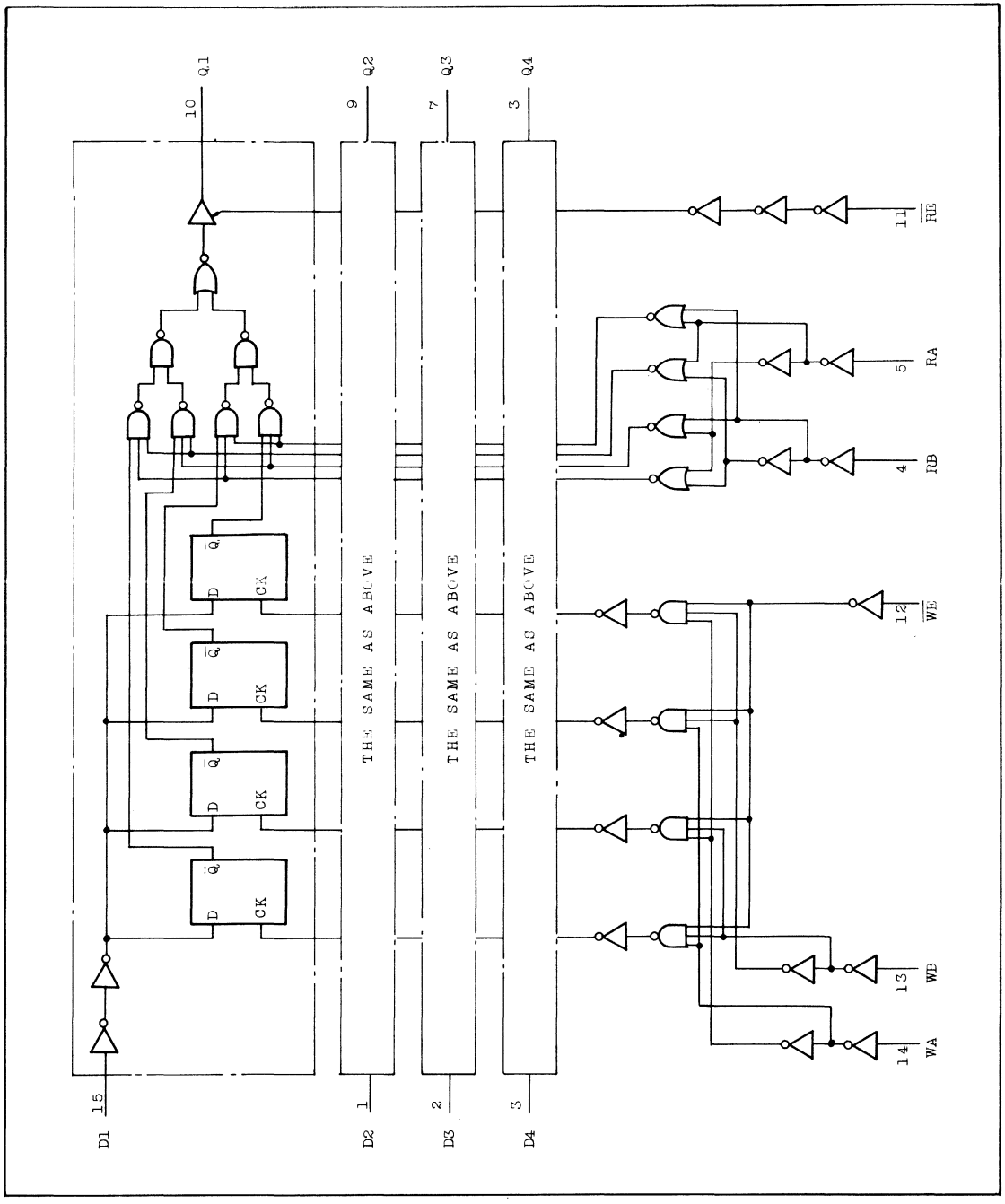
NOTES
1. X : DON'T CARE Z : HIGH IMPEDANCE
2. (Q=D) = THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3. Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4. W0B1 = THE FIRST BIT OF WORD 0, etc.

BLOCK DIAGRAM



TC74HC670P

LOGIC DIAGRAM

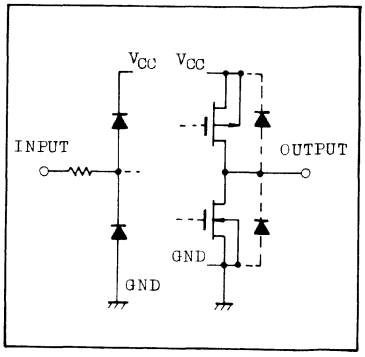


TC74HC670P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (RA, RB - Qn)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{WE}$ - Qn)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Propagation Delay Time (Dn - Qn)	t_{pLH} t_{pHL}		2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Minimum Pulse Width ($\overline{WE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Dn - $\overline{WE}$)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set-up Time (WA, WB - $\overline{WE}$)	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time (Dn - $\overline{WE}$)	t_h		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (WA, WB - $\overline{WE}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Latch Time ($\overline{WE}$ - RA, RB)	(1) t_{latch}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	68	120	-	150	
			4.5	-	17	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(2)			-	44	-	-	-	

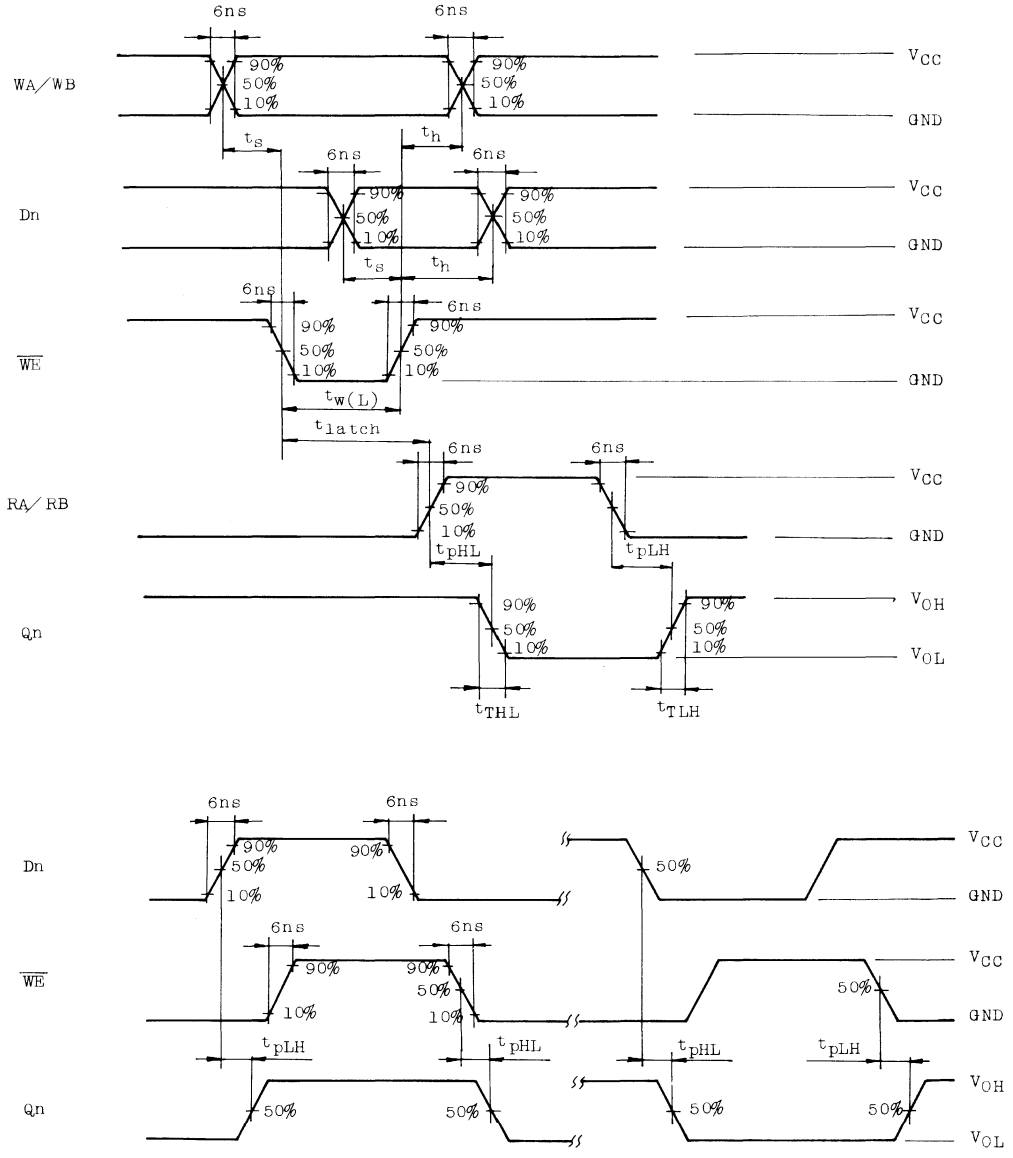
Note(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

(2): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

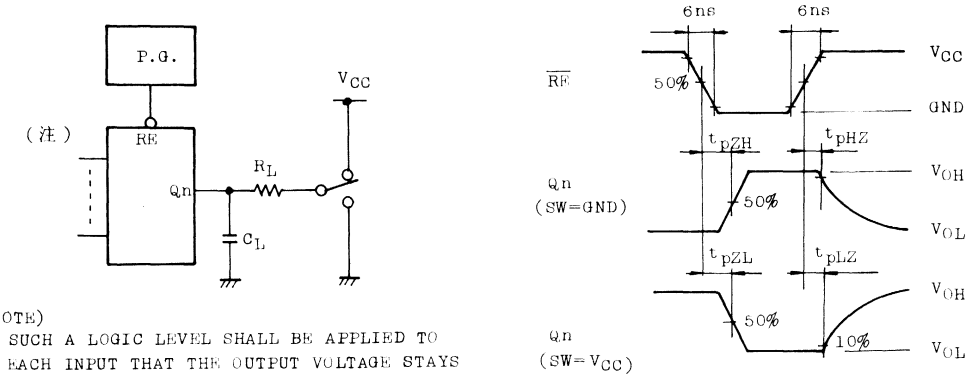
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC670P

SWITCHING CHARACTERISTICS TEST WAVEFORM

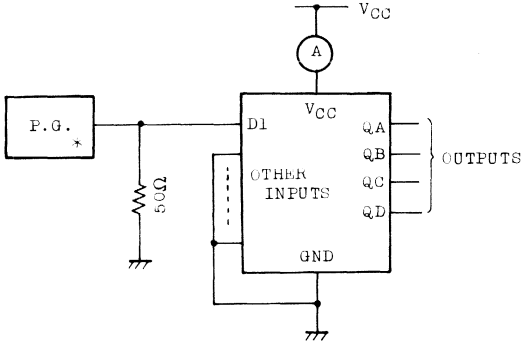


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



(NOTE)
SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

I_{CC}(Opr.) TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC688P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC688P/F 8-BIT EQUALITY COMPARATOR

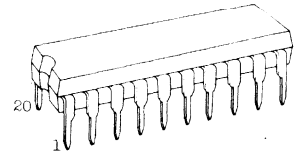
The TC74HC688 utilizes silicon gate C²MOS technology to achieve operating speeds equivalent to LSTTL parts. Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the driving capability of 10 LSTTL loads.

The TC74HC688 compares bit for bit two 8-bit words applied input $P_0 \sim P_7$ and input $Q_0 \sim Q_7$ and indicate whether or not they are equal.

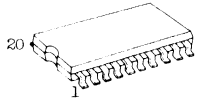
A single active low enable is provided to facilitate cascading of several packages to enable comparison of words greater than 8 bits. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=25ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS688.



DIP20(3D20A-P)



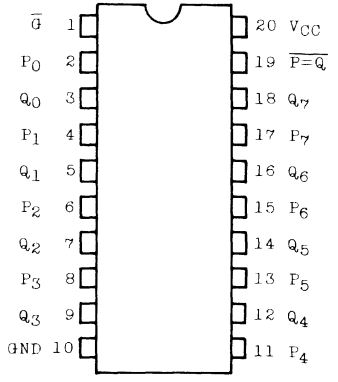
MFP20(F20GA-P)

TRUTH TABLE

INPUT		OUTPUT
P,Q	$\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	L	H
*	H	H

* Don't care

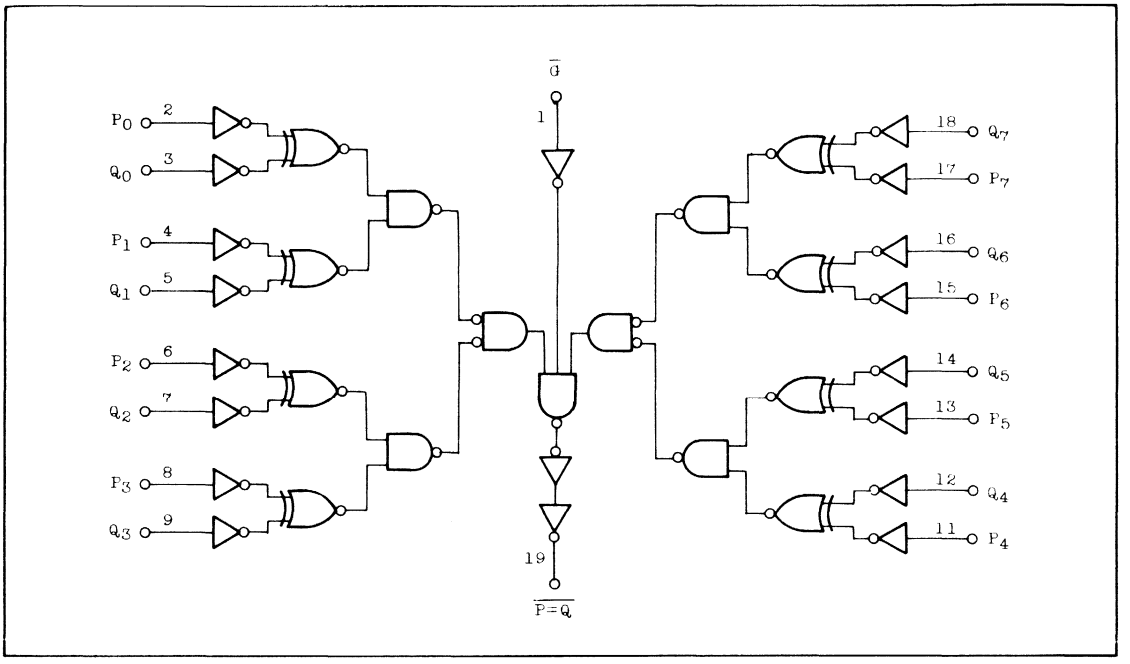
PIN ASSIGNMENT



(TOP VIEW)

TC74HC688P/F

LOGIC DIAGRAM

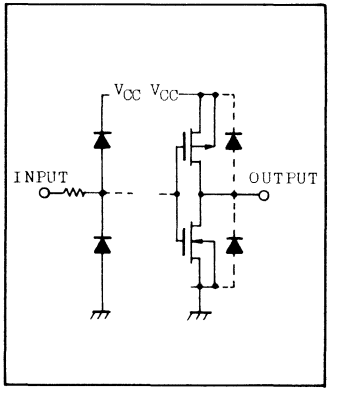


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	Tstg	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC688P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

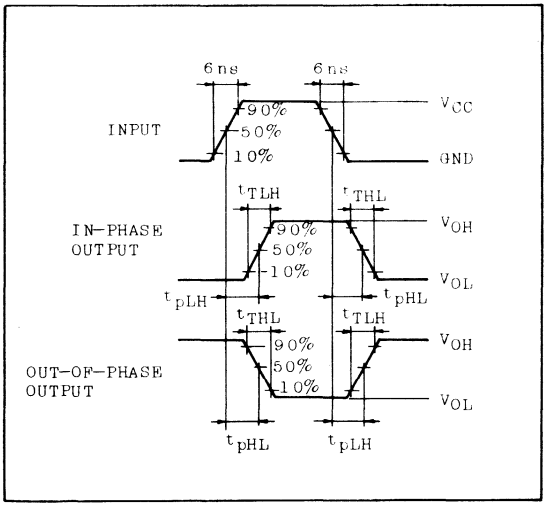
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

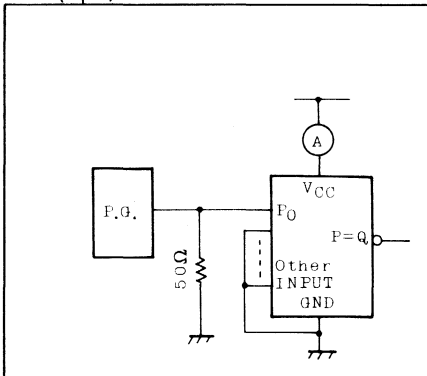
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (P_n,Q_n - $\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	-	104	195	-	245	
			4.5	-	26	39	-	49	
			6.0	-	22	33	-	42	
Propagation Delay Time ($\overline{G}$ - $\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	40	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC690P
TC74HC691P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC690P DECADE COUNTER REGISTER
TC74HC691P 4-BIT BINARY COUNTER REGISTER

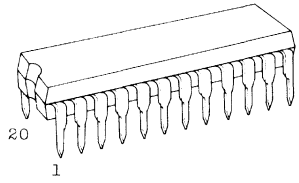
The TC74HC690/691 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

TC74HC690 is BCD DECADE COUNTER, TC74HC691 is 4-BIT BINARY COUNTER, these devices have Registers respectively.
If LOAD input ($\overline{LOAD}$) is held "L", DATA input (A ∿ D) are loaded in internal counter at positive edge of counter clock input ($\overline{CCK}$). And at counter mode, internal counter counts up at positive edge of counter clock. If counter clear input ($\overline{CCLR}$) is held "L", internal counter cleared asynchronously to counter clock.

Internal counter's outputs are stored in output register at positive edge of register clock (RCK). If register clear input ($\overline{RCLR}$) is held "L", the register cleared asynchronously to register clock. At this point, internal counter outputs no change. The outputs (Q_A ∿ Q_D) are selected internal counter outputs or register outputs respectively by output select input (R/$\overline{C}$). Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

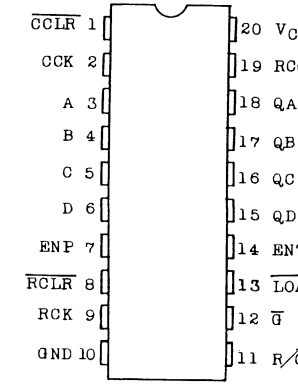


DIP20(3D20A-P)

FEATURES:

- High Speed ..... f_{MAX}=33MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads (For Q_A ∿ Q_D)
  10 LSTTL Loads (For RCO)
- Symmetrical Output Impedance
  $|I_{OH}|=I_{OL}$=6mA(Min.) for Q_A ∿ Q_D Output
  $|I_{OH}|=I_{OL}$=4mA(Min.) for RCO Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL(74LS690/691)

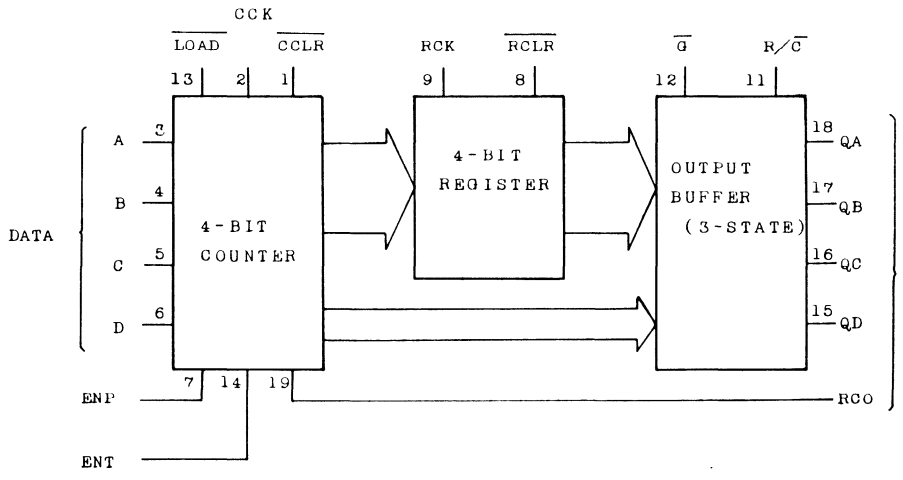
PIN ASSIGNMENT



(TOP VIEW)

TC74HC690P
TC74HC691P

BLOCK DIAGRAM



TRUTH TABLE

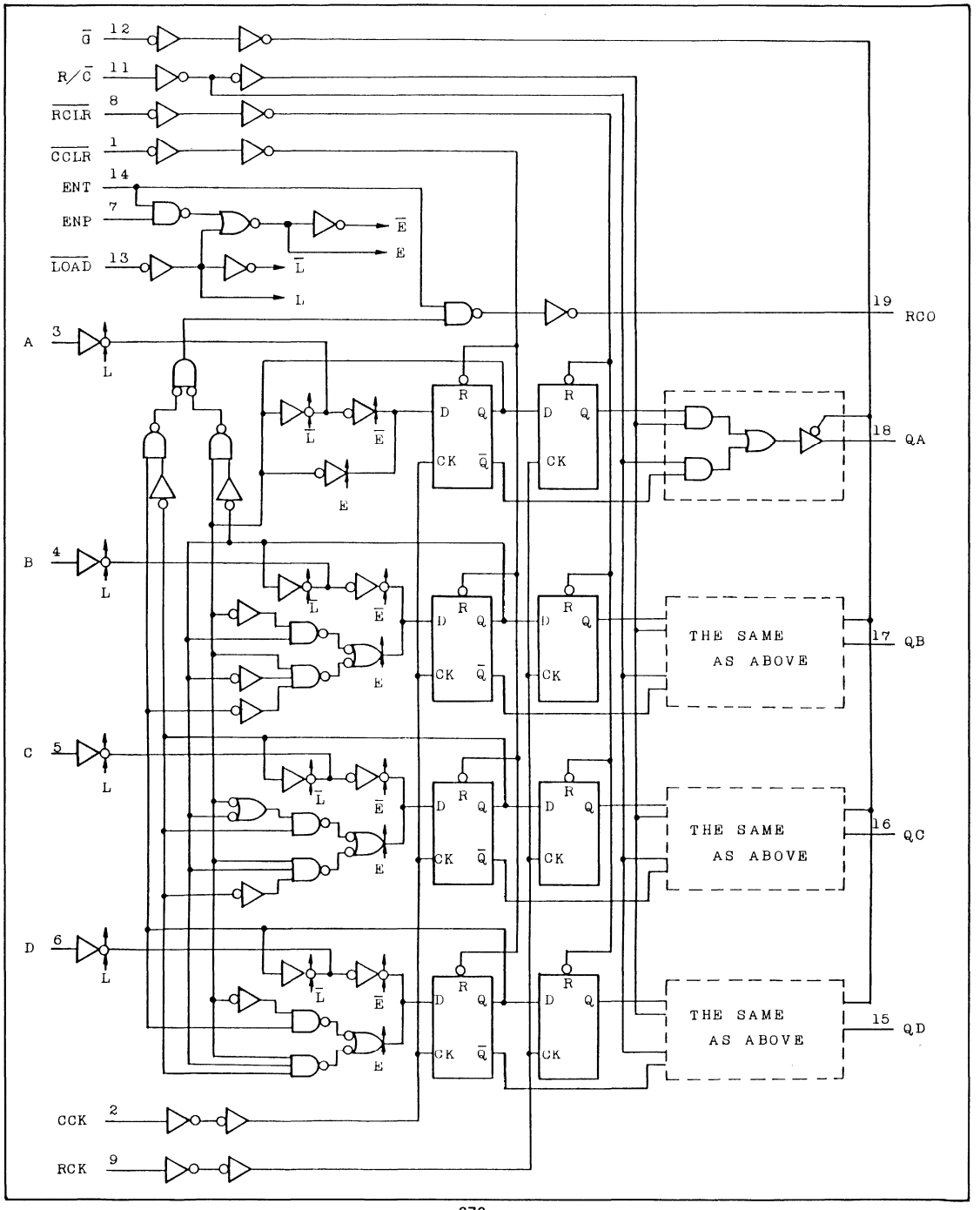
INPUTS									OUTPUTS				FUUCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	↓	X	X	L	L	NO CHANGE				COUNT DISABLE
H	H	X	L	↓	X	X	L	L					NO CHANGE
H	H	H	H	↓	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	X	H	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO CHANGE

X: Don't Care
Z: High Impedance
a∿d: The level of steady state input voltage at inputs A∿D respectively.
a'∿d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.

TC74HC690 RCO=QA • QD • ENT
TC74HC691 RCO=QA • QB • QC • QD • ENT

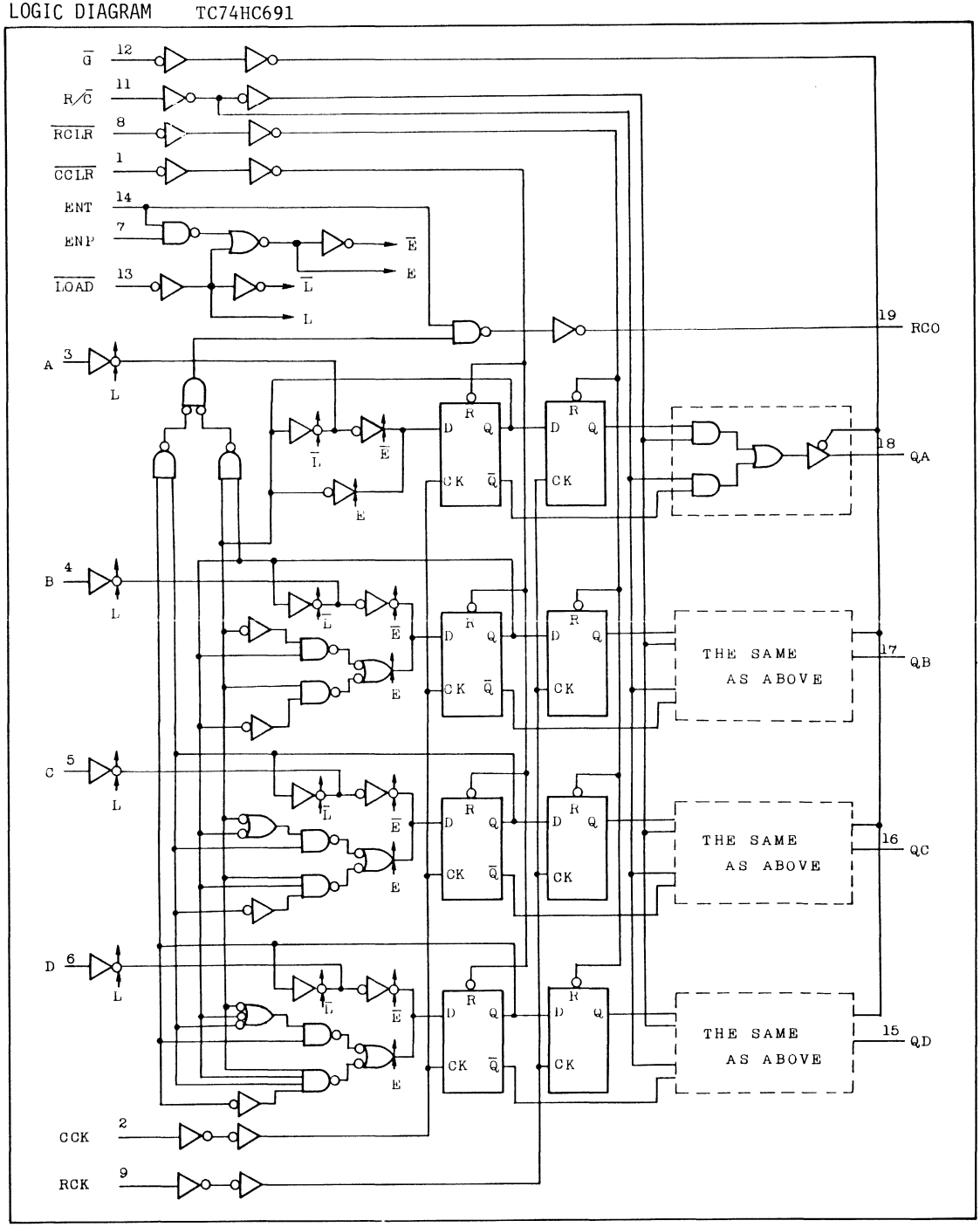
TC74HC690P
TC74HC691P

LOGIC DIAGRAM TC74HC690



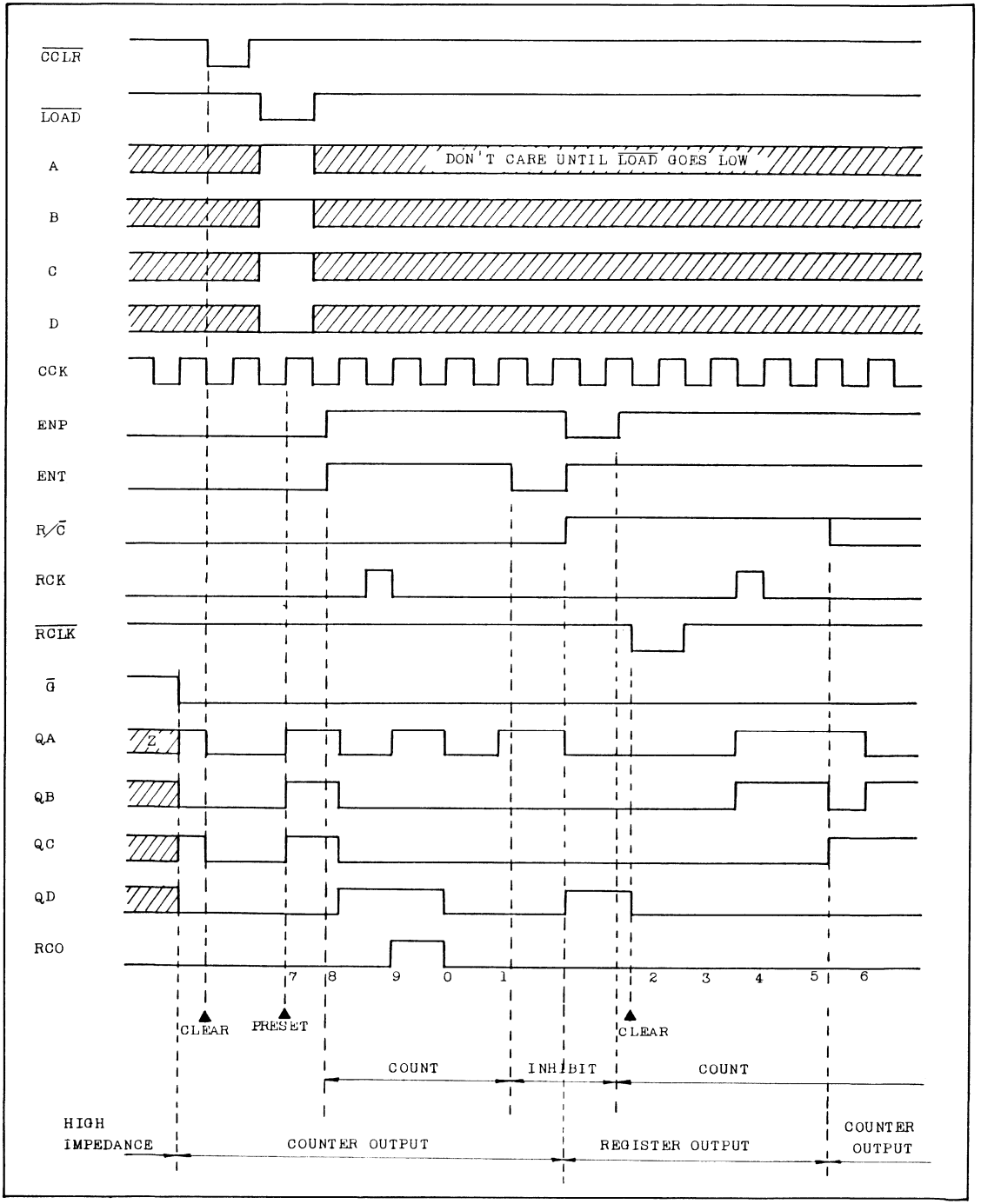
TC74HC690P
TC74HC691P

LOGIC DIAGRAM TC74HC691



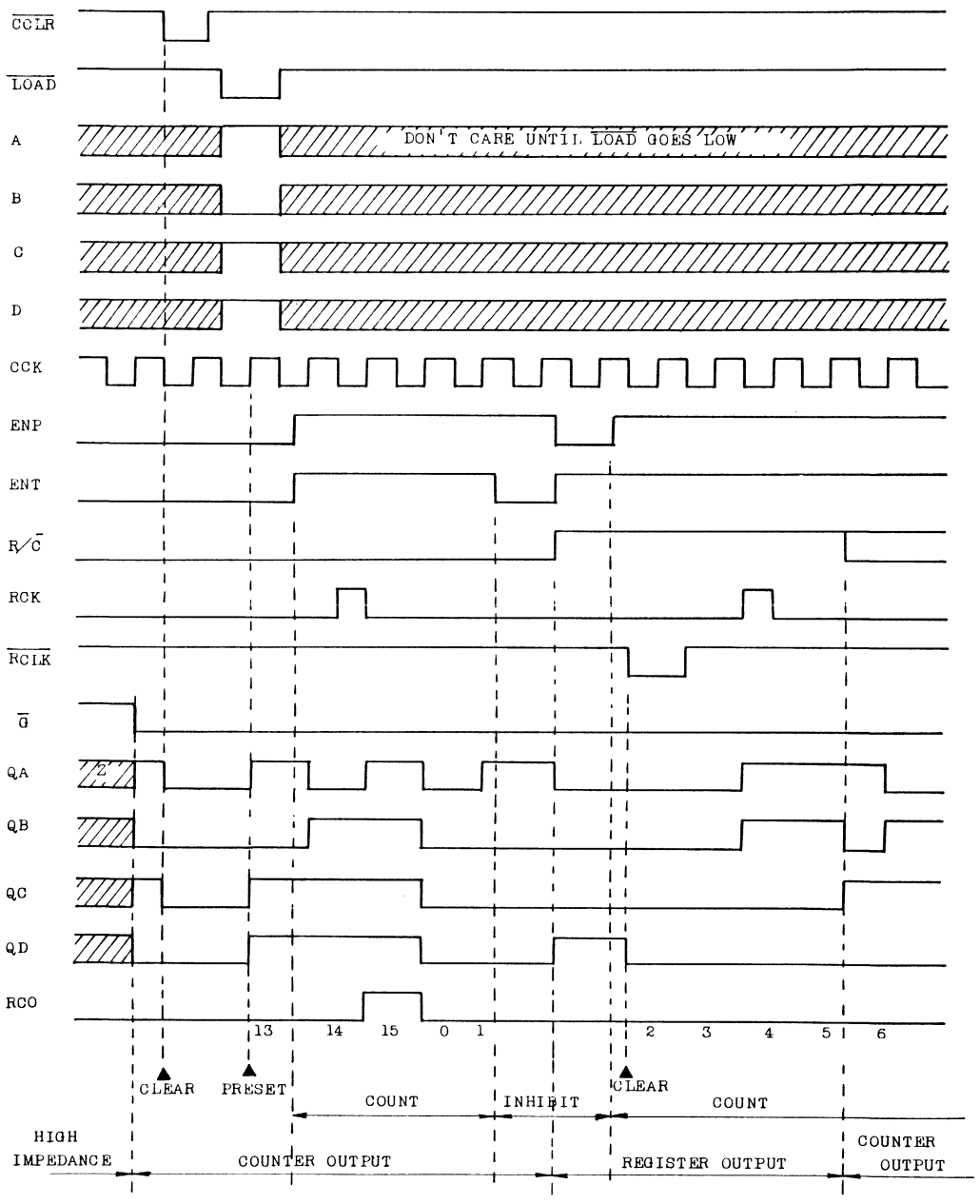
TC74HC690P
TC74HC691P

TIMING CHART TC74HC690



TC74HC690P
TC74HC691P

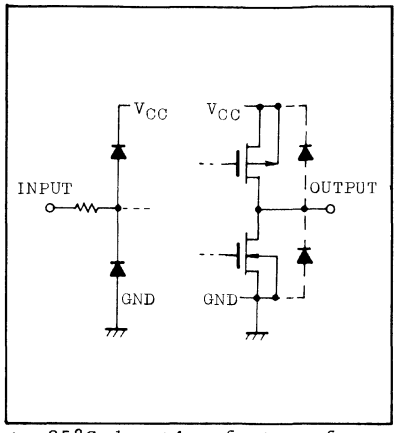
TIMING CHART TC74HC691



TC74HC690P
TC74HC691P

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage Range		V_{CC}	-0.5 ∿ 7	V
DC Input Voltage		V_{IN}	-0.5 ∿ V_{CC}+0.5	
DC Output Voltage		V_{OUT}	-0.5 ∿ V_{CC}+0.5	
Input Diode Current		I_{IK}	±20	mA
Output Diode Current		I_{OK}	±20	
DC Output Current	(RCO)	I_{OUT}	±25	
	(QA ∿ QD)		±35	
DC V_{CC}/Ground Current		I_{CC}	±70	
Power Dissipation		P_D	500*	mW
Storage Temperature		T_{STG}	-65 ∿ 150	°C
Lead Temperature(10sec)		T_L	300	



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}				2.0	1.5	-	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	
					6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}				2.0	-	-	0.5	-	0.5	
					4.5	-	-	1.35	-	1.35	
					6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}		I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
					4.5	4.4	4.5	-	4.4	-	
					6.0	5.9	6.0	-	5.9	-	
			QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
				I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
			RCO	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
				I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC690P
TC74HC691P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA∿QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		RCO	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Off Leak Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0		40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (RCO)	t_{TLH}		2.0	-	30	75	-	95	
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (RCK - Q)	t_{pLH}		2.0	-	148	285	-	355	
	t_{pHL}		4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CCK - RCO)	t_{pLH}		2.0	-	128	250	-	315	
	t_{pHL}		4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($R/\overline{C}$ - Q)	t_{pLH}		2.0	-	104	200	-	250	
	t_{pHL}		4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (ENT - RCO)	t_{pLH}		2.0	-	56	110	-	140	
	t_{pHL}		4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	

TC74HC690P
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AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	160	305	-	380	ns
			4.5	-	40	61	-	76	
			6.0	-	12	52	-	65	
Propagation Delay Time ($\overline{CCLR}$ - RCO)	t_{pLH}		2.0	-	132	255	-	320	
			4.5	-	33	51	-	64	
			6.0	-	28	44	-	54	
Propagation Delay Time ($\overline{RCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$, $\overline{RCLR}$)	$t_{w(L)}$		2.0	-	44	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set up Time ($\overline{LOAD}$, ENT, ENP)	t_s		2.0	-	80	175	-	220	
			4.5	-	20	35	-	44	
			6.0	-	17	30	-	37	
Minimum Set up Time (A, B, C, D)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set up Time (CCK - RCK)	t_s		2.0	-	76	175	-	220	
			4.5	-	19	35	-	44	
			6.0	-	16	30	-	37	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	170	-	215	
			4.5	-	23	34	-	43	
			6.0	-	20	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	80	-	-	-	

TC74HC690P
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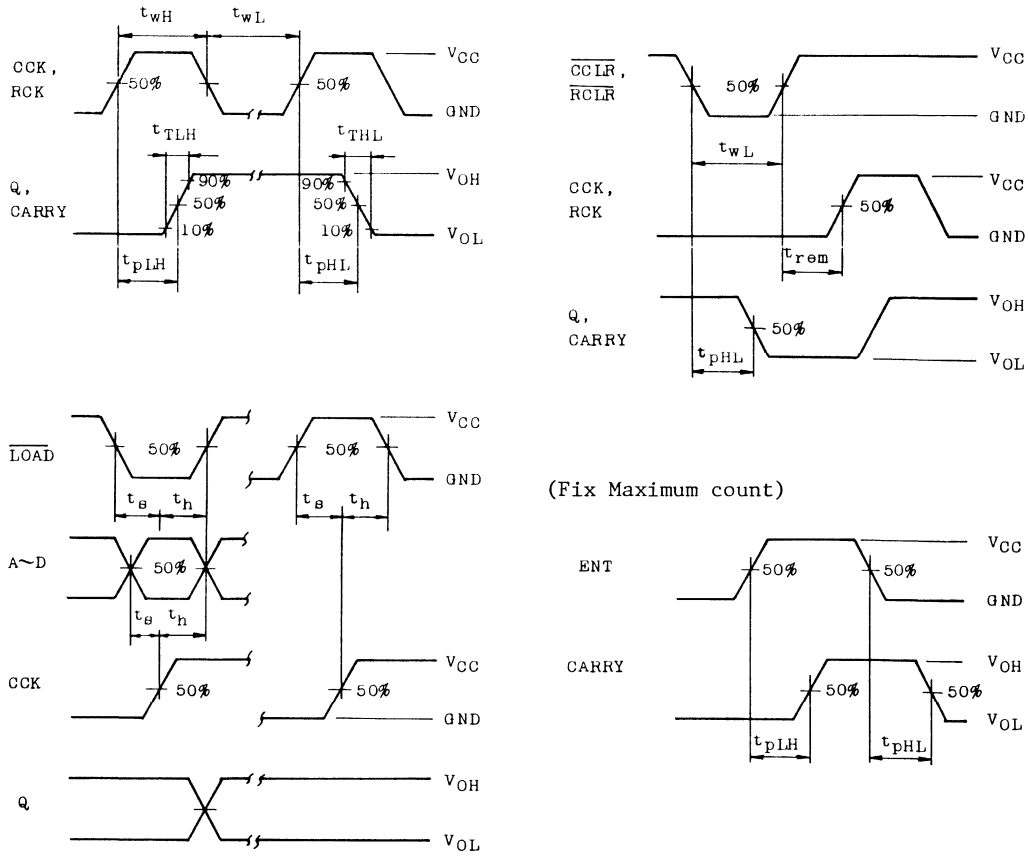
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 1)



TC74HC690P
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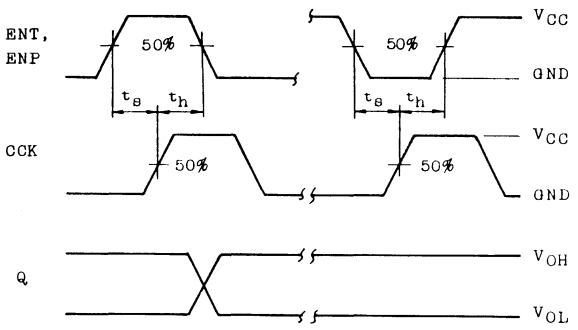
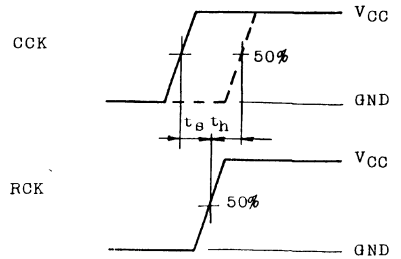
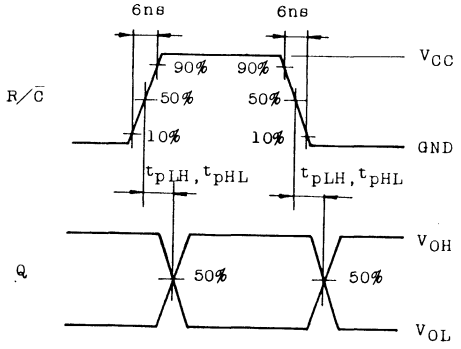
SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 2)

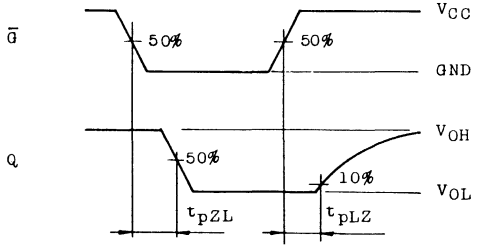






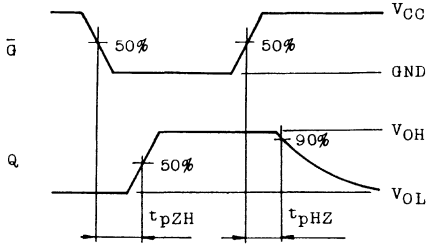
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

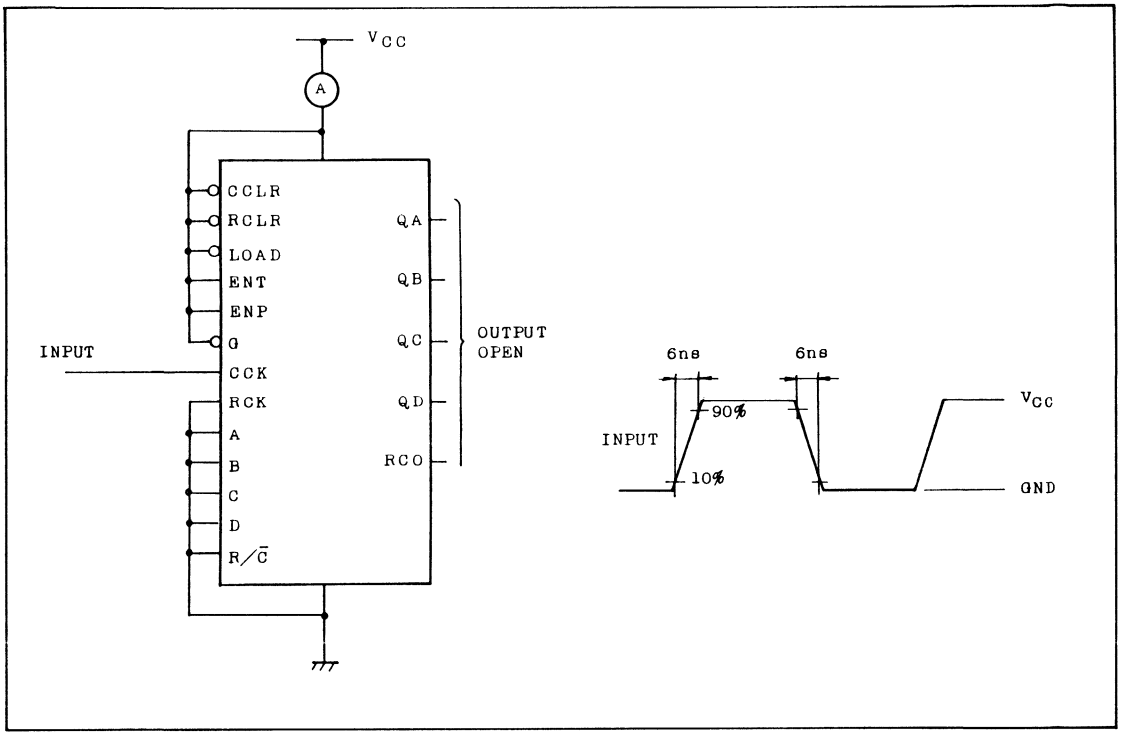


t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.



I_{CC}(Opr.) TEST WAVEFORM



TC74HC692P
TC74HC693P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC692P DECADE COUNTER REGISTER
TC74HC693P 4-BIT BINARY COUNTER REGISTER

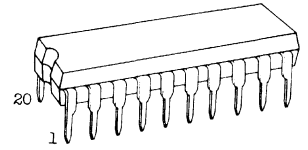
The TC74HC692/693 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalnet LSTTL while maintaining the CMOS low power dissipation.

TC74HC692 is BCD DECADE COUNTER, TC74HC693 is 4-BIT BINARY COUNTER, these devices have Registers respectively.
If LOAD input ($\overline{LOAD}$) is held "L", DATA input (A ∿ D) are loaded in internal counter at positive edge of counter clock input ($\overline{CCK}$). And at counter mode, internal counter counts up at positive edge of counter clock. If counter clear input ($\overline{CCLR}$) is held "L", internal counter cleared synchronously to counter clock.

Internal counter's outputs are stored in output register at positive edge of register clock (RCK). If register clear input ($\overline{RCLR}$) is held "L", the register cleared synchronously to register clock. At this point, internal counter outputs no change. The outputs ($Q_A \sim Q_D$) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$).
Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

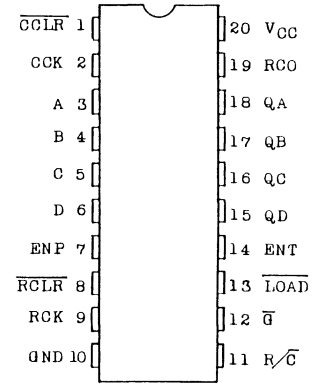


DIP20(3D20A-P)

FEATURES:

- High Speed ..... f_{MAX}=33MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads (For $Q_A \sim Q_D$)
  10 LSTTL Loads (For RCO)
- Symmetrical Output Impedance
  $|I_{OH}|=I_{OL}$=6mA(Min.) for $Q_A \sim Q_D$ Output
  $|I_{OH}|=I_{OL}$=4mA(Min.) for RCO Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS692/693)

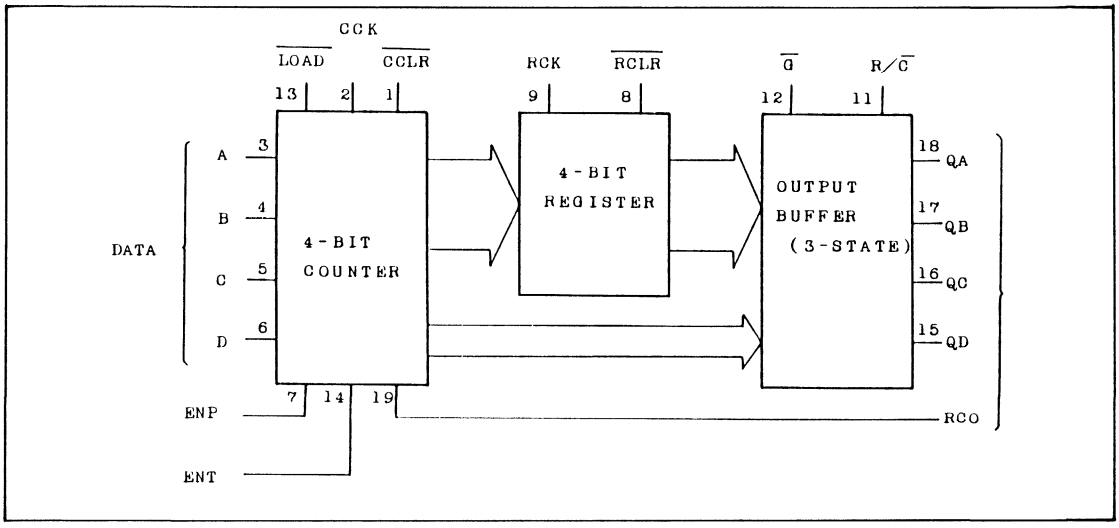
PIN ASSIGNMENT



(TOP VIEW)

TC74HC692P
TC74HC693P

BLOCK DIAGRAM



TRUTH TABLE

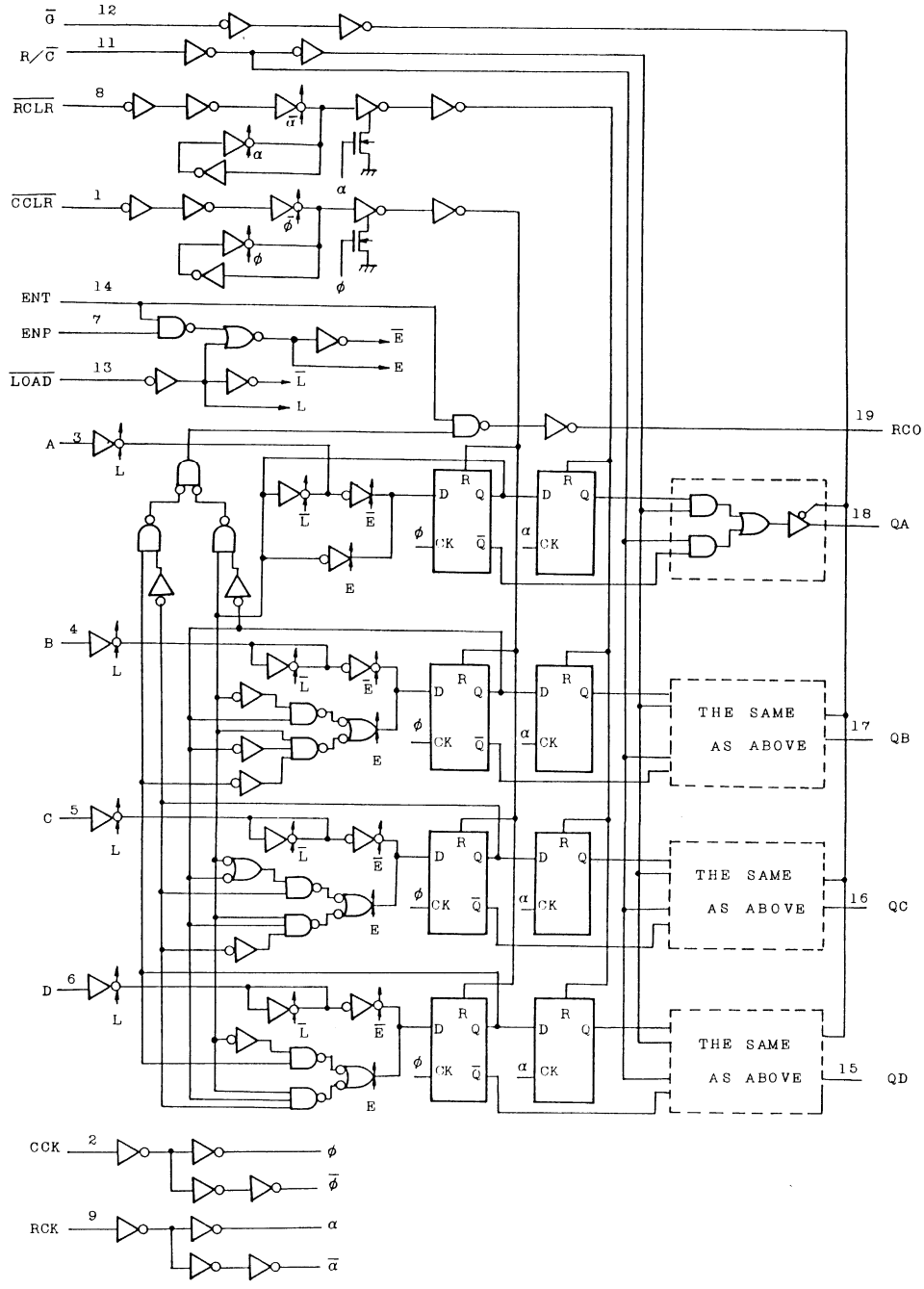
INPUTS									OUTPUTS				FUUCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↓	X	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	↓	X	X	L	L	NO CHANGE				COUNT DISABLE NO CHANGE
H	H	X	L	↓	X	X	L	L					
H	H	H	H	↓	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	↓	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	X	H	↓	H	L	a′	b′	c′	d′	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO CHANGE

X: Don't Care
Z: High Impedance
a∿d: The level of steady state input voltage at inputs A∿D respectively.
a'∿d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.

TC74HC692 RCO = QA • QD • ENT
TC74HC693 RCO = QA • QB • QC • QD • ENT

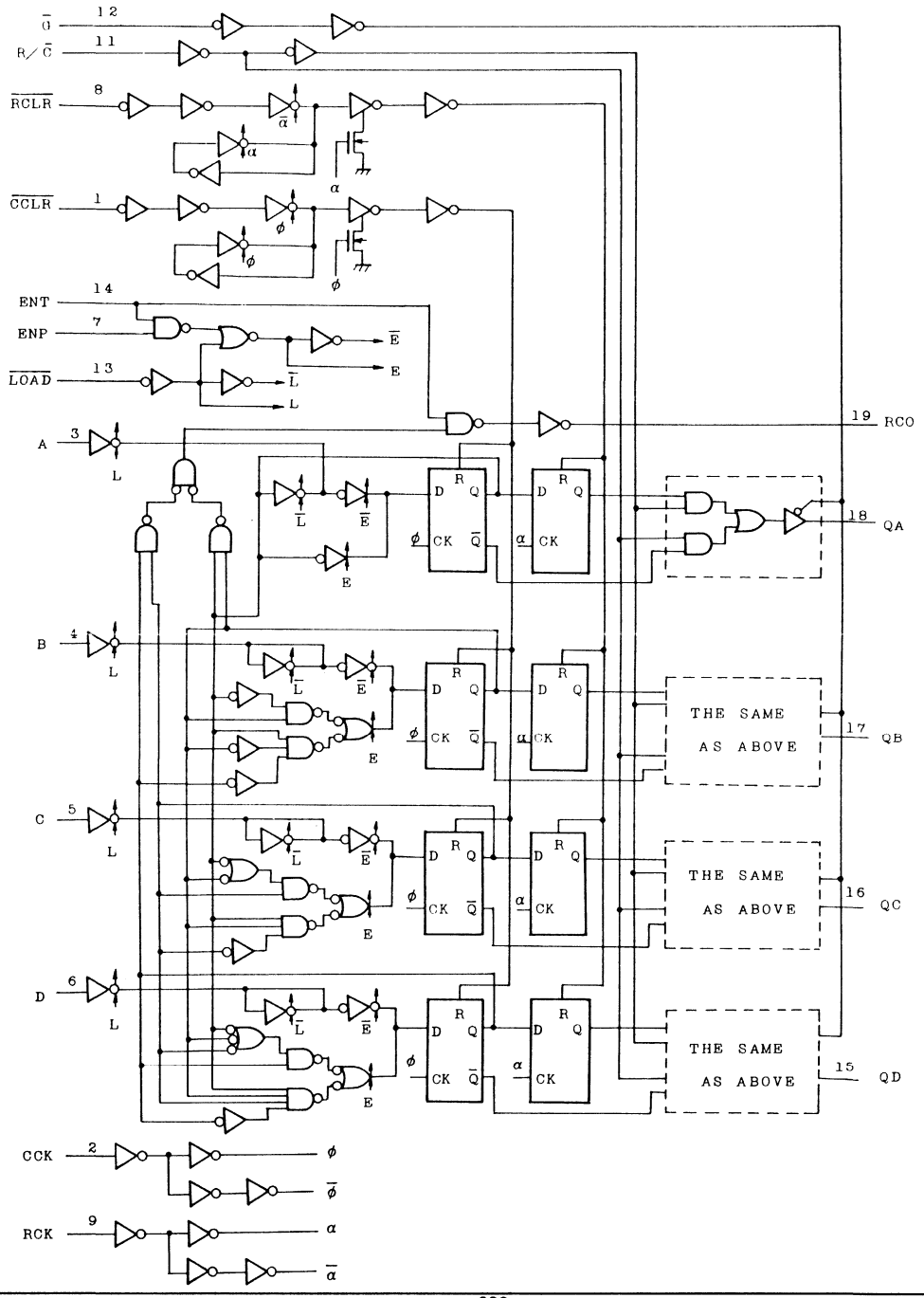
TC74HC692P
TC74HC693P

LOGIC DIAGRAM TC74HC692



TC74HC692P
TC74HC693P

LOGIC DIAGRAM TC74HC693



TC74HC692P
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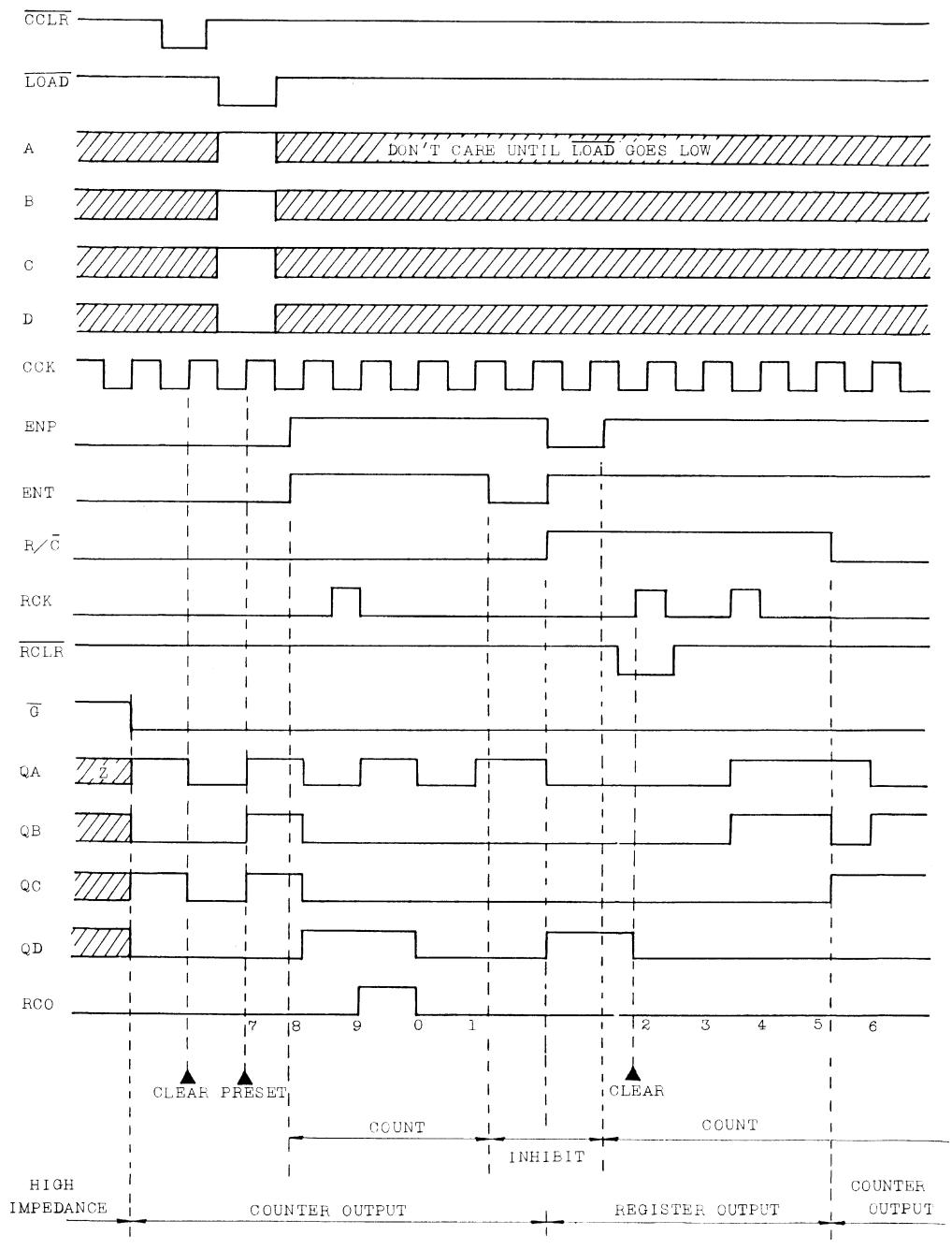
TIMING CHART TC74HC692



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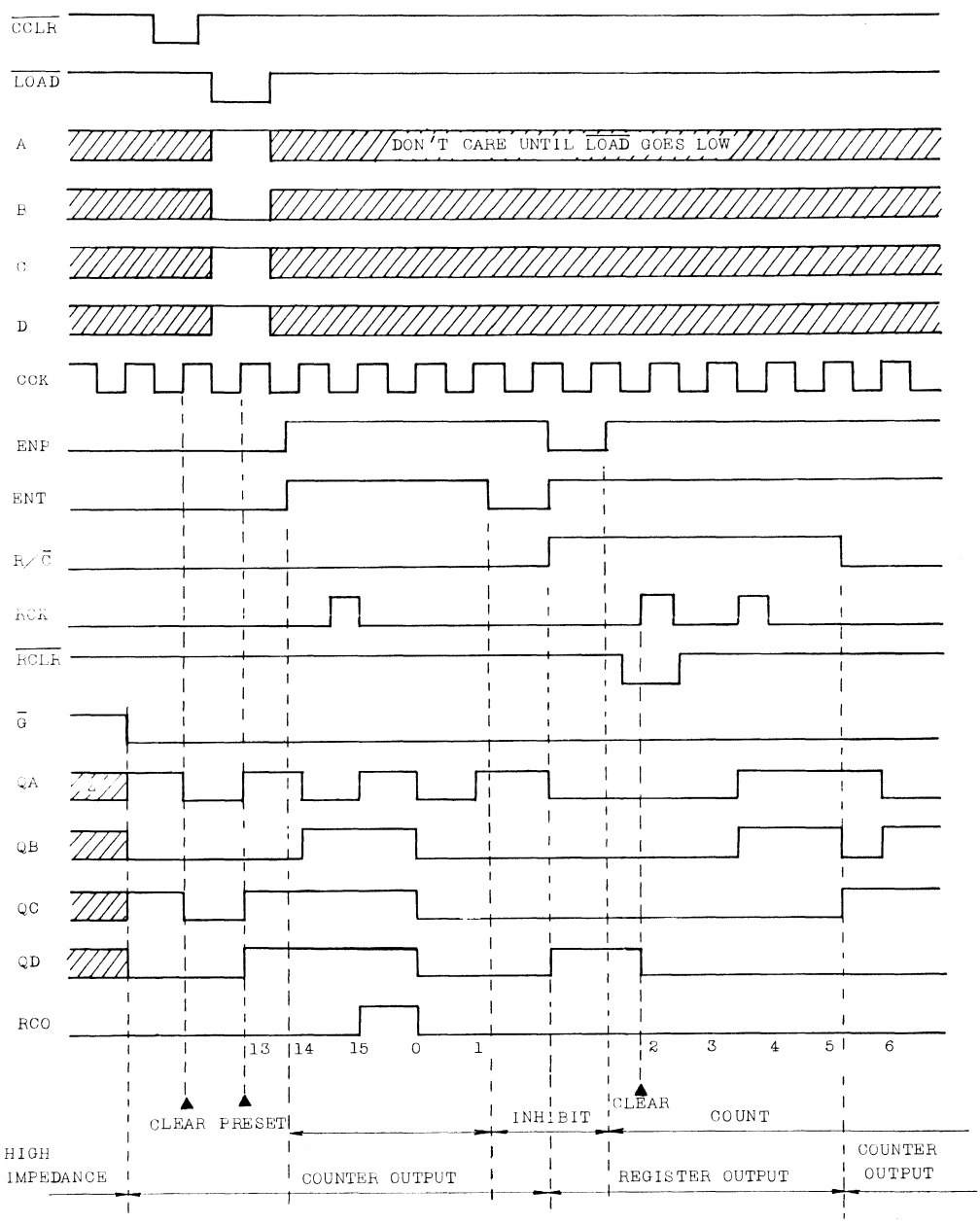
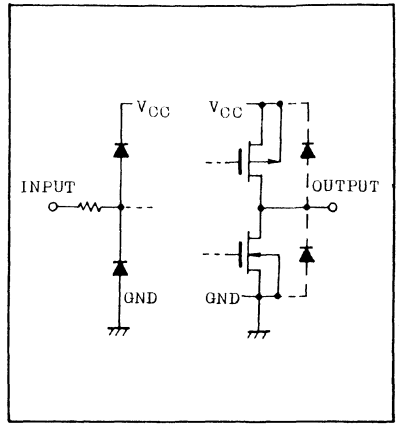
TIMING CHART TC74HC693



TC74HC692P
TC74HC693P

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage Range		V_{CC}	-0.5 ∿ 7	V
DC Input Voltage		V_{IN}	-0.5 ∿ V_{CC}+0.5	
DC Output Voltage		V_{OUT}	-0.5 ∿ V_{CC}+0.5	
Input Diode Current		I_{IK}	±20	mA
Output Diode Current		I_{OK}	±20	
DC Output Current	(RCO)	I_{OUT}	±25	
	(QA ∿ QD)		±35	
DC V_{CC}/Ground Current		I_{CC}	±70	
Power Dissipation		P_D	500*	mW
Storage Temperature		T_{STG}	-65 ∿ 150	°C
Lead Temperature(10sec)		T_L	300	



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		RCO	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

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DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ~ QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		RCO	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Off Leak Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (RCO)	t_{TLH}		2.0	-	30	75	-	95	
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH}		2.0	-	132	260	-	325	
	t_{pHL}		4.5	-	33	52	-	65	
			6.0	-	28	44	-	55	
Propagation Delay Time (RCK - Q)	t_{pLH}		2.0	-	136	260	-	325	
	t_{pHL}		4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time (CCK - RCO)	t_{pLH}		2.0	-	108	210	-	265	
	t_{pHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (R/C - Q)	t_{pLH}		2.0	-	92	180	-	225	
	t_{pHL}		4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (ENT - RCO)	t_{pLH}		2.0	-	48	95	-	120	
	t_{pHL}		4.5	-	12	19	-	24	
			6.0	-	10	16	-	20	

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AC ELECTRICAL CHARACTERISTICS (Continued)

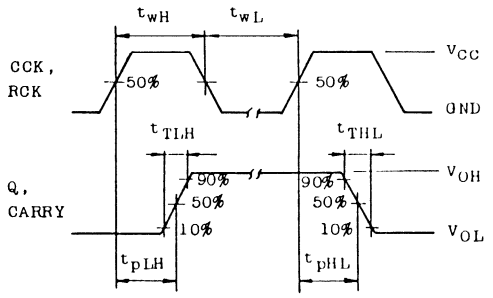
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$		2.0	-	48	125	-	160	ns
	$t_{w(L)}$		4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time ($\overline{LOAD}$, ENT, ENP)	t_s		2.0	-	68	150	-	190	
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	33	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time ($\overline{CCLR}$, $\overline{RCLR}$)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	68	150	-	190	
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	33	
Minimum Data Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	64	130	-	165	
	t_{pZH}		4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
3-State Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	80	145	-	180	
	t_{pHZ}		4.5	-	20	29	-	36	
			6.0	-	17	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	95	-	-	-	

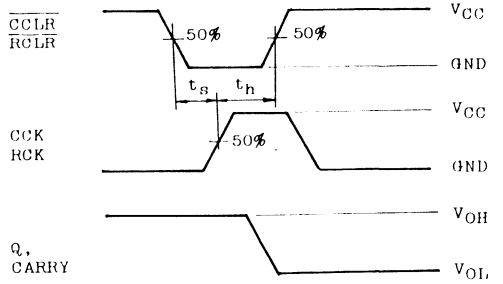
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

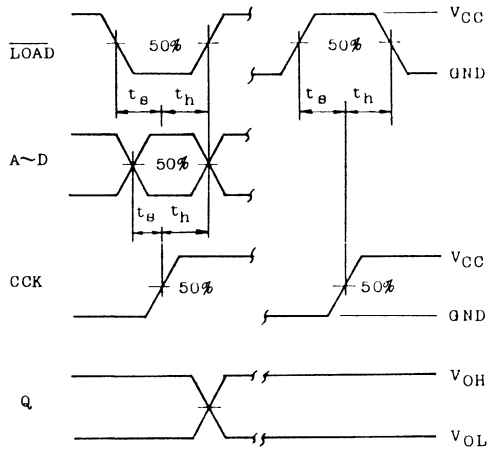
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC692P
TC74HC693P

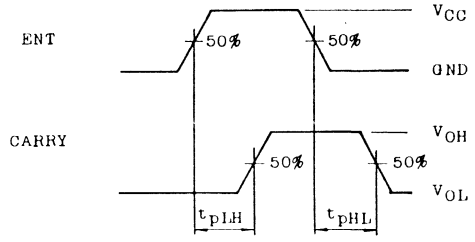
SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 1)

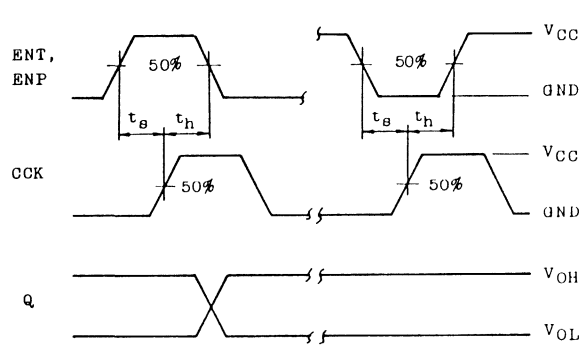


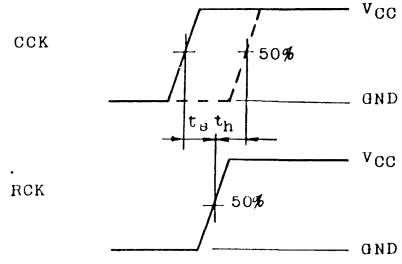




(Fix Maximum count)

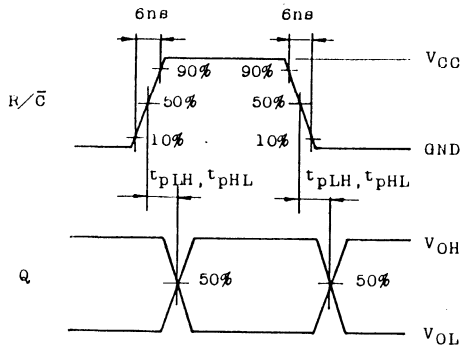






TC74HC692P
TC74HC693P

SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 2)

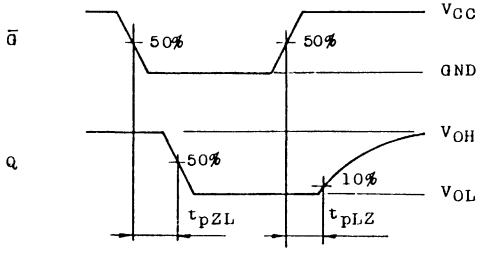


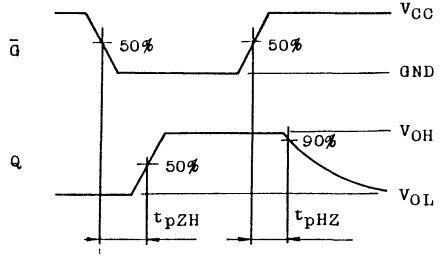
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

t_{pHZ}, t_{pZH}

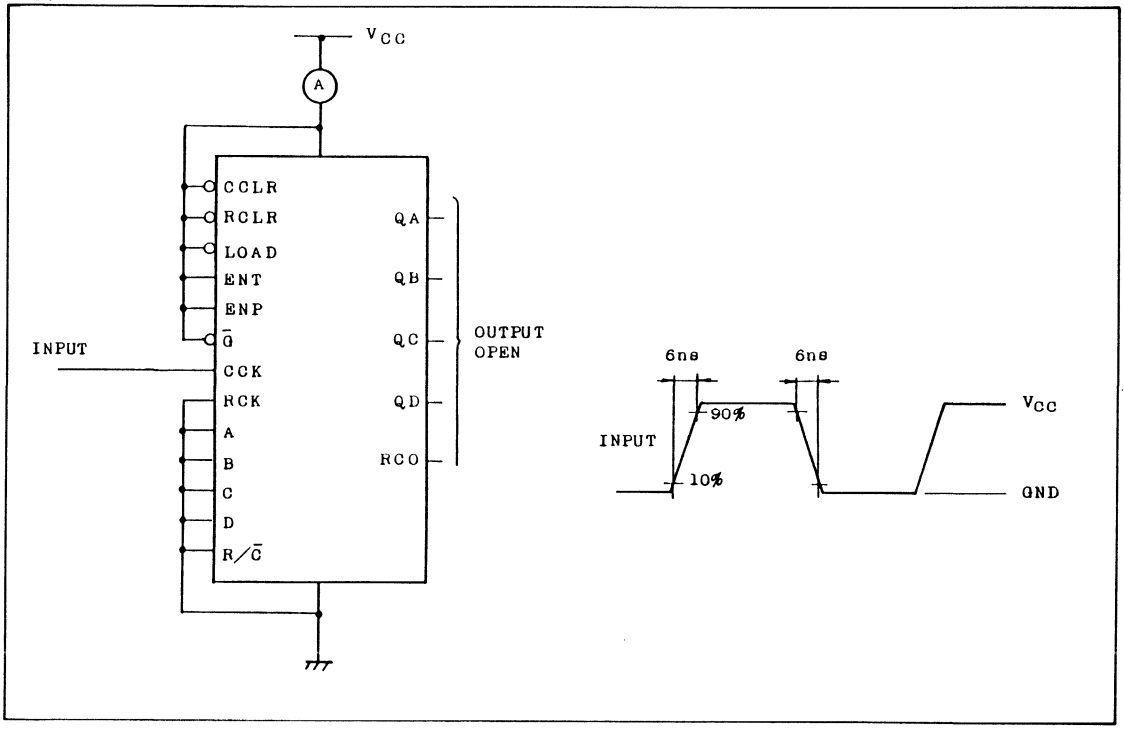
The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.





TC74HC692P
TC74HC693P

I_{CC}(Opr.) TEST WAVEFORM



TC74HC696P
TC74HC697P

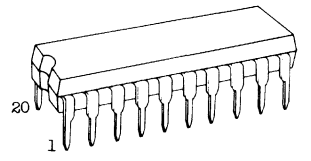
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC696P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC697P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC696 is BCD DECADE COUNTER, and TC74HC697 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input U/$\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ~ QD) are selected internal counter outputs or register outputs respectively by output select input (R/$\overline{C}$). Their clear function are cleared asynchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=33MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ~ QD)
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ~ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{pLH}\simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ~ 6V
- Pin and Function Compatible with LSTTL (74LS696/697)



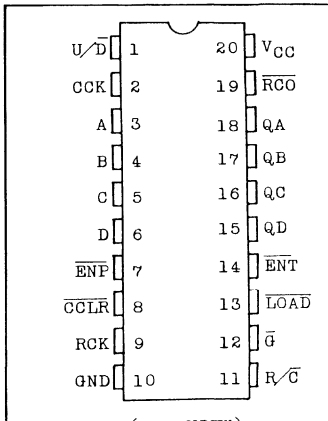
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ~ QD) ±20 (RCO)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC696P
TC74HC697P

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L					
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

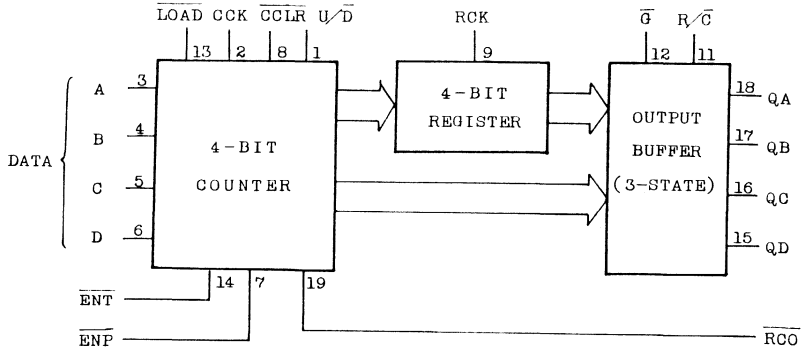
X: Don't care
Z: High Impedance
a ∿ d : The level of steady state inputs at inputs A through D respectively.
a' ∿ d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

TC74HC696 $\overline{RCO}=\overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)}$

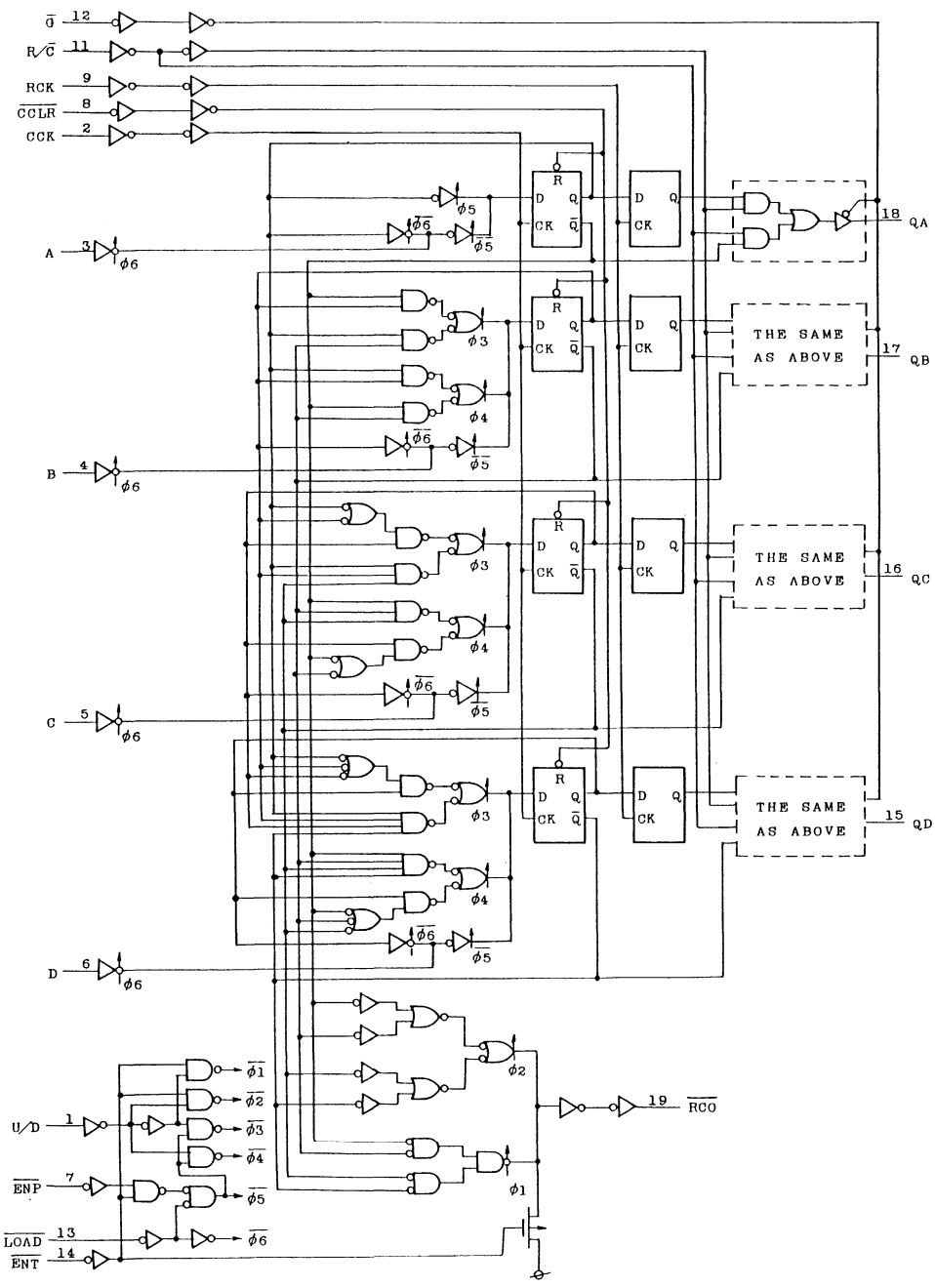
TC74HC697 $\overline{RCO}=\overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

BLOCK DIAGRAM



TC74HC696P
TC74HC697P

LOGIC DIAGRAM TC74HC696



TC74HC696P
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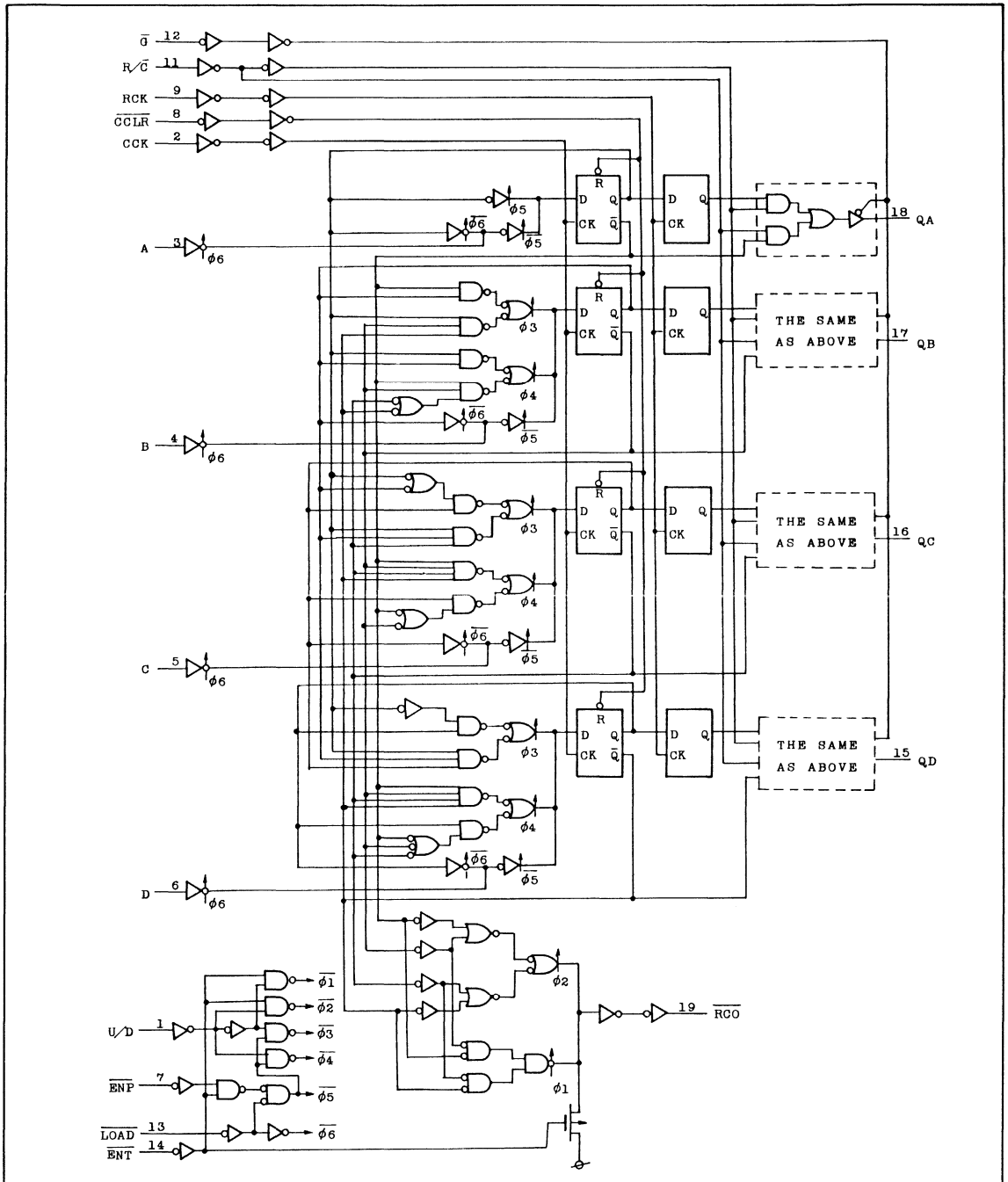
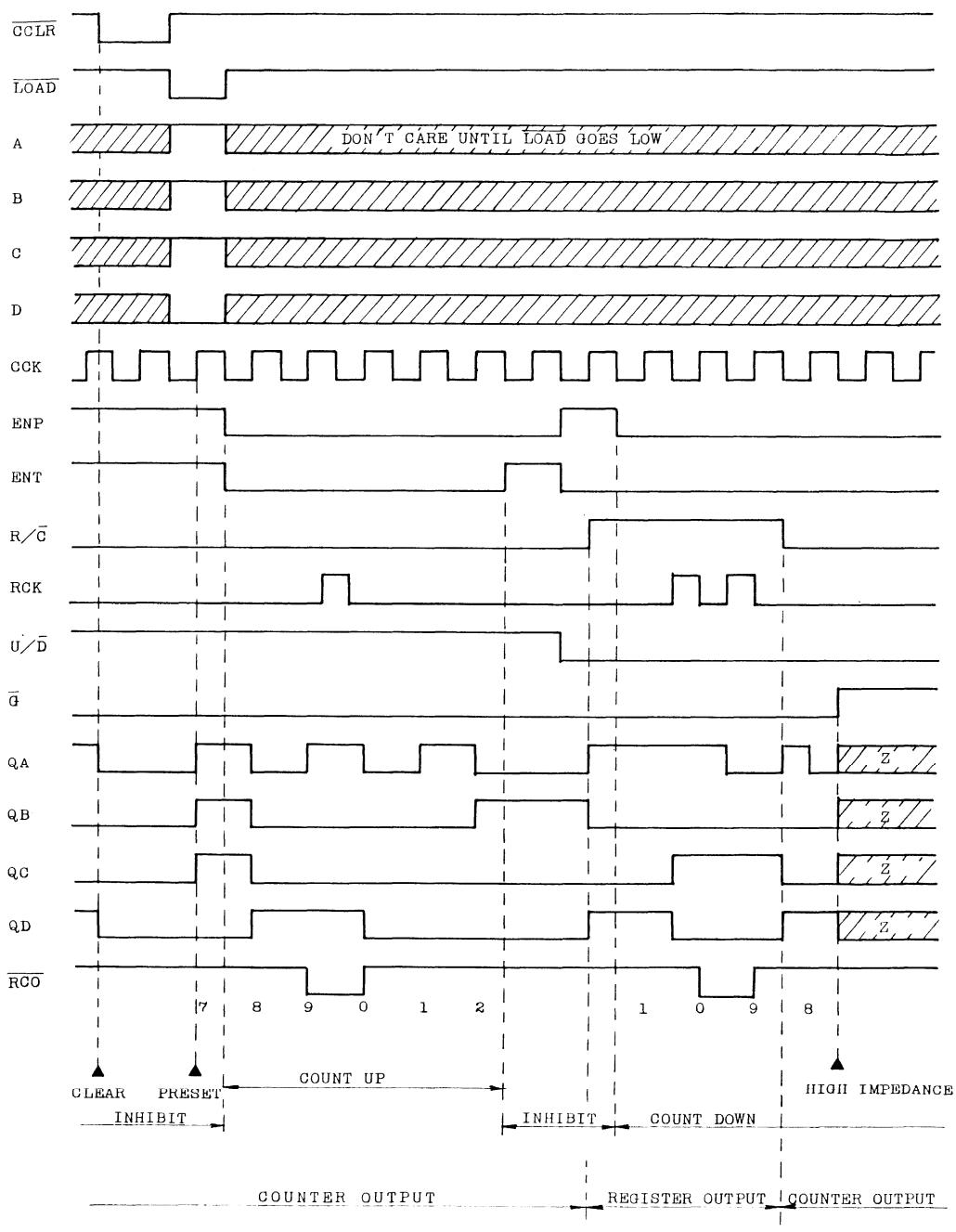
LOGIC DIAGRAM TC74HC697



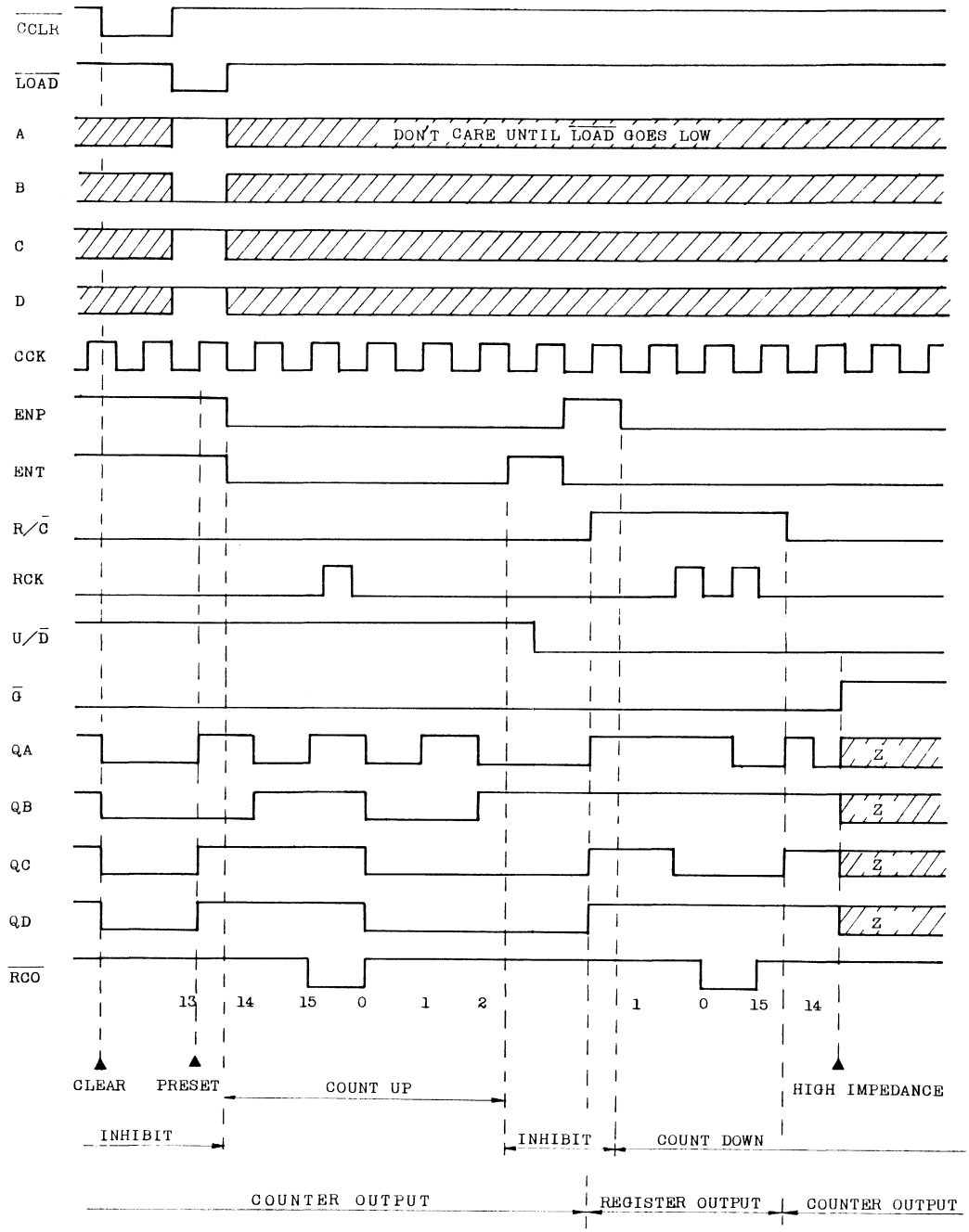
TC74HC696P
TC74HC697P

TIMING CHART TC74HC696



TC74HC696P
TC74HC697P

TIMING CHART TC74HC697

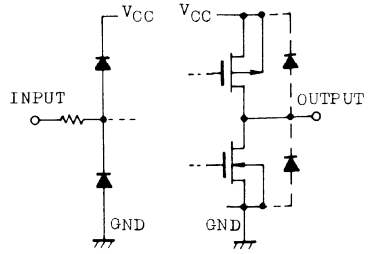


TC74HC696P
TC74HC697P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC696P
TC74HC697P

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	160	305	-	380	
			4.5	-	40	61	-	76	
			6.0	-	34	52	-	65	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	225	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{ENT}$ - RCO)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pHL}		2.0	-	172	325	-	405	
			4.5	-	43	65	-	81	
			6.0	-	37	55	-	69	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Widht (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	96	225	-	280	
			4.5	-	24	45	-	56	
			6.0	-	20	38	-	48	

TC74HC696P
TC74HC697P

AC ELECTRICAL CHARACTERISTICS (Continued)

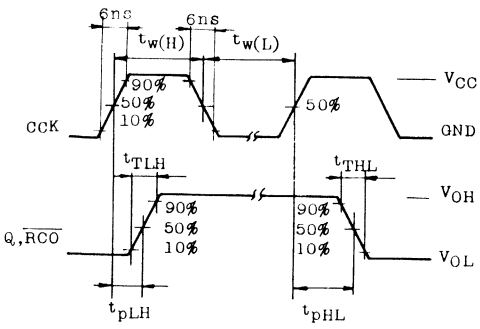
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	20	75	-	95	ns
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	52	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
Minimum Set-up Time ($U/\overline{D}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC696		-	90	-	-	-	
		TC74HC697		-	92	-	-	-	

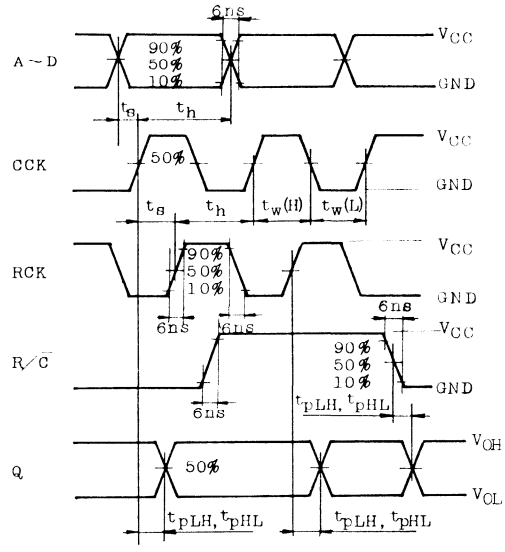
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

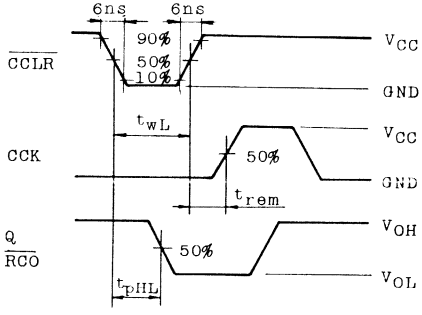
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

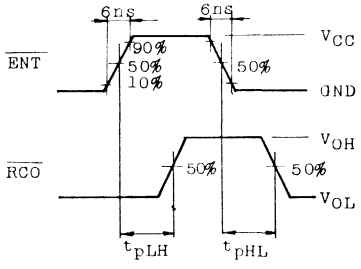
TC74HC696P
TC74HC697P

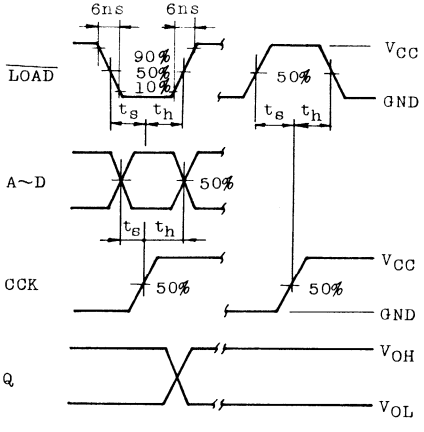
SWITCHING CHARACTERISTICS TEST WAVEFORM

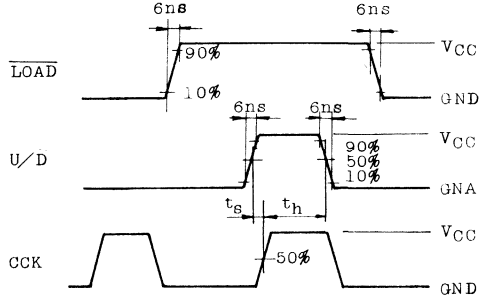








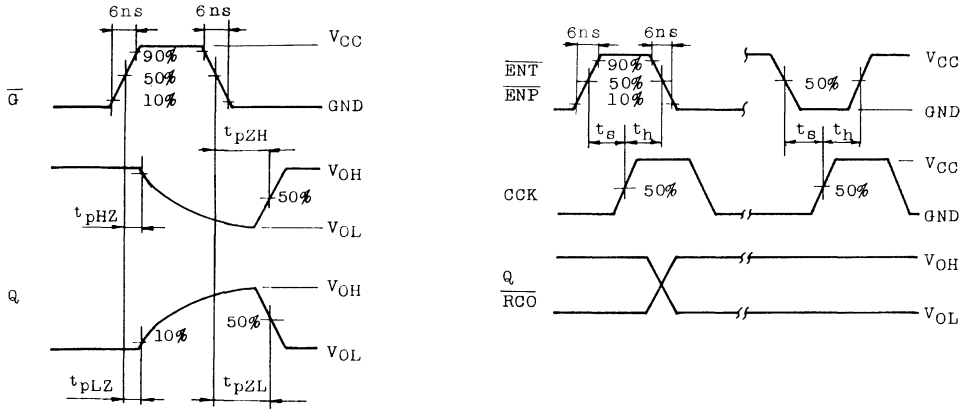




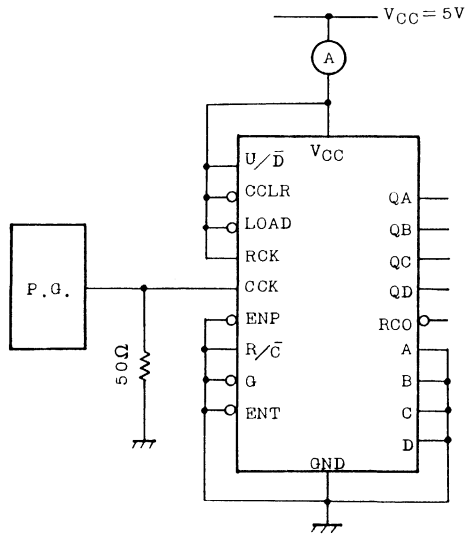
TC74HC696P
TC74HC697P

SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE



$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4002P/F

TC74HC4002P/F DUAL 4-INPUT NOR GATE

The TC74HC4002 is a high speed CMOS 4-INPUT NOR GATE fabricated with silicon gate C²MOS technology.

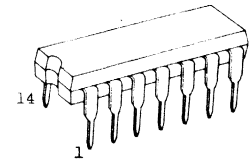
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output.

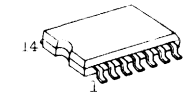
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4002B

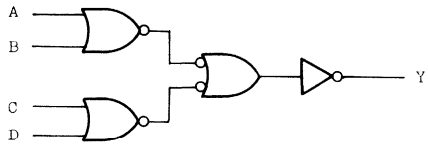


DIP14(3D14A-P)

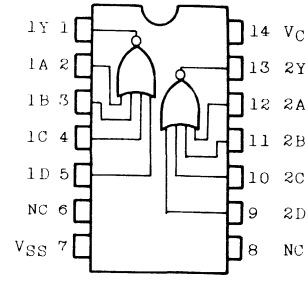


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC4002P/F

ABSOLUTE MAXIMUM RATINGS

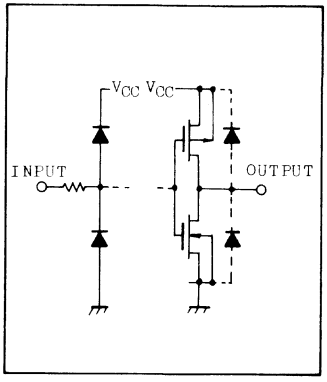
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

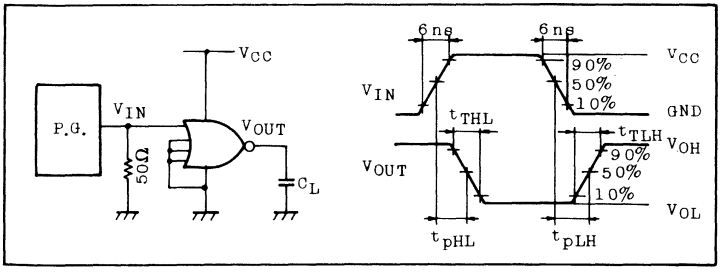
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

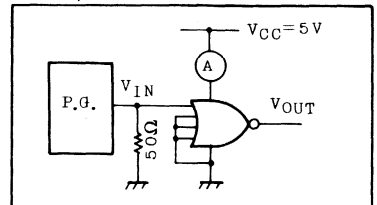
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	105	-	130	ns
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	26	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC4017P/F

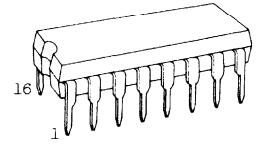
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4017P/F DECADE COUNTER/DIVIDER

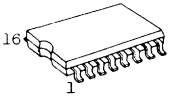
The TC74HC 4017 is a high speed CMOS DECADE JOHNSON COUNTER fabricated with silicon C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 5-stage divided-by-10 Johnson counter with 10 decoded output (Q0 - Q10) and carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{CE}$ input is held low, or it is advanced on the negative edge of the clock enable signal ($\overline{CE}$) when CLOCK input is held high, and selected one of ten outputs goes high. Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4017B



DIP16(3D16A-P)



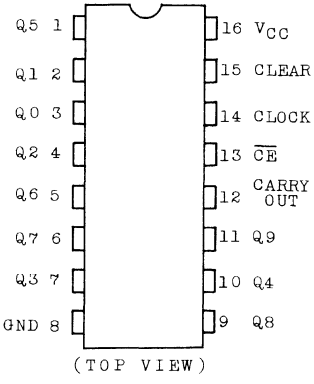
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

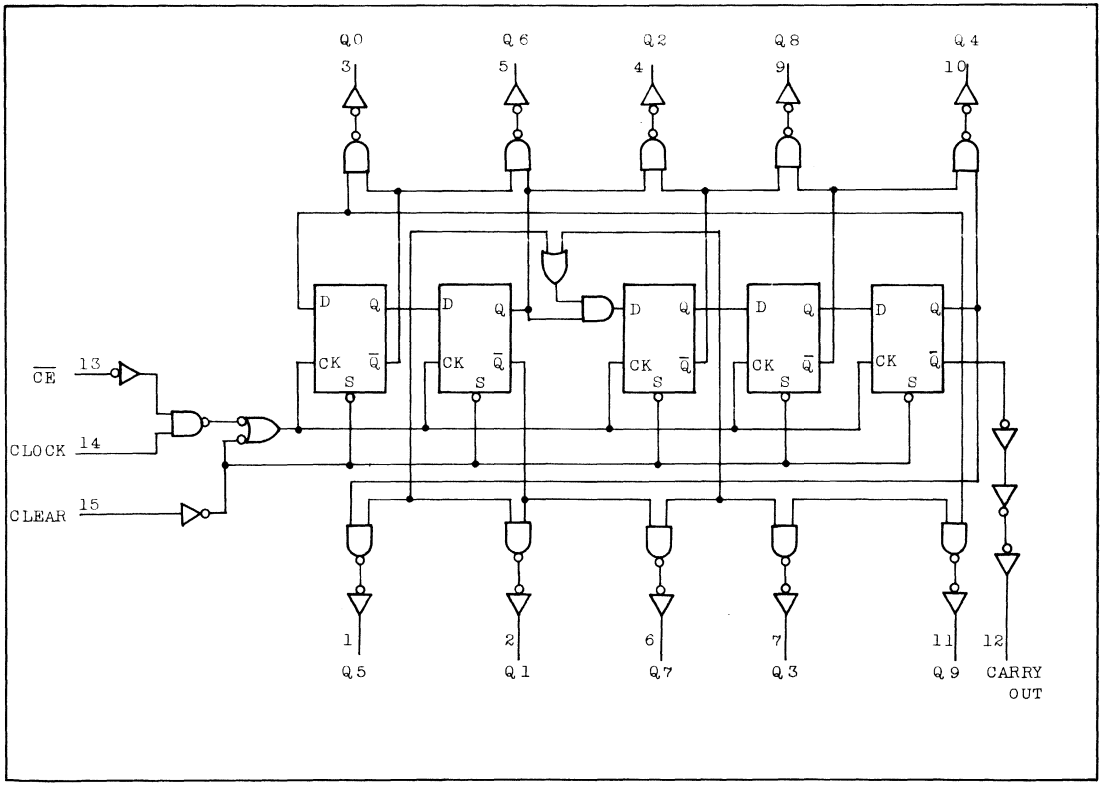
TC74HC4017P/F

TRUTH TABLE

CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
⌐¯	L	L	Qn+1
¯⌐	L	L	Qn
H	⌐¯	L	Qn
H	¯⌐	L	Qn+1

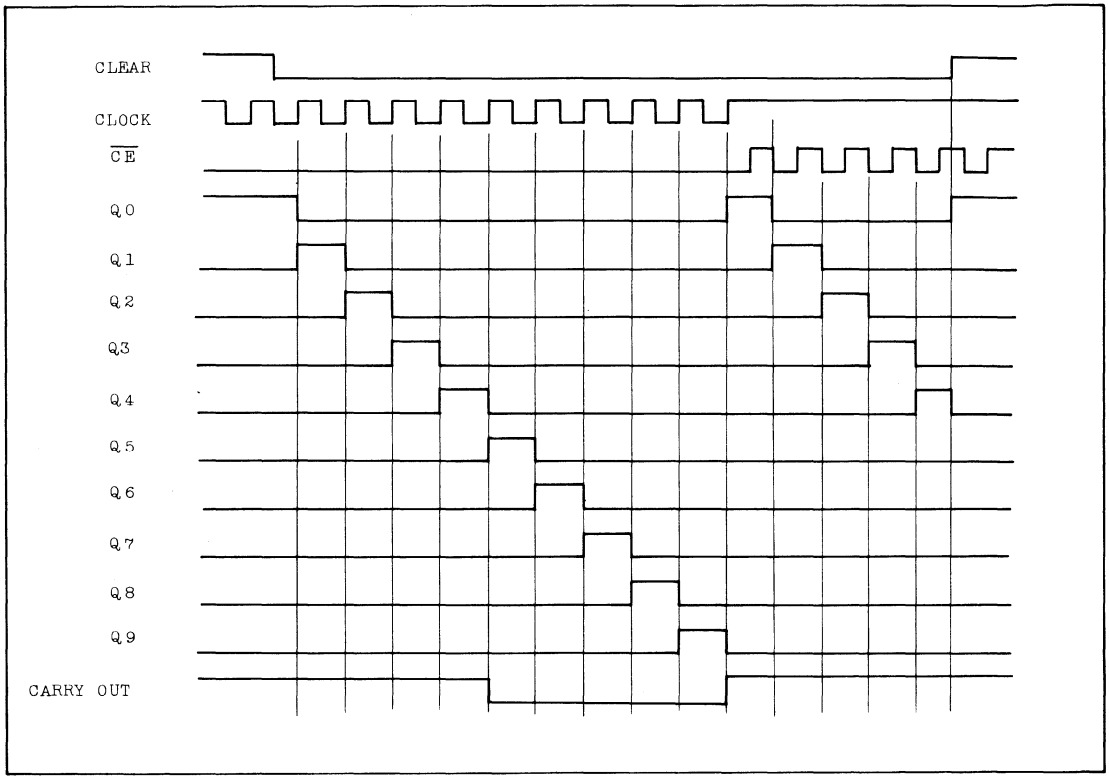
X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



TC74HC4017P/F

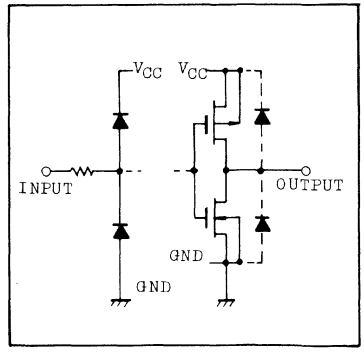
TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK, $\overline{CE}$ - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

TC74HC4017P/F

AC ELECTRICAL CAHRACTERISTICS (Continued)

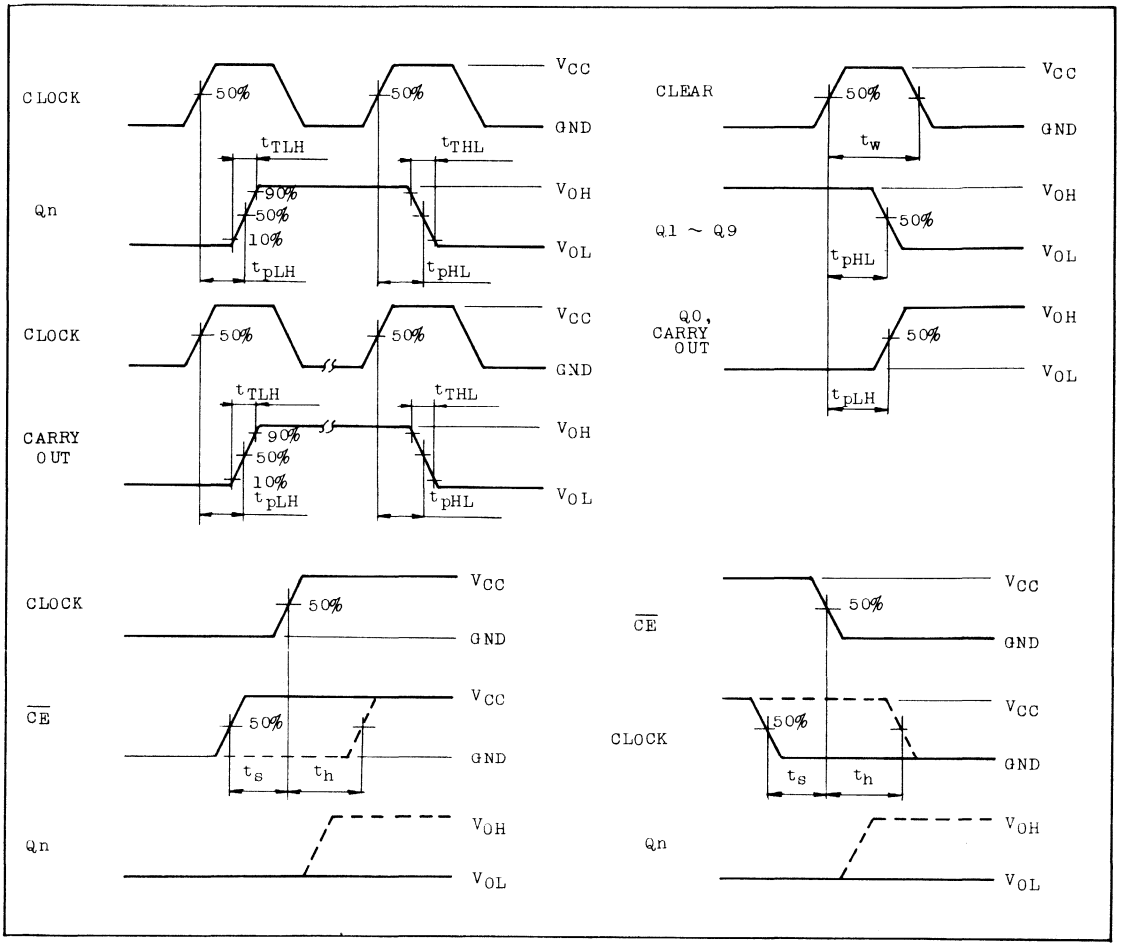
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	41	-	20	-	
			6.0	29	48	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
	$t_{w(H)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	74	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

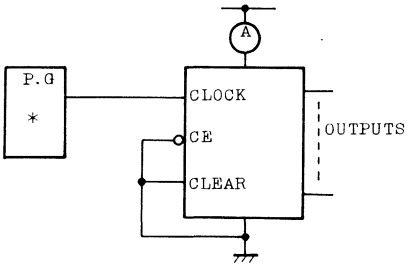
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4017P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4020P/F

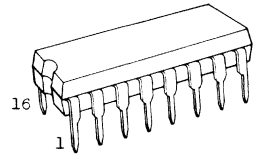
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4020P/F 14-STAGE BINARY COUNTER

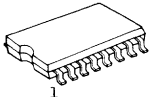
The TC74HC4020 is a high speed CMOS 14-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4020B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accoumplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. Twelve kinds of divided output are provided; 1'st and 4 stage thru 14 stage. And at the last stage, 1/16384 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V∿6V
- Pin and Function Compatible with 4020B.



DIP16(3D16A-P)



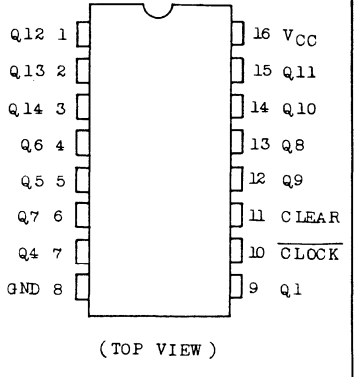
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

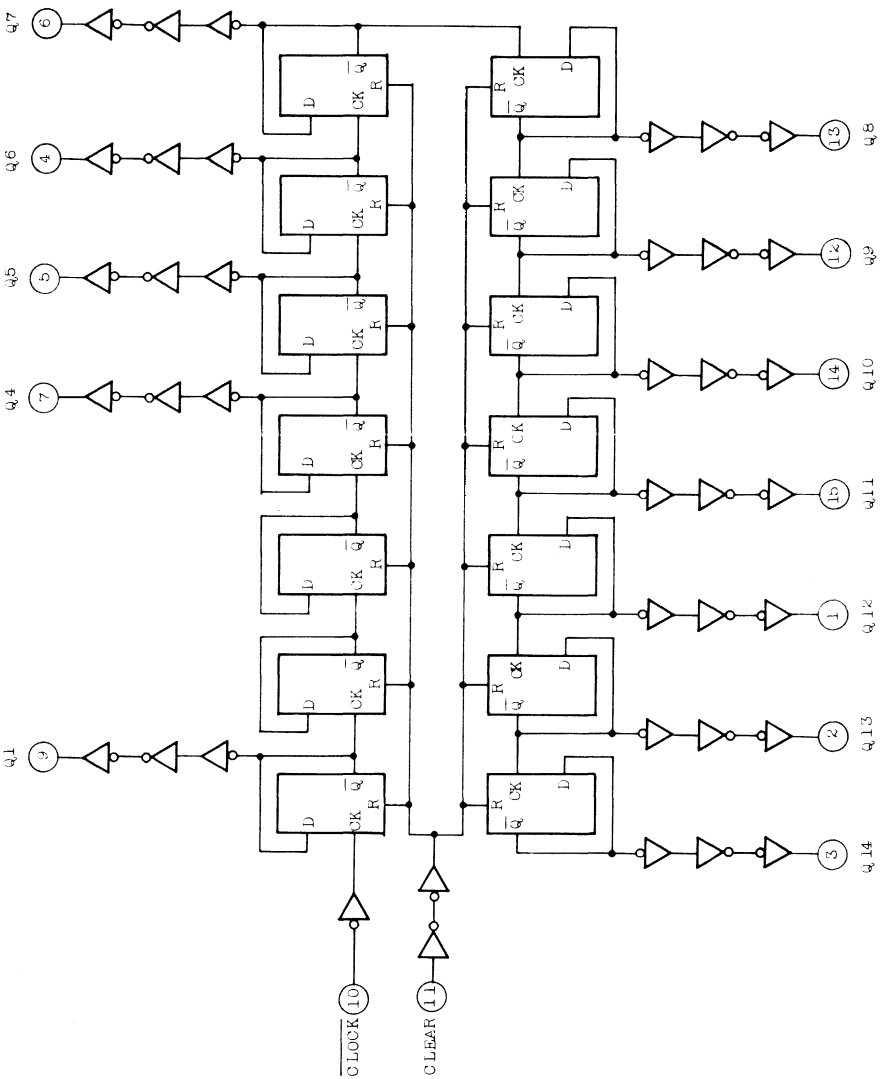
TC74HC4020P/F

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

X : DON'T CARE

LOGIC DIAGRAM

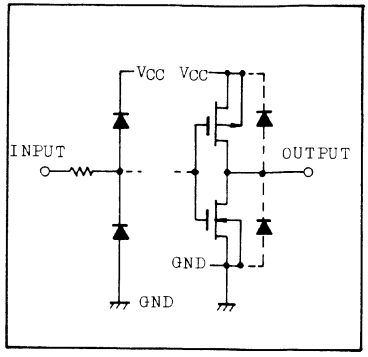


TC74HC4020P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

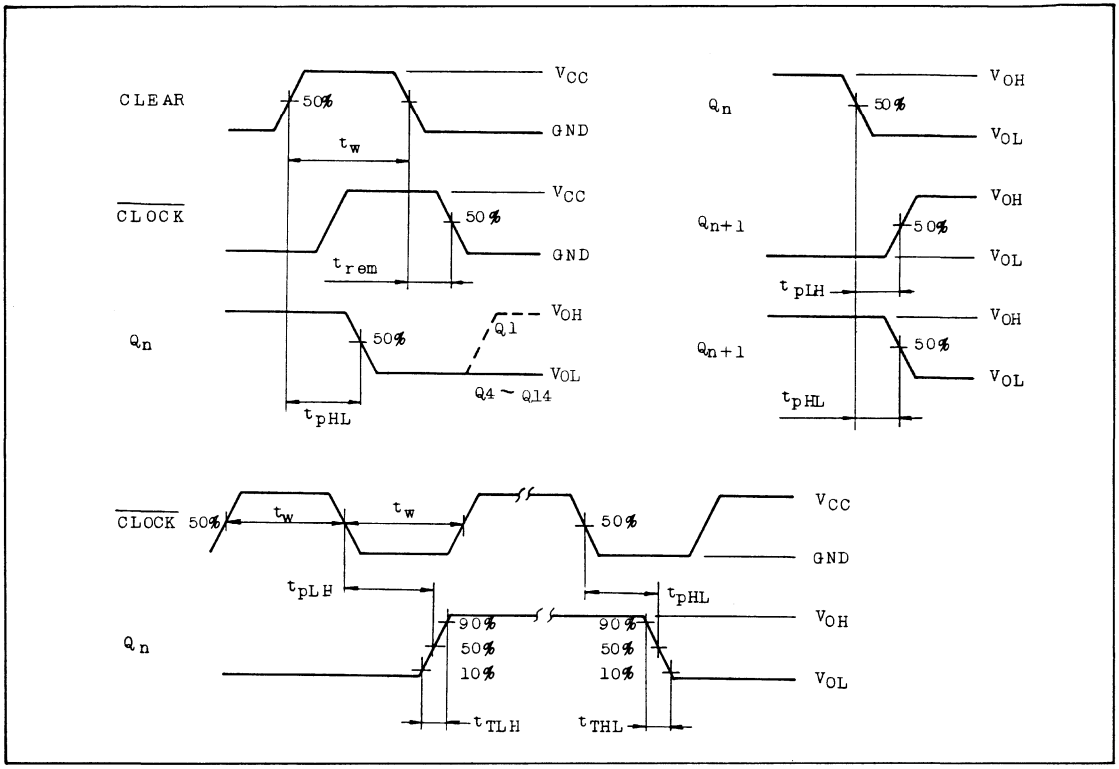
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time (Q_n - Q_{n+1})	t_{pLH} t_{pHL}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time (CLEAR)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	23	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

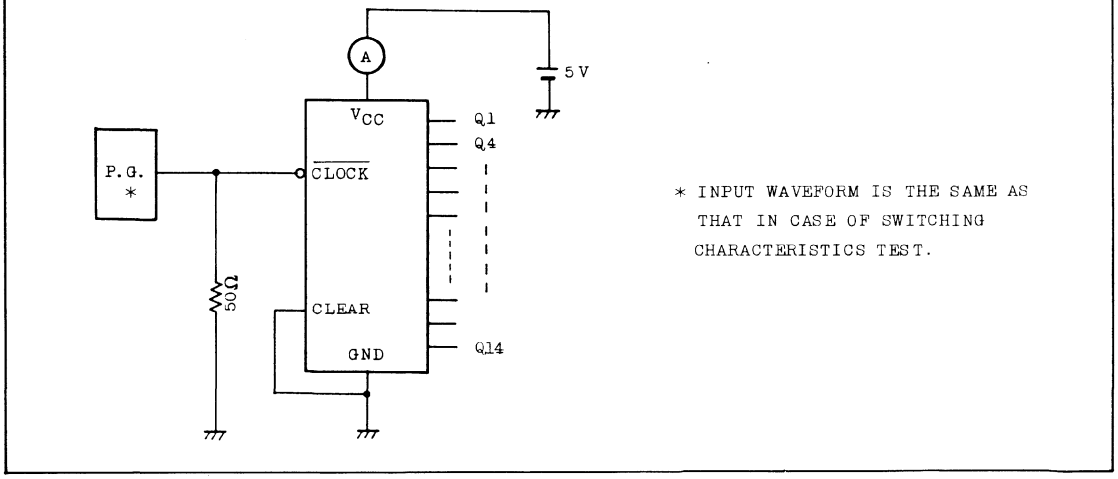
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4020P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4022P/F

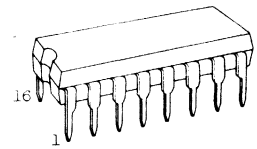
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4022P/F OCTAL COUNTER/DIVIDER

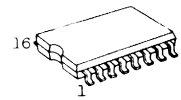
The TC74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 4-stage divide-by-8 Johnson counter with 8 decoded output ($Q_0 - Q_7$) and Carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{\text{CLOCK ENABLE}}$ input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high.
Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=43MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}= 4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4022B



DIP16(3D16A-P)



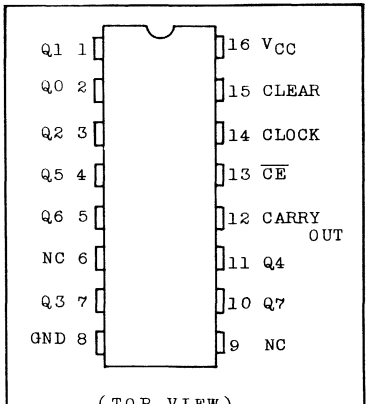
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

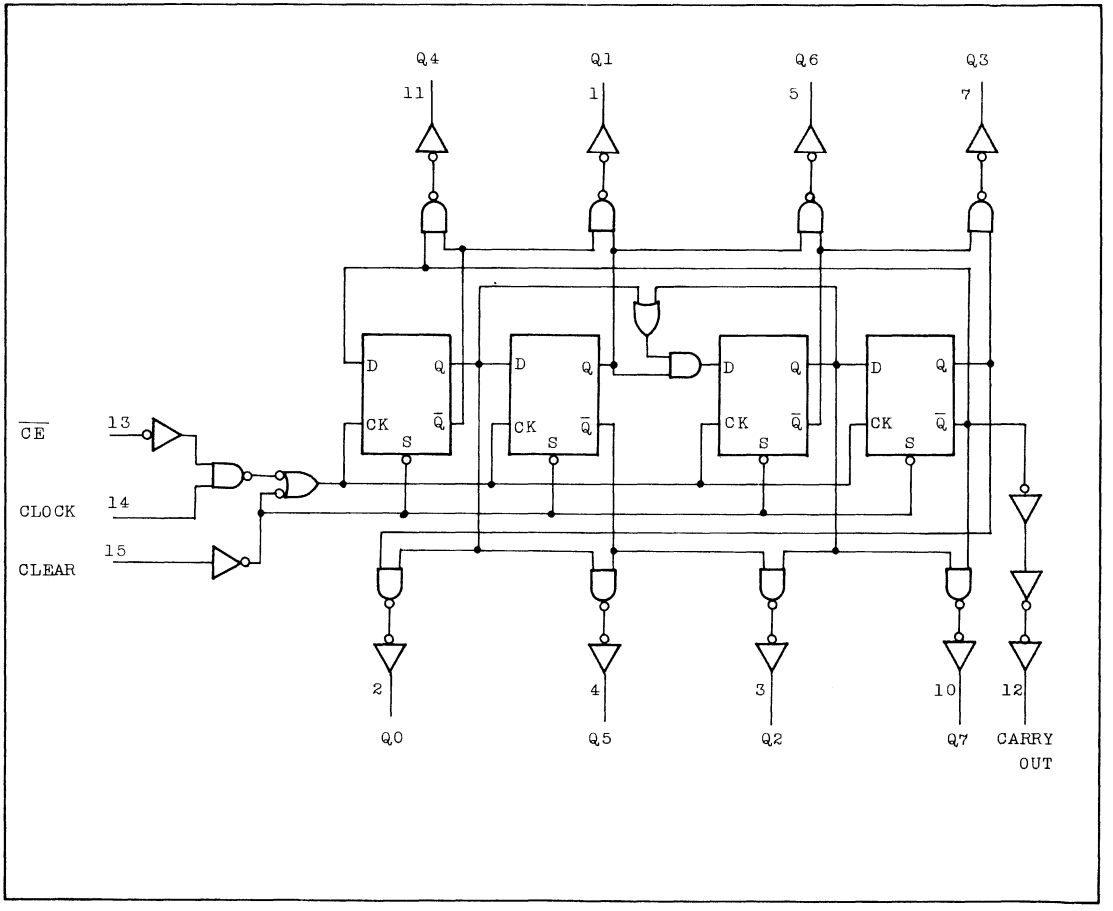
TC74HC4022P/F

TRUTH TABLE

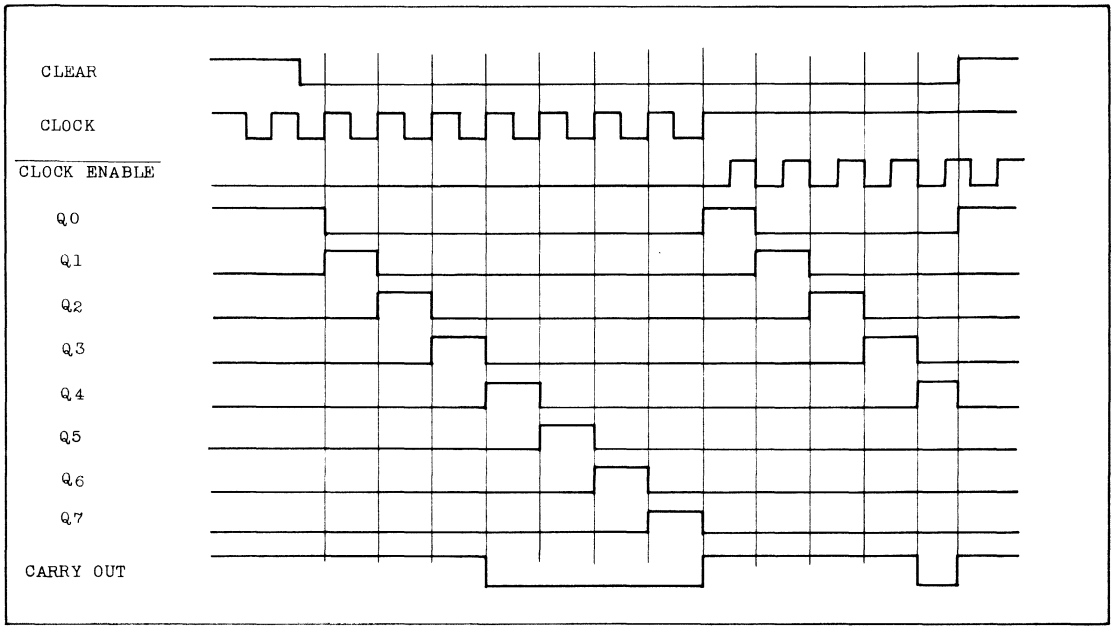
CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↓	L	L	Qn+1
↑	L	L	Qn
H	↓	L	Qn
H	↑	L	Qn+1

X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



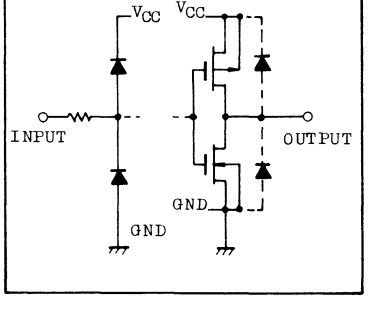
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4022P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Suppl Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

AC ELECTRICAL CHARACTERISTICS (Continued)

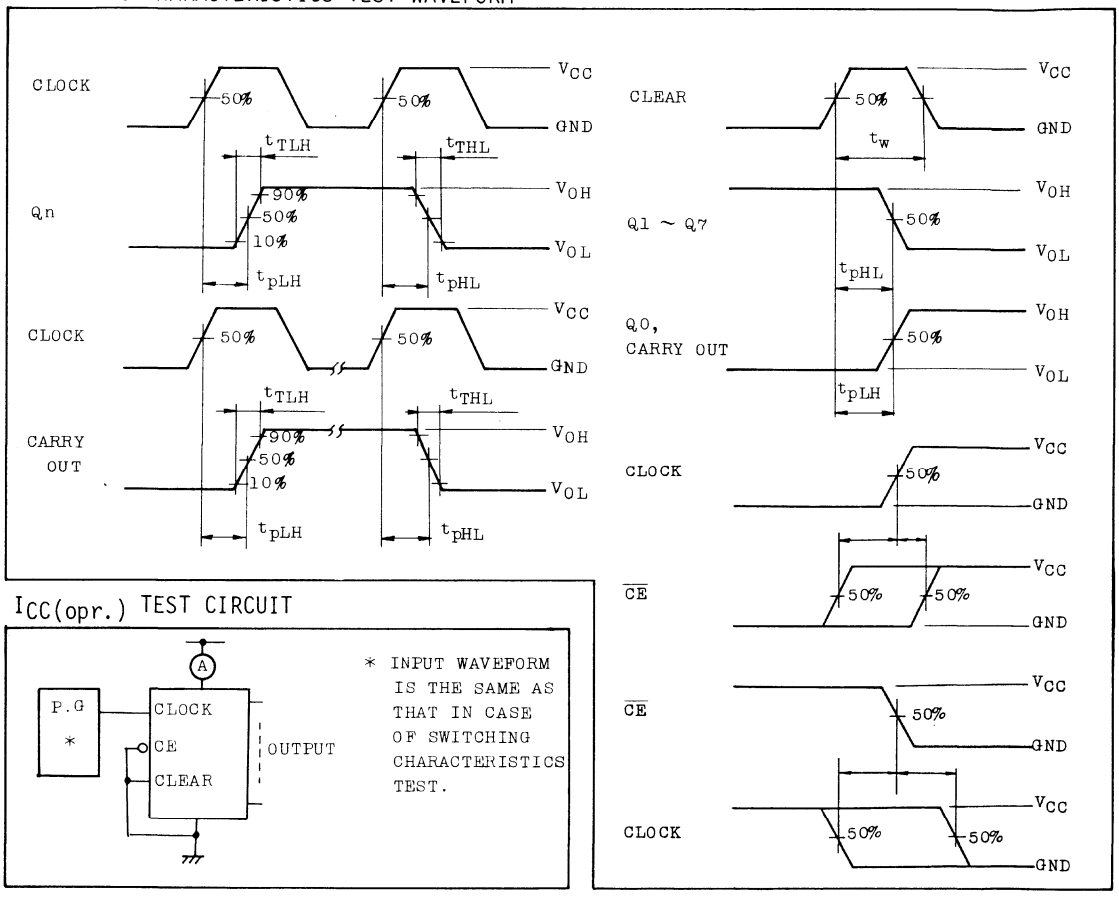
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Maximum Clock frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	40	-	20	-	
			6.0	29	47	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	52	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4022P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

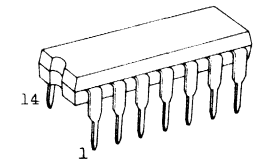
TC74HC4024P/F

TC74HC4024P/F 7-STAGE BINARY COUNTER

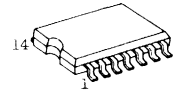
The TC74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C²MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4024B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the $\overline{\text{CLOCK}}$ input brings one increment to the counter. Seven kinds of divided output are provided; 1'st and 4 stage thru 7 stage. And at the last stage, 1/128 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 4024B.



DIP14(3D14A-P)



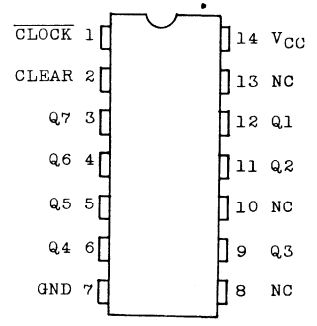
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

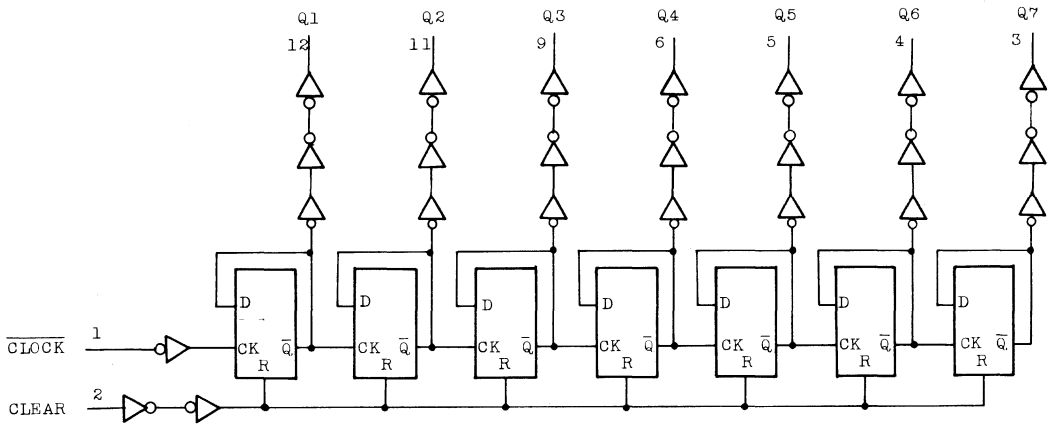
TC74HC4024P/F

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⌐‾	L	NO CHANGE
‾⌐	L	ADVANCE TO NEXT STATE

X : DON'T CARE

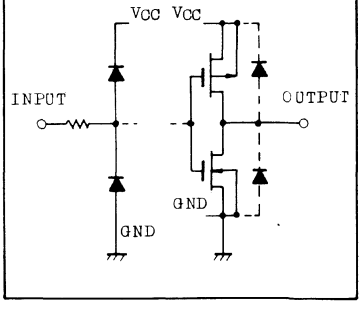
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4024P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
	t_{pHL}		6.0	-	15	25	-	31	
Propagation Delay Time (Qn - Qn+1)	t_{pLH}		2.0	-	28	60	-	75	
			4.5	-	7	12	-	15	
	t_{pHL}		6.0	-	6	10	-	13	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	

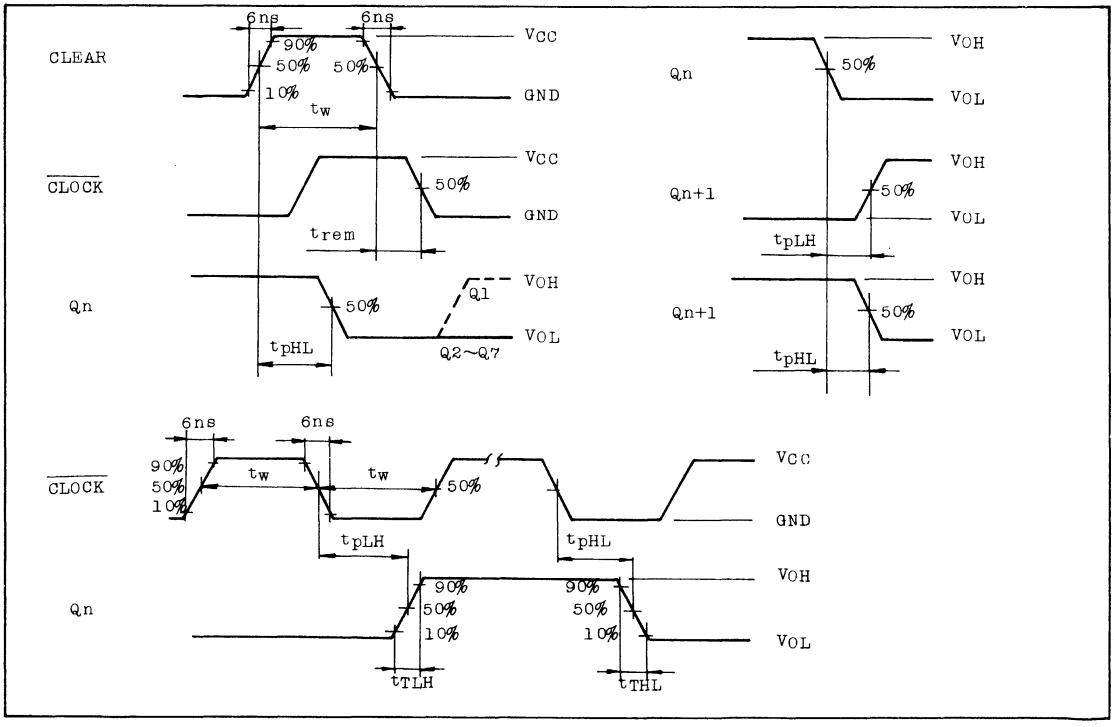
TC74HC4024P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

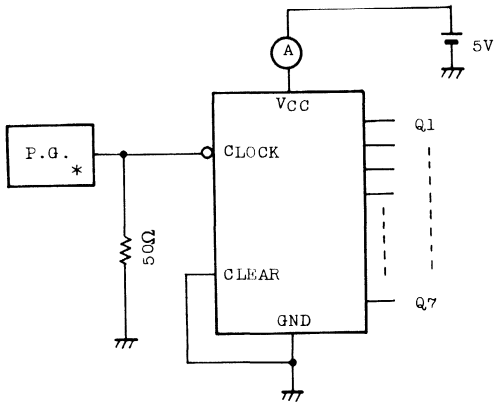
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	42	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4028P/F

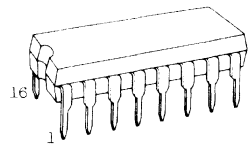
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4028P/F BCD-TO-DECIMAL DECODER

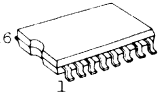
The TC74HC4028 is a high speed CMOS DECIMAL DECODER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
A BCD code applied to the four input (A thru D) provides a high level at the selected one of the decimal decoded outputs. A illegal BCD code such as eleven to fifteen gives a low level at all outputs.
The device also can be used as 3-to-8 LINE DECODER, when D input is assigned as a disable input.
The device is useful for code conversion, address decoding, memory selection, demultiplexing, or read out decoding.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=25ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays.....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range....$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4028B

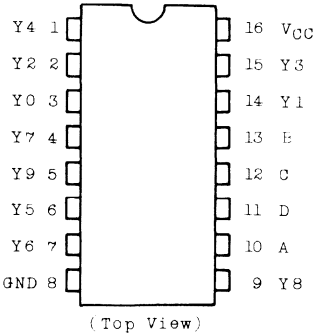


DIP16(3D16A-P)



MFP16(F16GC-P)

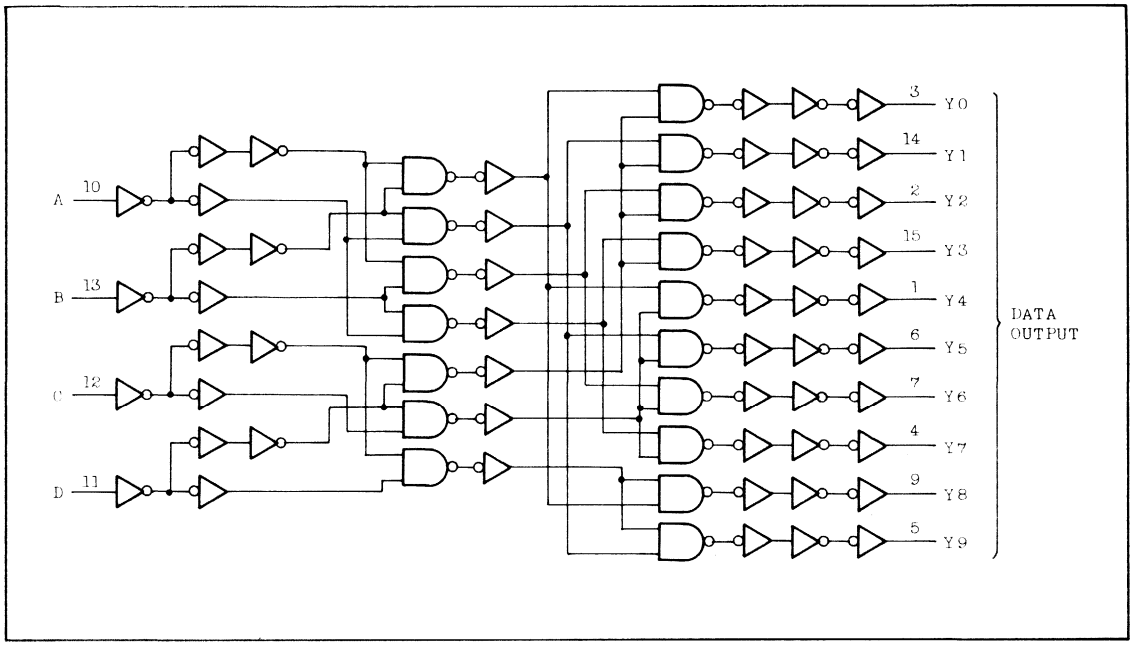
PIN ASSIGNMENT



(Top View)

TC74HC4028P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS										SELECTED OUTPUT
D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y_0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y_1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y_2
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y_3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y_4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y_5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y_6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y_7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y_8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y_9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

X : Don't care

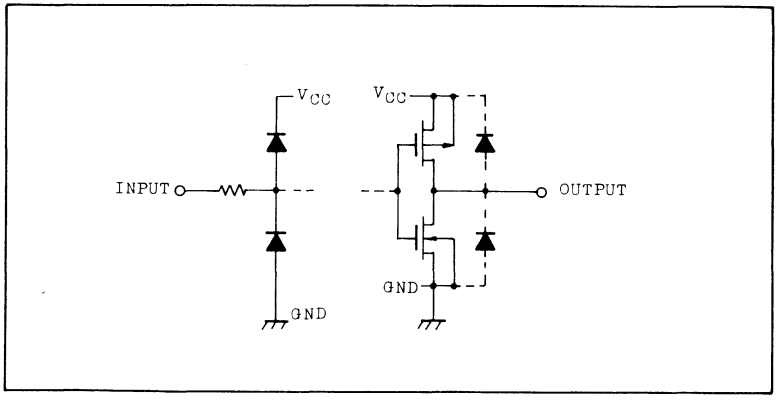
TC74HC4028P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC4028P/F

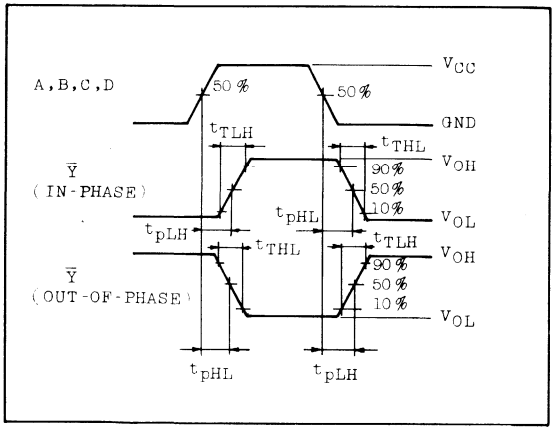
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A,B,C,D)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	58	-	-	-	

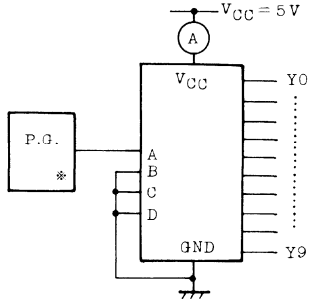
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



※ Input transition time is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4040P/F

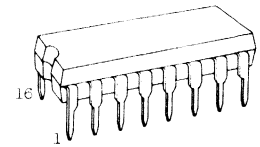
TC74HC4040P/F 12-STAGE BINARY COUNTER

GENERAL DESCRIPTION

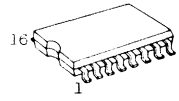
The TC74HC4040 is a high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4040B) with the same power dissipation.
A clear input is used to reset the counter to all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. All divided output stages are provided, and 1/4096 divided frequency will obtained at the last stage.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Functional Compatible with 4040B.



DIP16(3D16A-P)



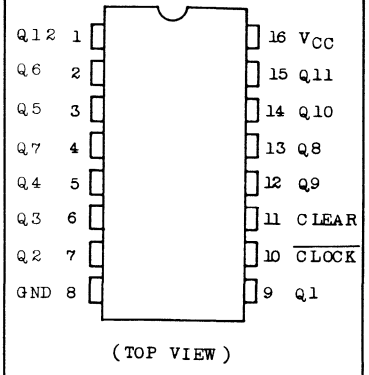
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

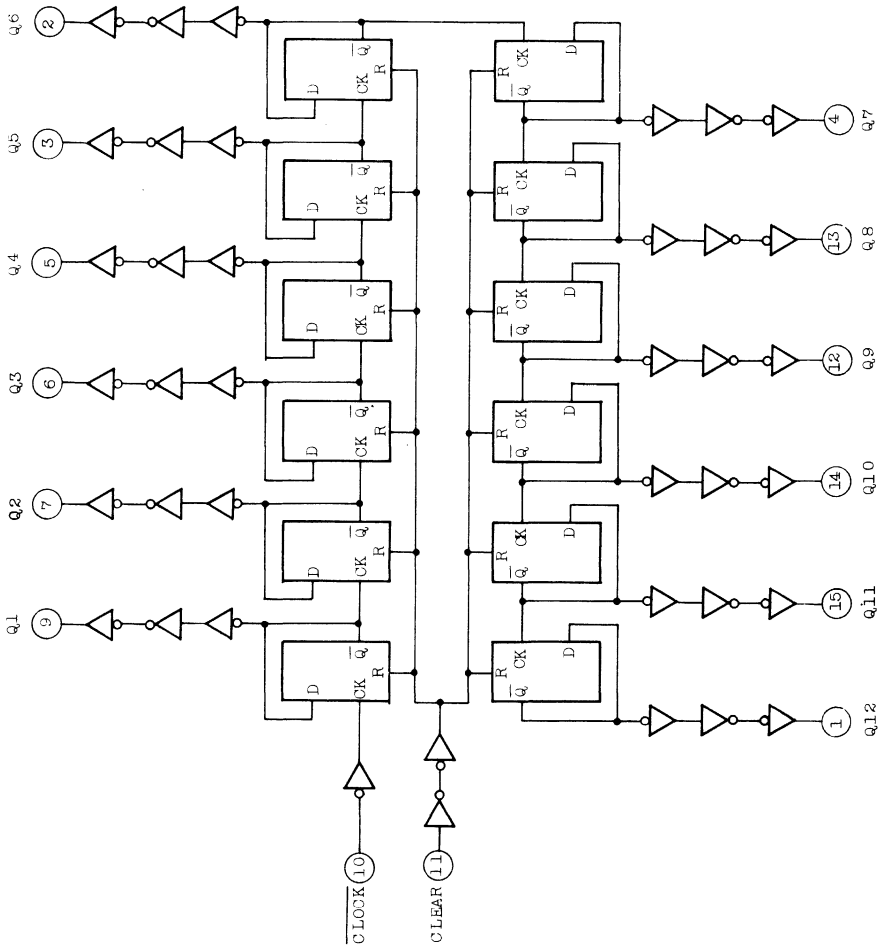
TC74HC4040P/F

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

X : DON'T CARE

LOGIC DIAGRAM

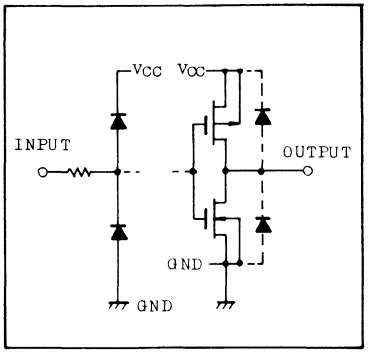


TC74HC4040P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC4040P/F

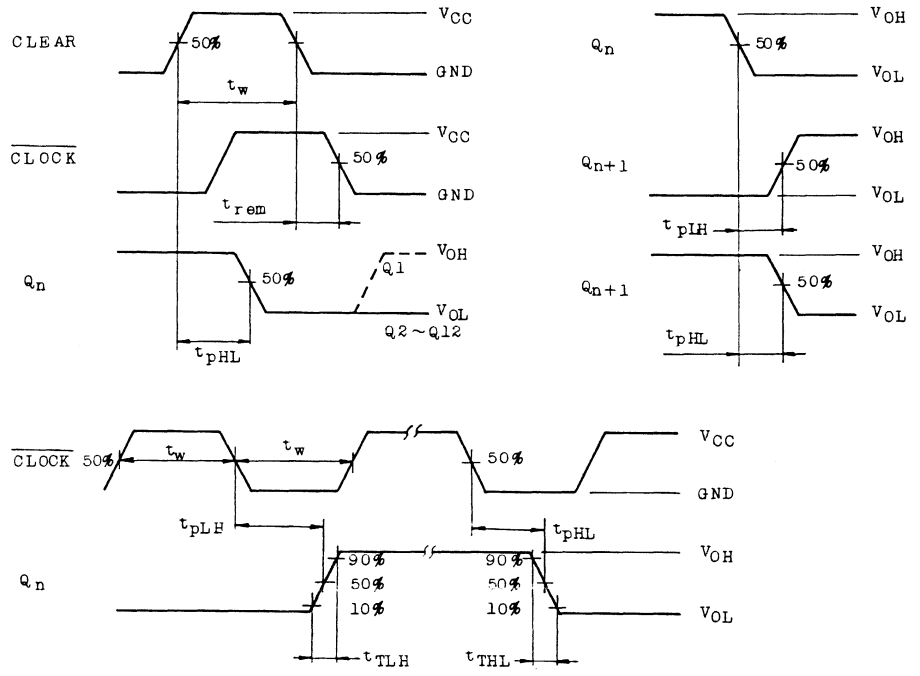
AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q_1)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time (Q_n - Q_{n+1})	t_{pLH} t_{pHL}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time (CLEAR)	t_{pHL}		2.0	-	104	205	-	225	
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	32	-	-	-	

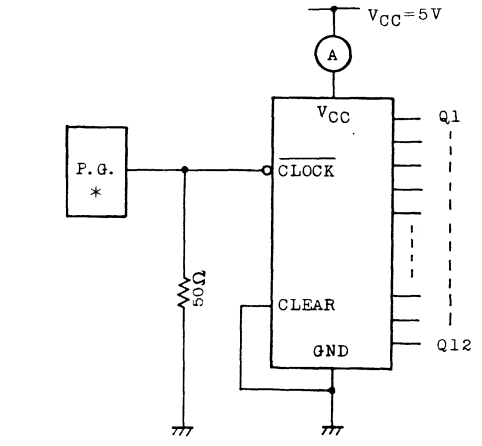
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4049P/F
TC74HC4050P/F

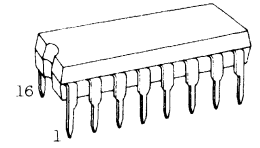
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4049 P/ F HEX BUFFER/CONVERTER (INVERTING)
TC74HC4050 P/ F HEX BUFFER CONVERTER

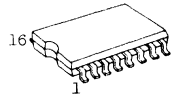
The TC74HC4049 and the TC74HC4050 are high speed CMOS HEX BUFFER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC4049 is an inverting buffer, while the TC74HC4050 is a non-inverting buffer.
The internal circuit is composed of 3-stage or 2-stage inverters, which enables high noise immunity and stable output.
Input protection circuits are different from those of the high speed CMOS IC's.
They eliminate diodes of V_{CC} side and enable logic-level conversion from high-level voltage (up to 8V) to low-level voltage.
These IC's are useful for battery back up circuits, because input voltage can be appled on IC's which is not biased by V_{CC}.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4049B, 4050B.



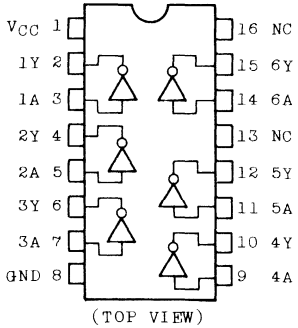
DIP16(3D16A-P)



MFP16(F16GC-P)

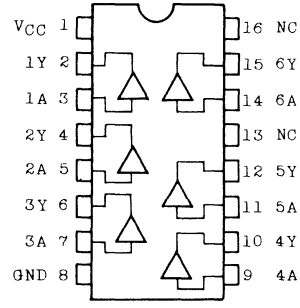
PIN ASSIGNMENT

TC74HC4049



(TOP VIEW)

TC74HC4050

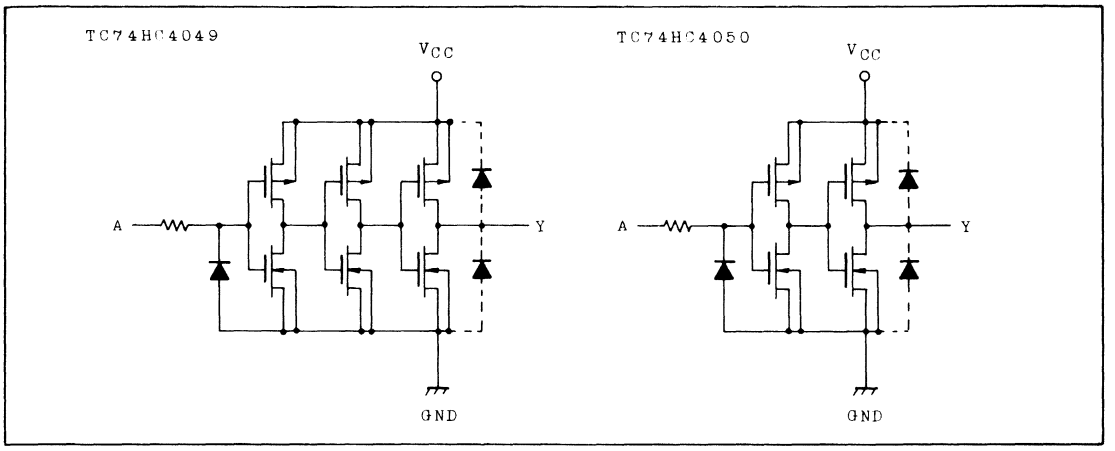


(TOP VIEW)

NC : No Connection

TC74HC4049P/F
TC74HC4050P/F

CIRCUIT SCHEMATIC (per Gate)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ 10*	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)**/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

Note.
*DC input voltage is able to impress -0.5V to 10V based on GND without any relation to voltage of V_{CC}. Recommended operating condition is from 0V to 8V and it is possible to vonvert logic-level from 8V to 5V or 5V to 2V.

**500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ 8	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

TC74HC4049P/F
TC74HC4050P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

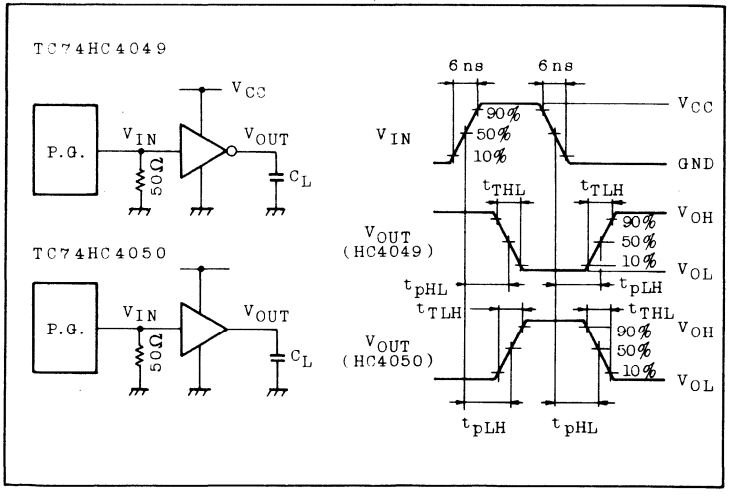
TC74HC4049P/F
TC74HC4050P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

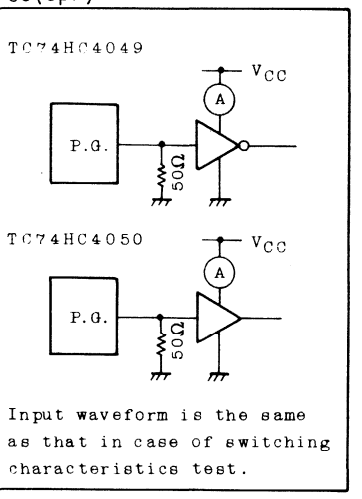
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC4060P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4060P/F 14-STAGE BINARY COUNTER/DIVIDER WITH OSCILLATOR

The TC74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It operates ten times as fast as that of metal-gate C^2MOS IC (4060BP) with the same power dissipation.

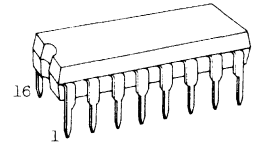
The oscillator configuration allows designs of either RC or crystal oscillator circuits. A clear input is used to reset the counter to the all low level state and disable the oscillator. A high level at CLEAR accomplishes the reset function.

A negative transition on the clock input incliments the counter. Ten kinds of devided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. And at the last stage, 1/16384 devided frequency is obtained.

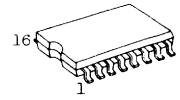
The $\overline{\phi}_I$ input and the CLEAR input are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed.....f_{max}=60MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.) (Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Oscillator Configulation .....RC or Crystal Oscillator
- Schmitt Trigger Clock Input
- Pin and Function Compatible with 4060B



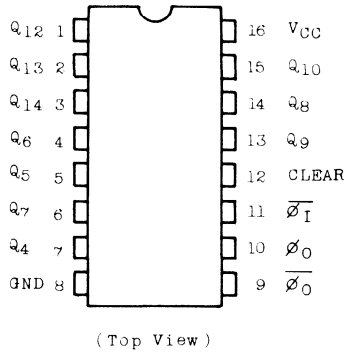
DIP16(3D16A-P)



MFP16(F16GC-P)

TC74HC4060P/F

PIN ASSIGNMENT



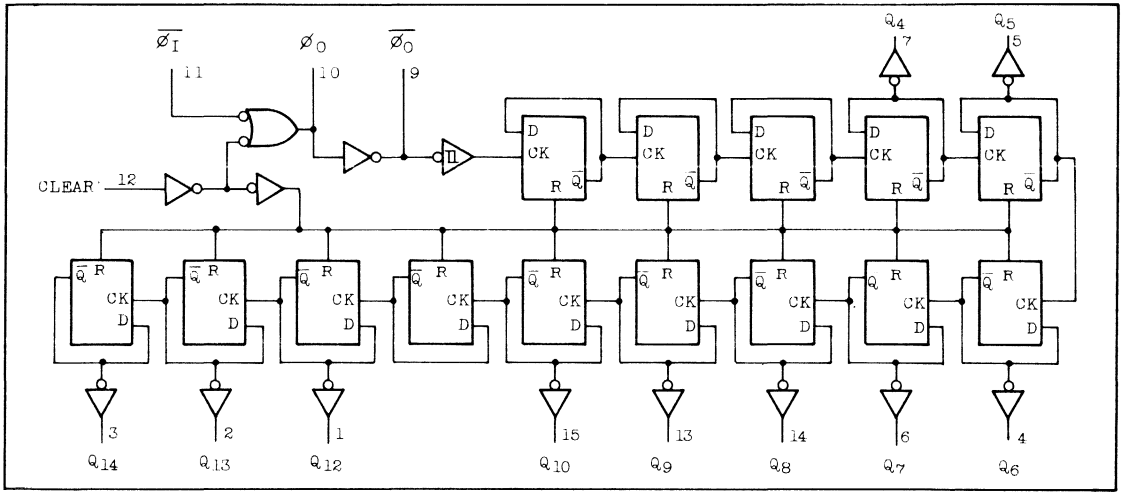
(Top View)

TRUTH TABLE

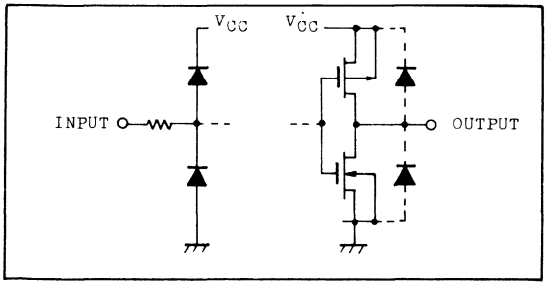
INPUTS		FUNCTION
$\overline{\phi}_I$	CLEAR	
x	H	Counter is reset to zero state. ϕ_0 output goes to high level $\overline{\phi}_0$ output goes to low level
↓	L	Count up one step.
↑	L	No change.

x Don't care

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4060P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q Outputs)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.8	2.0	-	1.8	-	V
				4.5	4.0	4.5	-	4.0	-	
				6.0	5.5	5.9	-	5.5	-	
Low-Level Output Voltage (Q Outputs)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Low-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.2	-	0.2	V
				4.5	-	0.0	0.5	-	0.5	
				6.0	-	0.1	0.5	-	0.5	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q Outputs)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time $\overline{\phi}_I$ - Q_4	t_{pLH} t_{pHL}		2.0	-	196	370	-	465	
			4.5	-	49	74	-	93	
			6.0	-	42	63	-	79	
Q_n - Q_{n+1}	t_{pLH} t_{pHL}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
CLEAR - Q_n	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	

TC74HC4060P/F

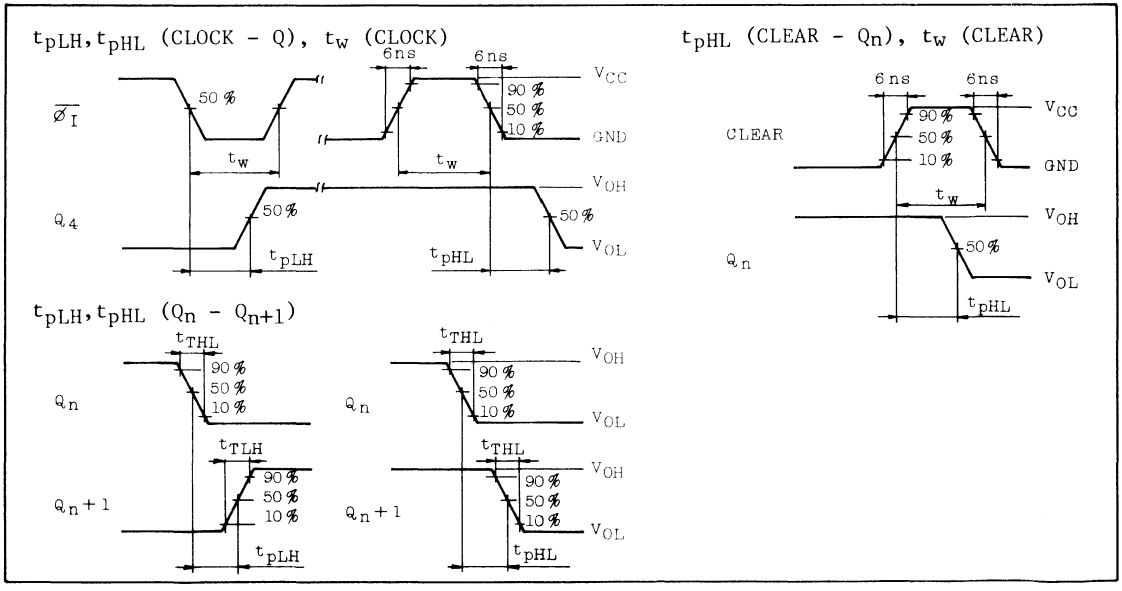
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns) (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width CLOCK ($\overline{\phi}_I$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
CLEAR	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time CLEAR	t_{rem}		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	33	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

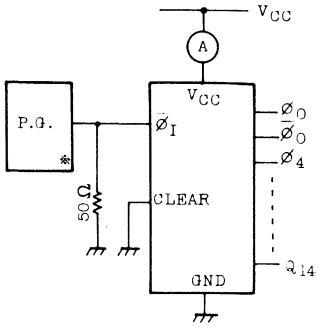
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC4060P/F

$I_{CC(opr)}$ TEST CIRCUIT



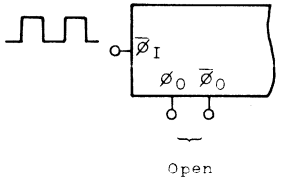
* $\overline{\phi}_I$ input $t_r=t_f=6ns$ Duty=50%

Note

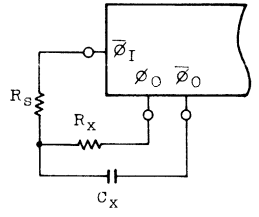
When CR or crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the measured value from the test circuit shown left, because these oscillion circuits spend much supply current.

TYPICAL CLOCK DRIVE CIRCUITS

EXTERNAL CLOCK DRIVE

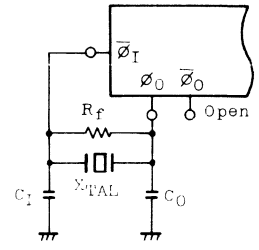


TYPICAL RC CIRCUIT



R_S : $2R_X \sim 10R_X$

TYPICAL CRYSTAL CIRCUIT



TC74HC4066P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4066P/F QUAD BILATERAL SWITCH

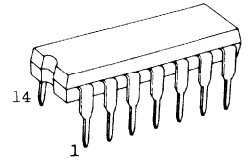
The TC74HC4066 is a high speed CMOS QUAD BILATERAL SWITCH fabricated with silicon gate C²MOS technology.

It consists of four independent high speed switches capable of controlling either digital or analog signals with as low power dissipation as that of metal-gate C²MOS IC.

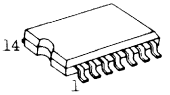
C input is provided to control the switch; the switch is ON while the C input is maintained at high level, and the switch is OFF while at low level.

FEATURES:

- High Speed.....t_{pd}=12ns(Typ.) (V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.) (Ta=25°C)
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Low ON Resistance.....R_{ON}=80Ω(Typ.) (V_{CC}=5V)
- High Degree of Liniarity.....DISTORTION=0.05%(Typ.) (V_{CC}=5V)
- Pin and Function Compatible with 4066B

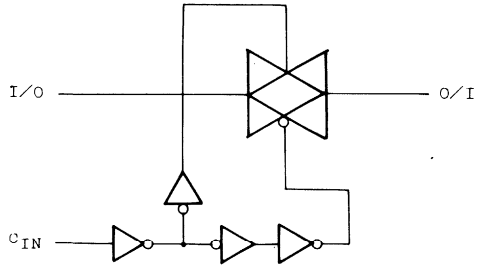


DIP14(3D14A-P)

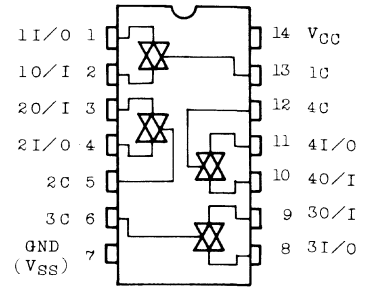


MFP14(F14GB-P)

LOGIC DIAGRAM (PER CHANNEL)



PIN ASSIGNMENT



(Top View)

TC74HC4066P/F

ABSOLUTE MAXIMUM RATINGS

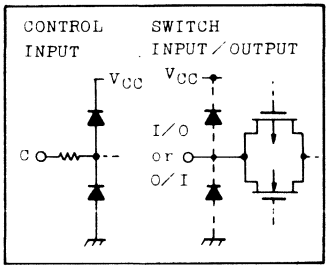
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Control Input Voltage	V_{IH}	Refer to R_{ON} specification	2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Control Input Voltage	V_{IL}	$\|I_{OFF}\| \leqq 1.0\mu A$	2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	
ON Resistance	R_{ON}	V_C=V_{IHC} $V_{I/O}$=0 ~ V_{CC} $I_{I/O}$=100μA	2.0	-	2000	-	-	-	Ω
			4.5	-	100	200	-	250	
			6.0	-	60	170	-	210	
Difference of ON Resistance Between Any Two of Four Switches	ΔR_{ON}	V_C=V_{IHC} $I_{I/O}$=100μA	2.0	-	50	-	-	-	
			4.5	-	3	-	-	-	
			6.0	-	2	-	-	-	

TC74HC4066P/F

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Input/Output Leakage Current (Switch OFF)	I_{OFF}	$V_C=V_{ILC}$ $V_{I/O}=6V$, $V_{O/I}=0V$ or $V_{I/O}=0V$, $V_{O/I}=6V$	6.0	-	-	±0.1	-	±0.1	μA
Input Leakage Current	I_{IN}		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

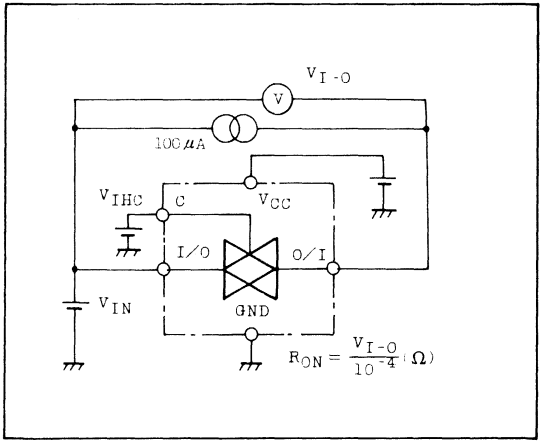
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Propagation Delay Time (Input to Output)	t_{pLH} t_{pHL}	R_L=10kΩ	2.0	-	13	50	-	65	ns
			4.5	-	5	10	-	13	
			6.0	-	4	9	-	11	
Output Enable Time	t_{pZH} t_{pZL}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	64	115	-	145	
			4.5	-	16	23	-	29	
			6.0	-	14	20	-	25	
Sine Wave Distortion		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=10kΩ f=1kHz	2.5	-	0.05	-	-	-	%
Frequency Response (Switch ON) $20\log_{10}\frac{V_{out}}{V_{in}}$=-3dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	30	-	-	-	MHz
Feedthrough Attenuation (Switch OFF) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	1.0	-	-	-	
Crosstalk (Control Input to Signal Output)		R_{IN}=1kΩ R_L=10kΩ	2.0	-	25	-	-	-	mV
			4.5	-	60	-	-	-	
			6.0	-	75	-	-	-	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input tr=tf=6ns) (CONTINUED)

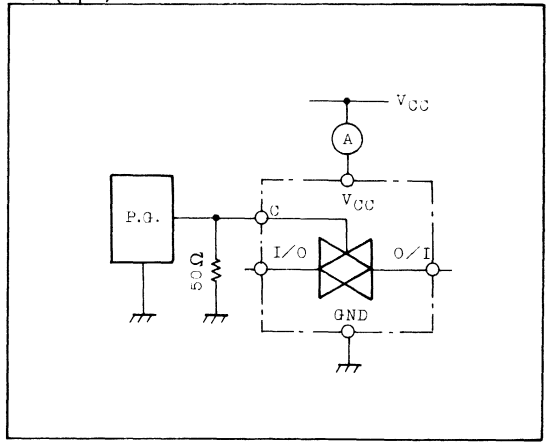
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Cross talk (Between any two switches) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V, V_{in}=0.88VRMS, R_L=1kΩ	2.5	-	1.5	-	-	-	MHz
Maximum Control Input Frequency		R_L=1kΩ, C_L=15pF, V_{OUT}=1/2 V_{CC}	2.0	-	20	-	-	-	MHz
			4.5	-	30	-	-	-	MHz
			6.0	-	30	-	-	-	MHz
Control Input Capacitance	C_{IN}			-	5	10	-	10	pF
Switch Input/Output Capacitance	$C_{I/O}$			-	6	-	-	-	pF
Feedthrough Capacitance	C_{I-O}			-	0.5	-	-	-	pF
Power Dissipation Capacitance	C_{PD}(1)			-	13	-	-	-	pF

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per CHANNEL)

CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



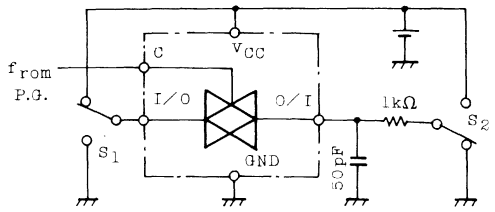
$I_{CC(opr)}$ TEST CIRCUIT

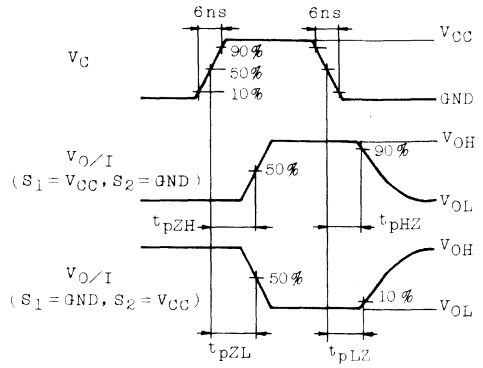


TC74HC4066P/F

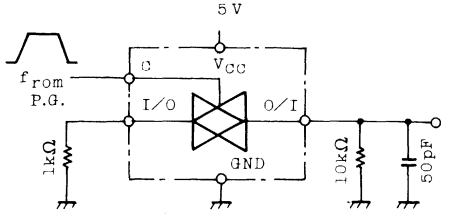
SWITCHING CHARACTERISTICS TEST CIRCUIT

1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

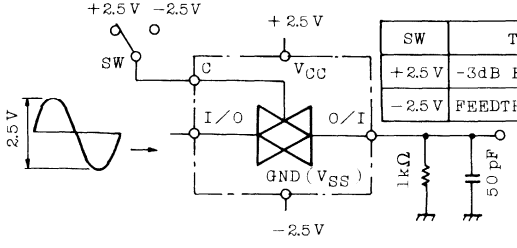




2. CROSSTALK (CONTROL TO OUTPUT)

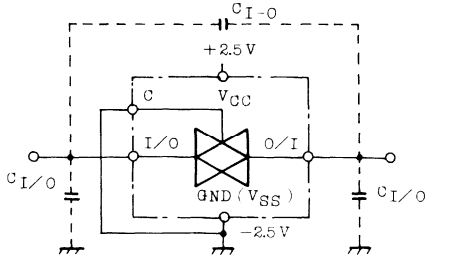


3. BANDWIDTH AND FEEDTHROUGH ATTENUATION

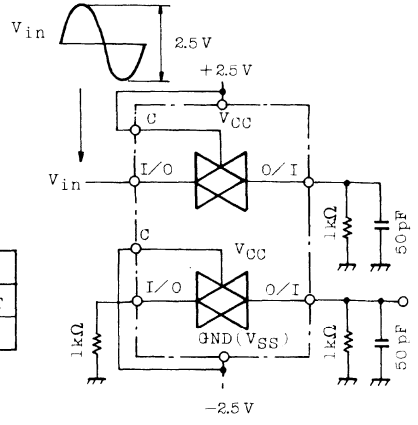


SW	TEST ITEM
+2.5 V	-3dB BANDWIDTH TEST
−2.5 V	FEEDTHROUGH TEST

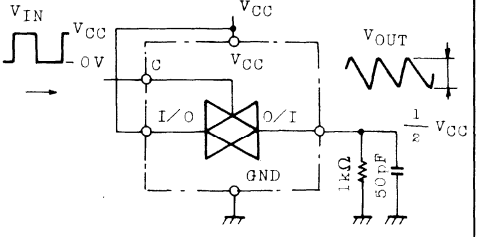
4. C_{I-O}, $C_{I/O}$



5. CROSSTALK BETWEEN ANY TWO SWITCHES



6. MAXIMUM CONTROL FREQUENCY



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4072P/F

TC74HC4072P/F DUAL 4-INPUT OR GATE

The TC74HC4072 is a high speed CMOS 4-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

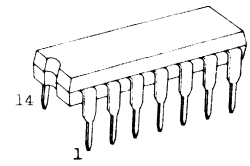
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output.

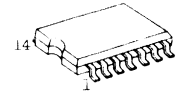
All inputs are equipped with protection circuits against static discharge or excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance...|I_{OH}|=I_{OL}=4mA(Min.)
- Balanced Propagation Delays....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range...V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 4072B

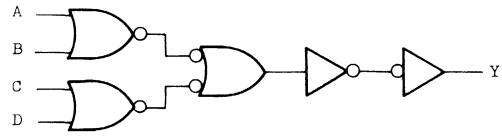


DIP14(3D14A-P)

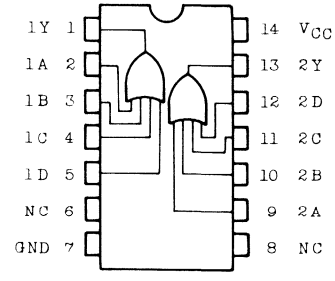


MFP14(F14GB-P)

LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)



PIN ASSIGNMENT



(Top View)

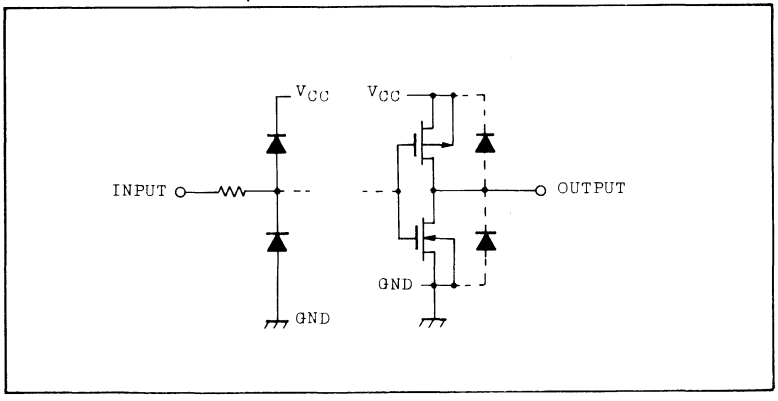
TC74HC4072P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40 ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

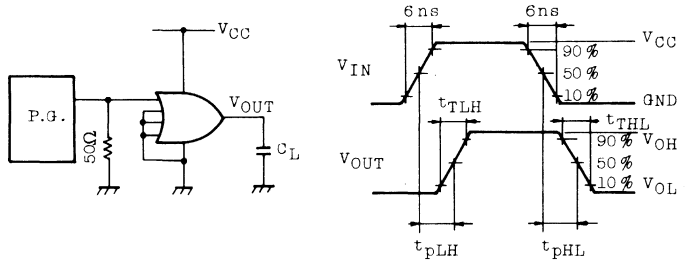
TC74HC4072P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

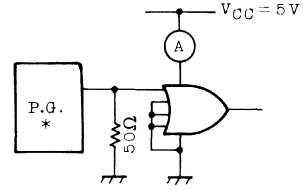
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT and WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



*Input waveform is the same as that in case of switching characteristics test.

TC74HC4075P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4075P/F TRIPLE 3-INPUT OR GATE

The TC74HC4075 is a high speed CMOS 3- INPUT OR GATE fabricated with silicon gate C^2MOS technology.

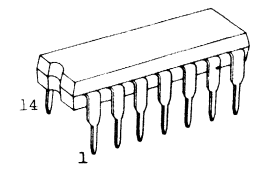
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

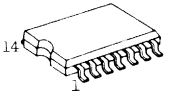
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}= 9 ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 4075B



DIP14(3D14A-P)



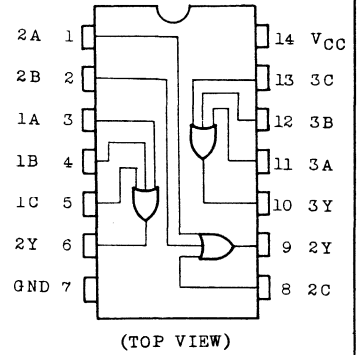
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

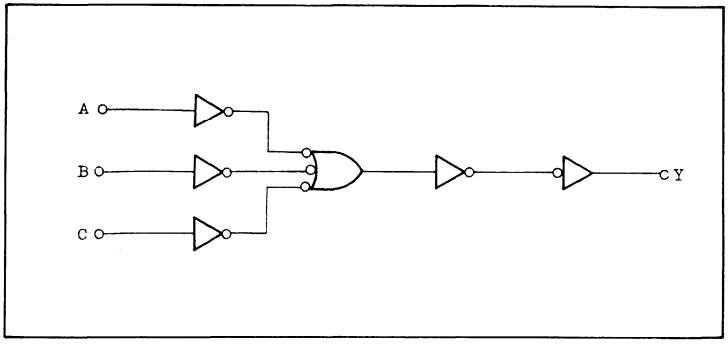
PIN ASSIGNMENT



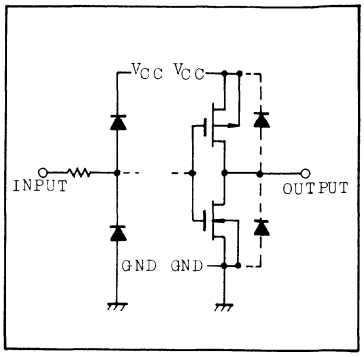
(TOP VIEW)

TC74HC4075P/F

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISITCS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH} t_{PHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	30	-	-	-	

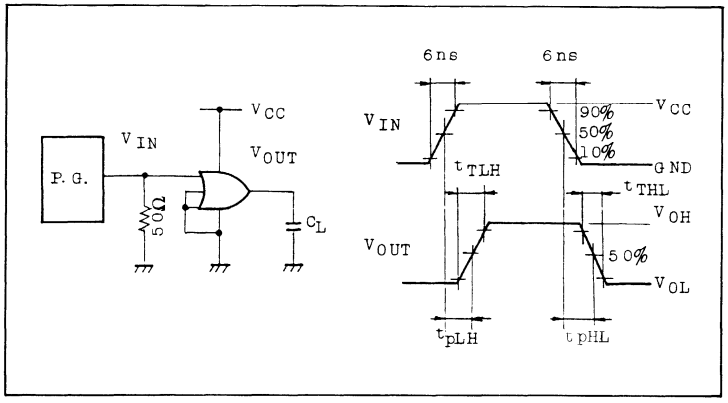
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

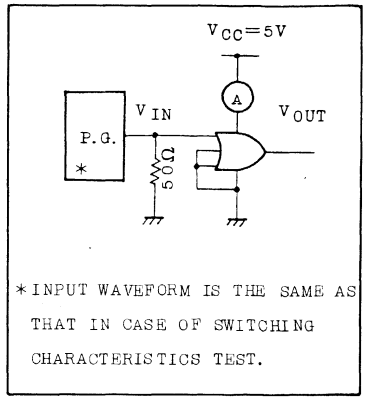
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3 \quad \text{(per gate)}$$

TC74HC4075P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4078P/F

TC74HC4078P/F 8-INPUT NOR GATE

The TC74HC4078 is a high speed CMOS 8-INPUT NOR GATE fabricated with silicon gate C²MOS technology.

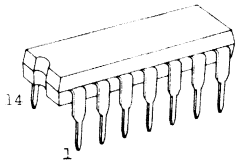
It operates ten times as fast as that of metal-gate C²MOS IC (4078B) with the same power dissipation.

Output X is 8-INPUT NOR, output Y is 8-INPUT OR. Both outputs are buffered, which enables high noise immunity and stable output.

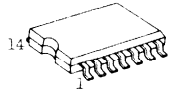
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4078B



DIP14(3D14A-P)



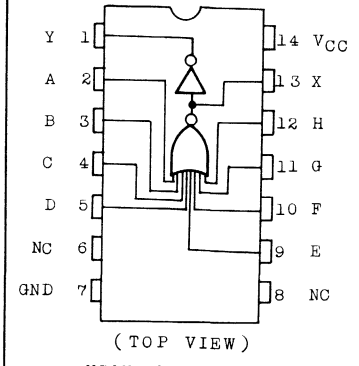
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

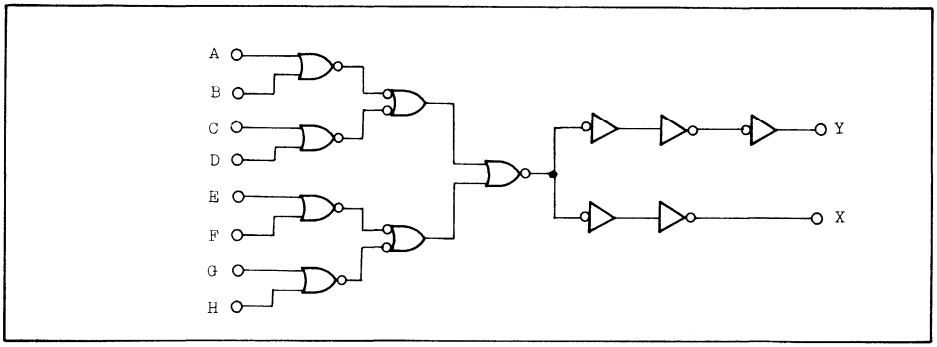


(TOP VIEW)

NC:No Connection

TC74HC4078P/F

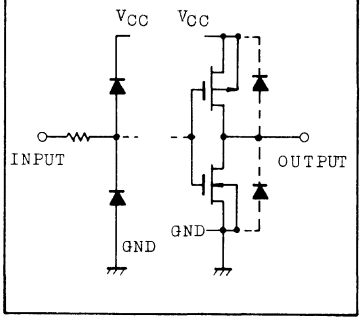
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	58	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	73	-	-	-	

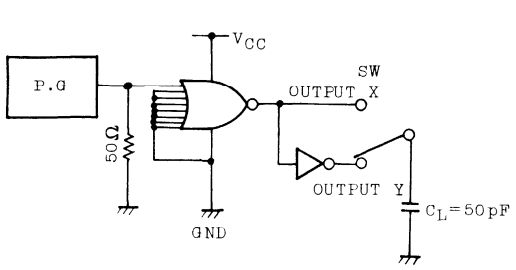
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

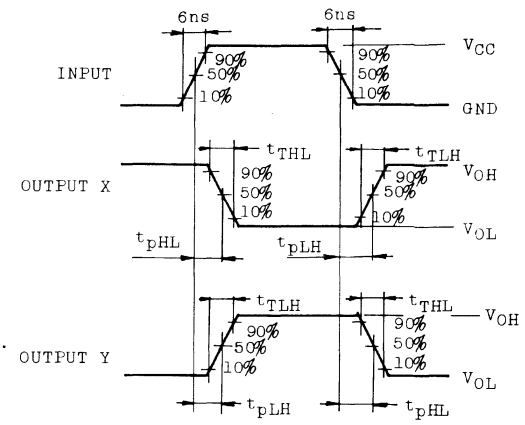
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

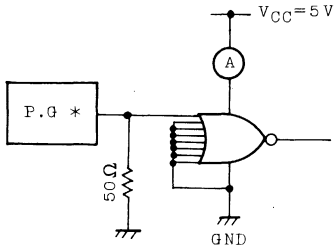
TC74HC4078P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT





$I_{CC(Opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

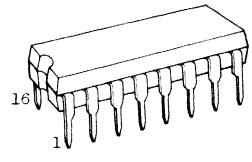
TC74HC4094P/F

TC74HC4094P/F 8-BIT SHIFT AND STORE REGISTER (3-STATE)

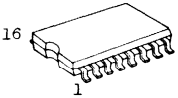
The TC74HC4094 is a high speed CMOS 8-STAGE SHIFT-AND-STORE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device consists of an 8-bit shift register and a 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices. Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided to a latch, which latches data on the negative going transition of the STROBE input signal. When STROBE input is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=42MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Oerating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4094B



DIP16(3D16A-P)



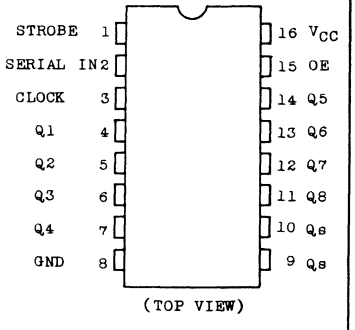
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

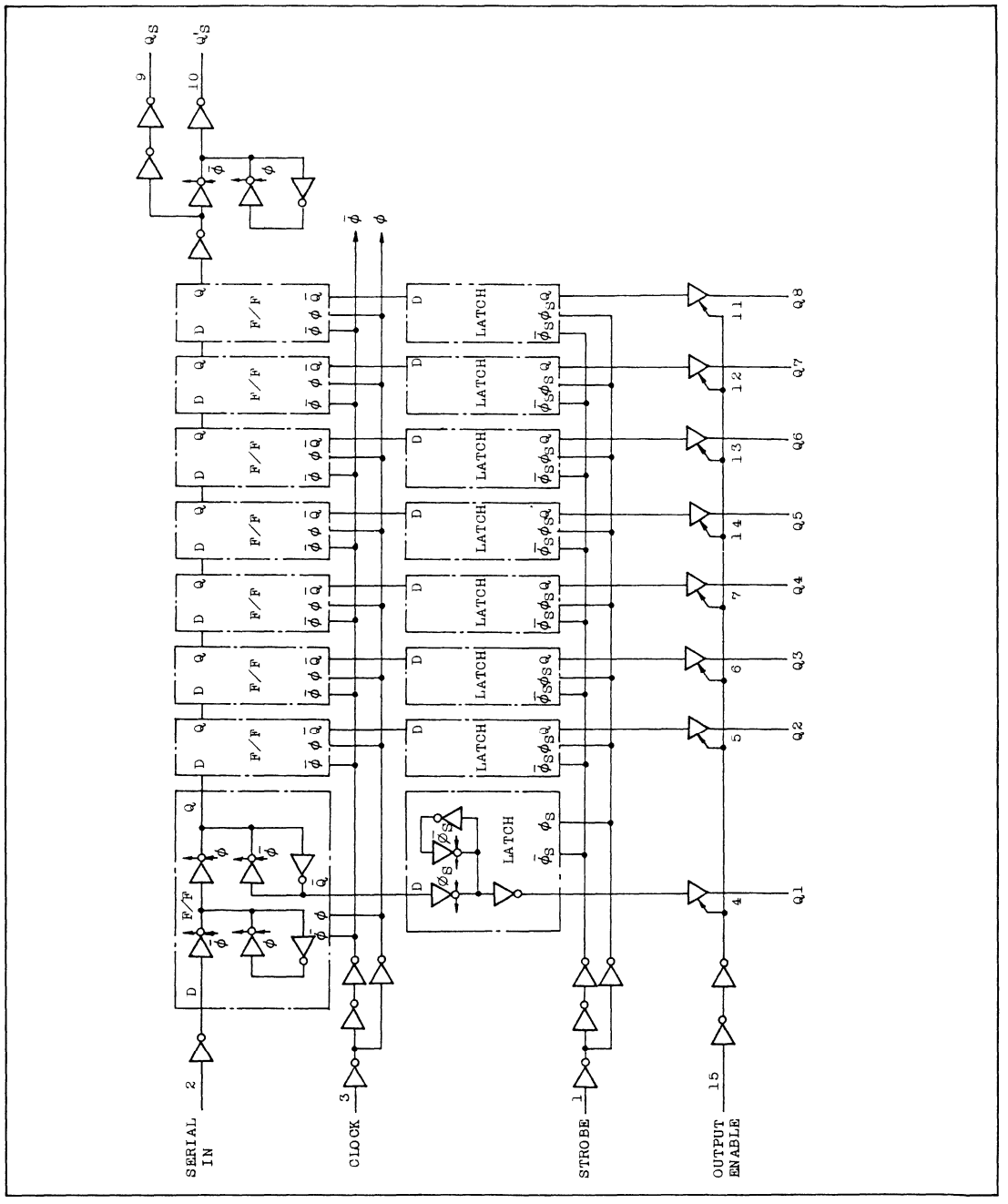
* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

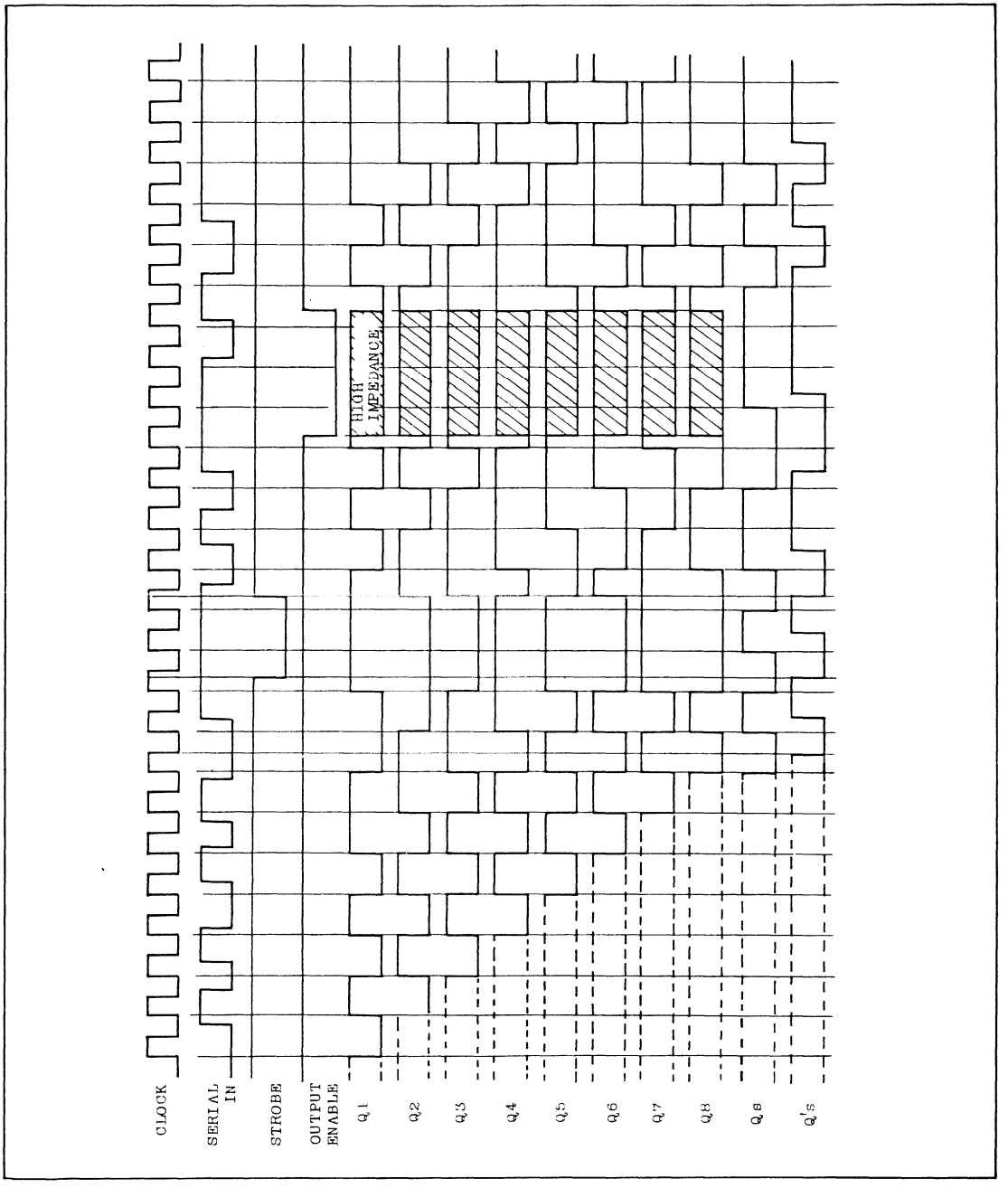


TC74HC4094P/F

LOGIC DIAGRAM



TIMING CHART



TC74HC4094P/F

TRUTH TABLE

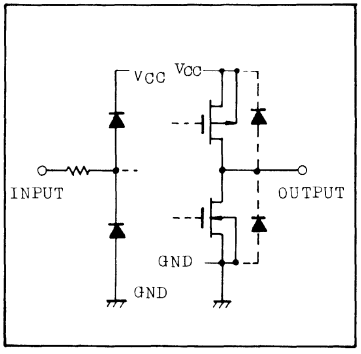
CK	OE	ST	SI	PARA.OUT		SERI.OUT	
				Q_1	Q_n	Q_s	Q_s
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Q_s
↓	L	X	X	Z	Z	NC	Q_s

X : DON'T CARE
NC: NO CHANGE
Z : HIGH IMPEDANCE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn)	t_{PLH}		2.0	-	140	270	-	340	
			4.5	-	35	54	-	68	
	t_{PHL}		6.0	-	30	46	-	58	
Propagation Delay Time (CLOCK - Qs, Qs')	t_{PLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
	t_{PHL}		6.0	-	22	34	-	43	
Propagation Delay Time (STROBE - Qn)	t_{PLH}		2.0	-	135	210	-	265	
			4.5	-	27	42	-	53	
	t_{PHL}		6.0	-	23	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	4	10	-	3	-	MHz
			4.5	20	38	-	16	-	
			6.0	24	45	-	19	-	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	ns
			4.5	-	9	20	-	25	
	$t_{w(L)}$		6.0	-	8	17	-	21	
Minimum Strobe Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	

TC74HC4094P/F

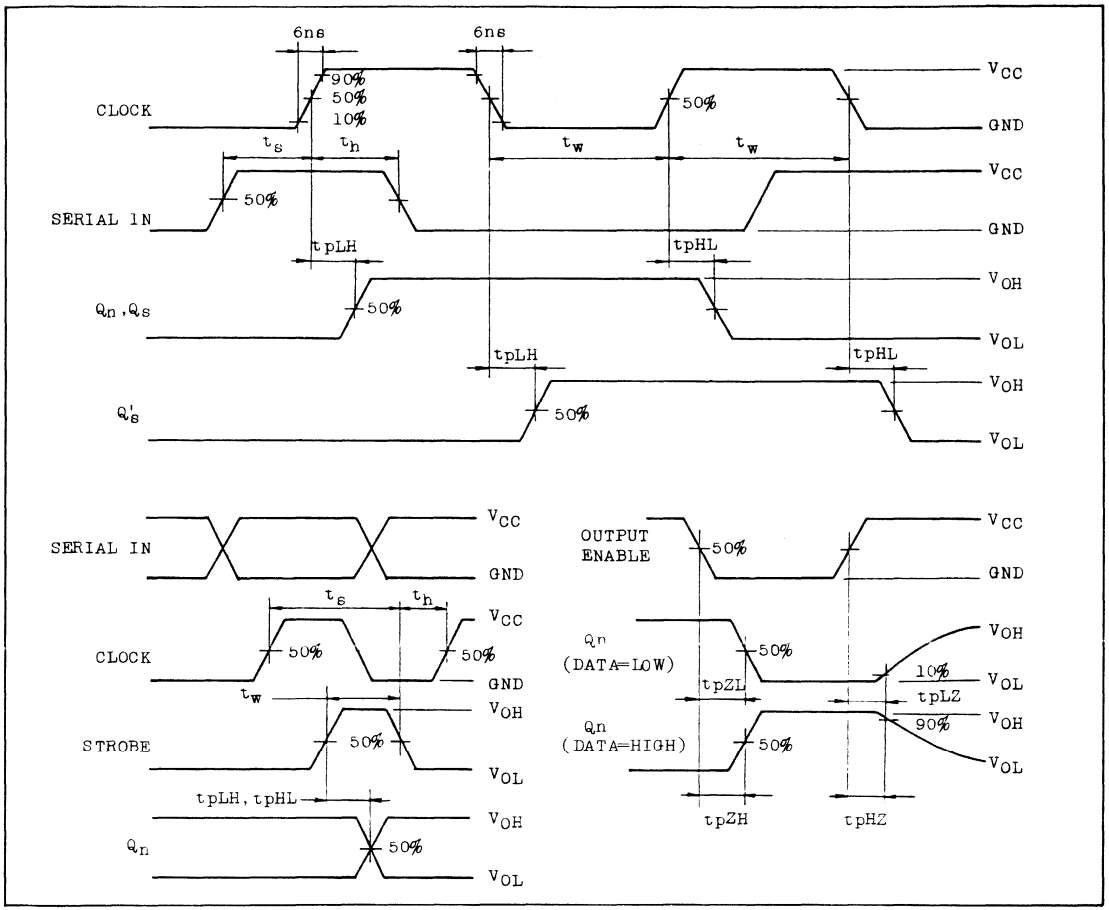
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Minimum Serial In Set-up Time	t_s		2.0	-	25	75	-	95	ns
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Strobe Set-up Time	t_s		2.0	-	50	150	-	190	
			4.5	-	13	30	-	38	
			6.0	-	11	26	-	33	
Minimum Serial In Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Strobe Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD} (1)			-	167	-	-	-	

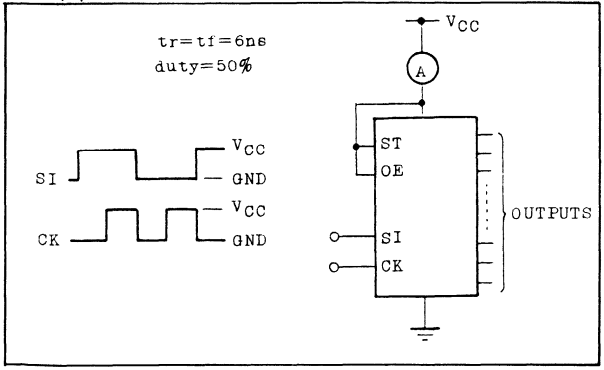
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC40102P
TC74HC40103P

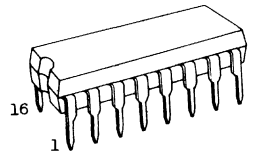
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC40102P DUAL BCD PROGRAMMABLE DOWN COUNTER
TC74HC40103P 8-BIT BINARY PROGRAMMABLE DOWN COUNTER

The TC74HC40102 and TC74HC40103 are high speed CMOS PROGRAMMABLE DOWN COUNTER fabricated with silicon gate C^2MOS technology.
They operate ten times as fast as that of metal-gate C^2MOS IC (40102/40103B) with the same power dissipation. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero. As the TC74HC40102 adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The 74HC40103 with 8-bits binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{CLR}$ control input setting counter to maximum counting mode.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range .....V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 40102B, 40103B



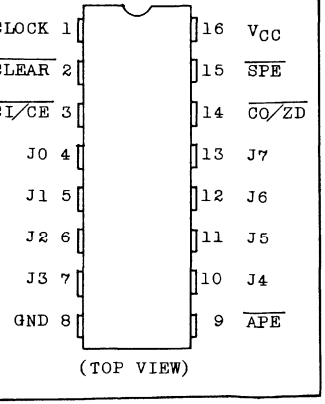
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC40102P
TC74HC40103P

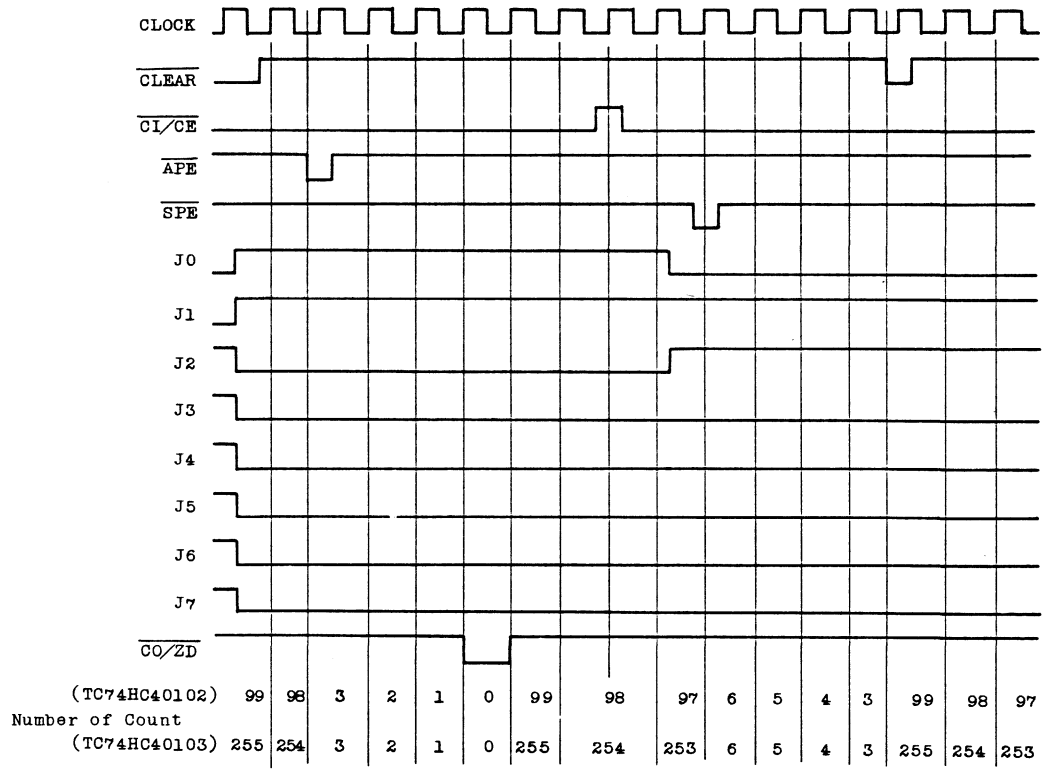
TRUTH TABLE

CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	X	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	X	X	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	X	X	X	Clear	Counter is set to maximum count.

Note 1. X: Don't care

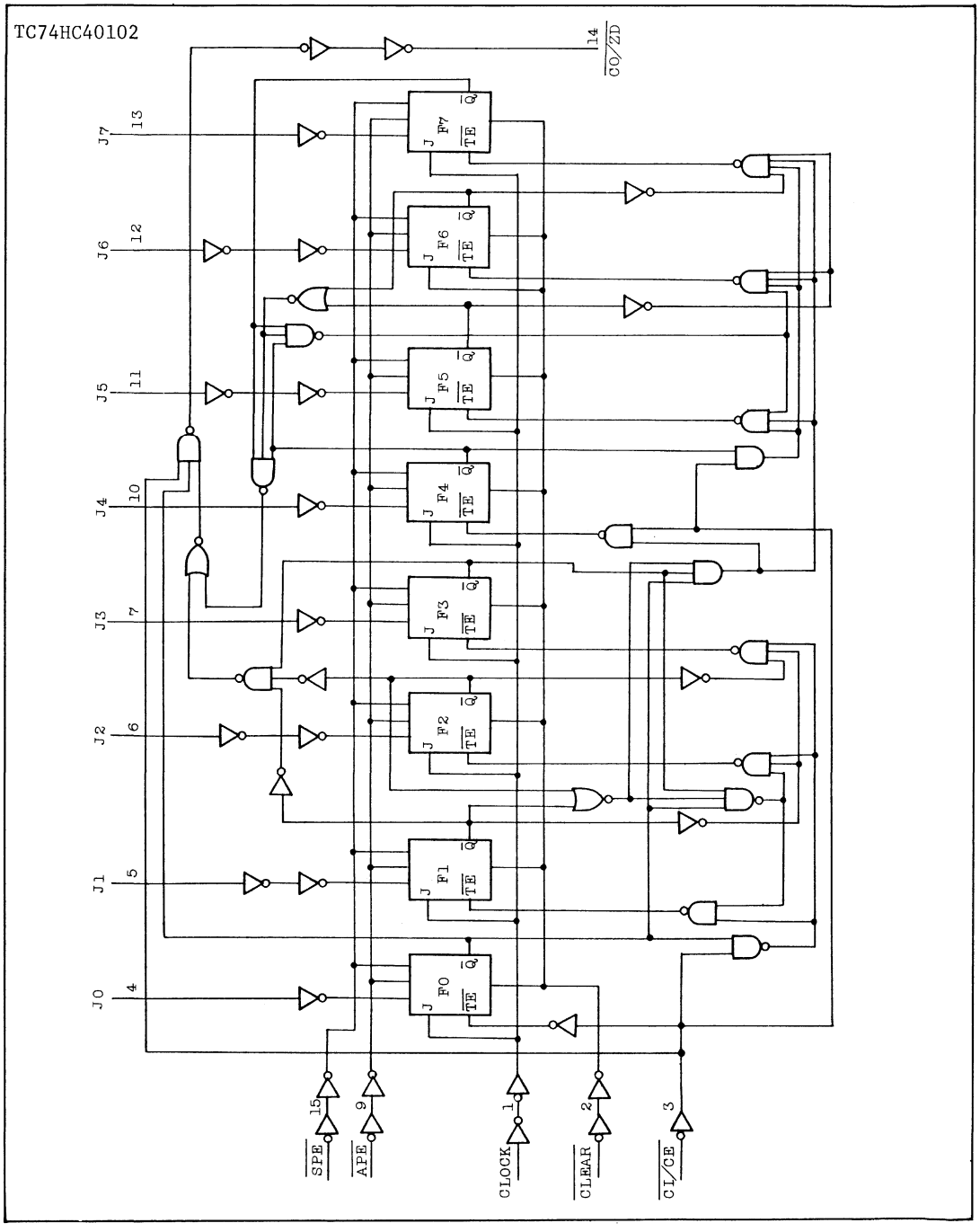
2. Maximum count: "99" for TC74HC40102 and "255" for TC74HC40103.

TIMING CHART



TC74HC40102P
TC74HC40103P

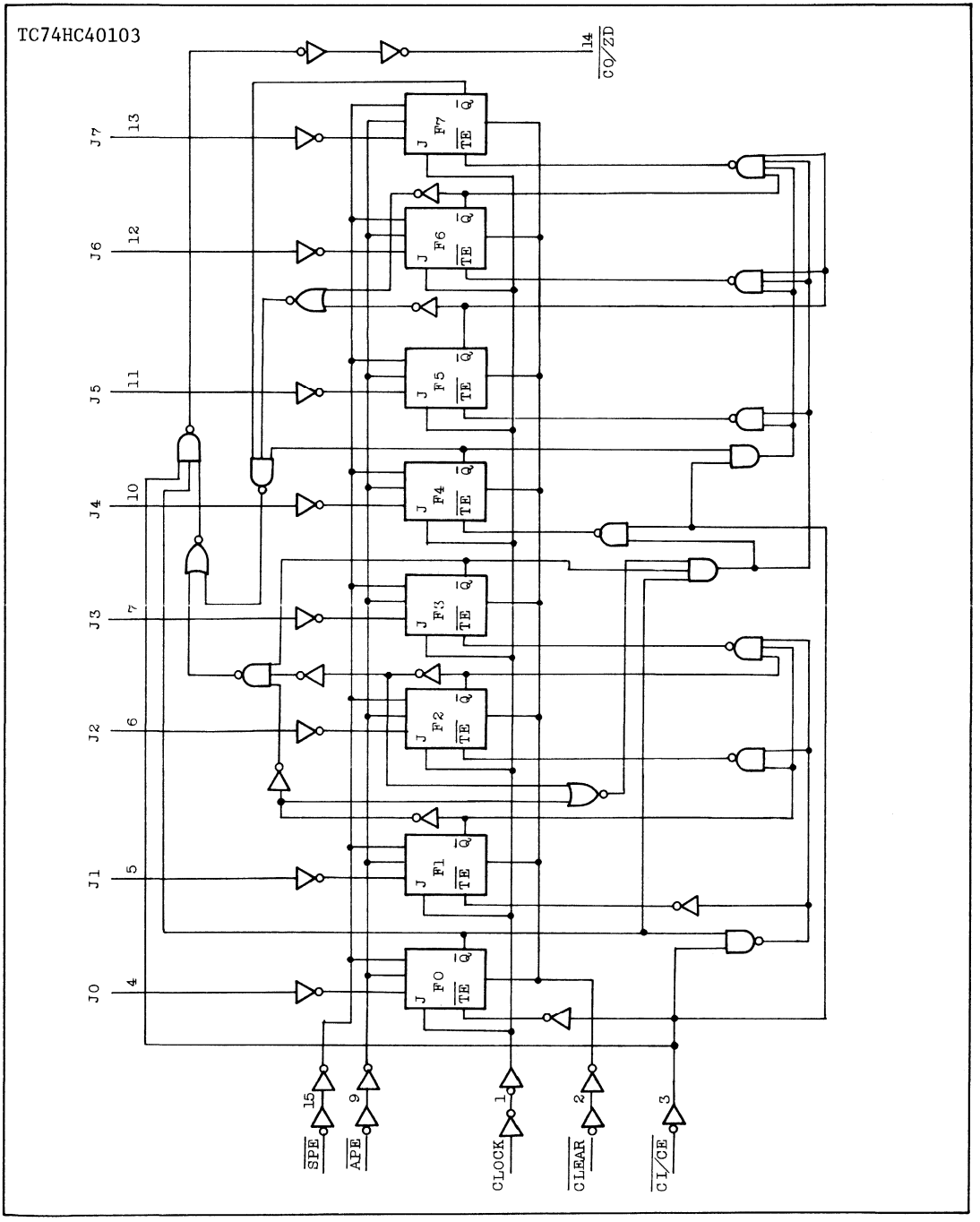
LOGIC DIAGRAM



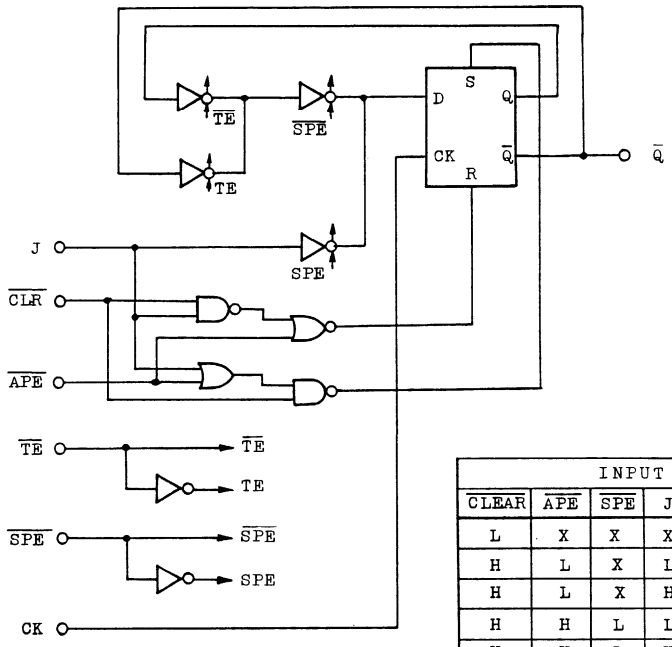
TC74HC40102P
TC74HC40103P

LOGIC DIAGRAM

TC74HC40103



TC74HC40102P
TC74HC40103P



INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q_n}+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↓	L
H	H	L	H	X	↓	H
H	H	L	X	X	↑	$\overline{Q_n}$
H	H	H	X	L	↓	Q_n
H	H	H	X	H	X	$\overline{Q_n}$

FUNCTIONAL DESCRIPTION

The TC74HC40102 and TC74HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103 adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level.

(Continued)

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102 and 255 for the TC74HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102 and TC74HC40103, respectively, when clock input alone is given without various kinds of preset operations.

PRESET OPERATION AND RESET OPERATION

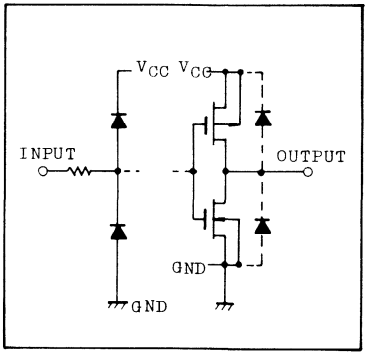
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC40102P
TC74HC40103P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	128	245	-	305	
	t_{pHL}		4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	156	300	-	375	
	t_{pHL}		4.5	-	39	60	-	75	
			6.0	-	33	51	-	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CLEAR}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	124	240	-	300	ns
			4.5	-	31	48	-	60	
			6.0	-	27	41	-	51	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	31	-	16	-	
			6.0	24	36	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$, $\overline{APE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$, $\overline{APE}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set up Time ($\overline{SPE}$ - CK)	t_s		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Set up Time ($\overline{CI/CE}$ - CK)	t_s		2.0	-	56	125	-	160	
			4.5	-	14	25	-	32	
			6.0	-	12	21	-	27	
Minimum Set up Time (Jn - CK)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set up Time (Jn - $\overline{APE}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (All Inputs)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	74HC40102		-	110	-	-	-	
		74HC40103		-	128	-	-	-	

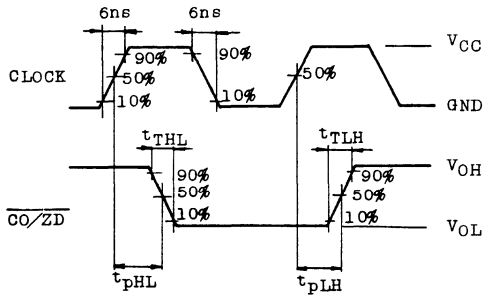
TC74HC40102P
TC74HC40103P

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

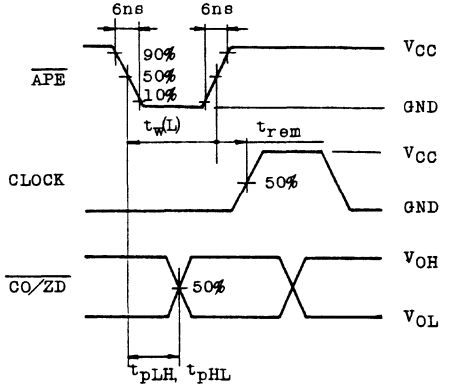
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

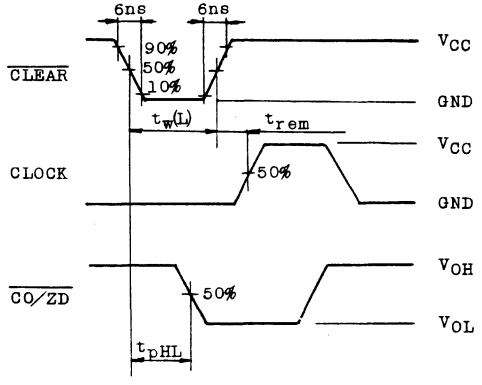
WAVEFORM 1



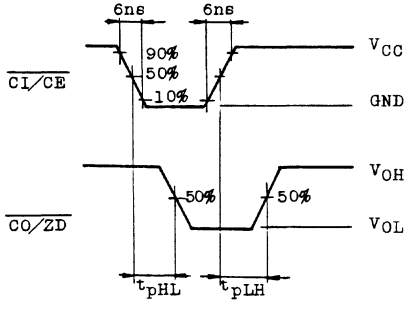
WAVEFORM 2



WAVEFORM 3

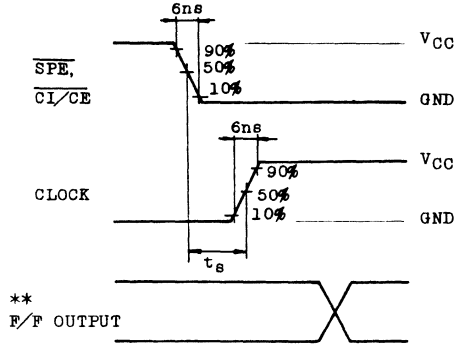


WAVEFORM 4

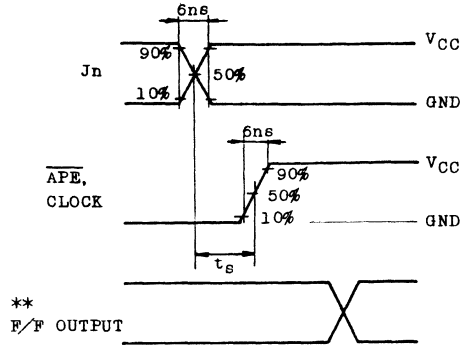


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

WAVEFORM 5

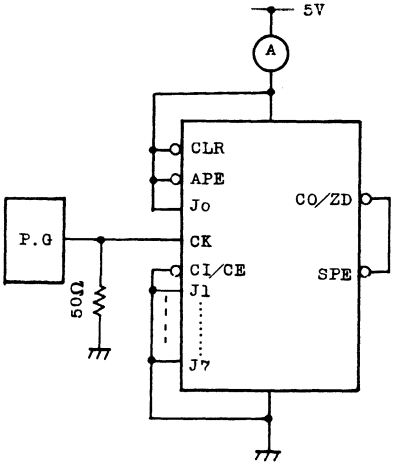


WAVEFORM 6



(** F/F output is internal signal of IC)

I_{CC}(Opr.) TEST CIRCUIT

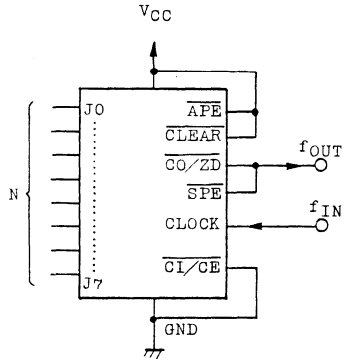


Input transition time is the same as that in case of switching characteristics test.

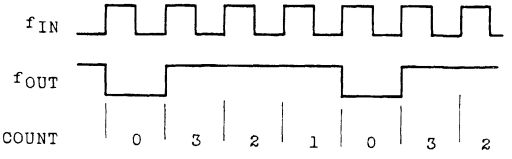
TC74HC40102P
TC74HC40103P

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

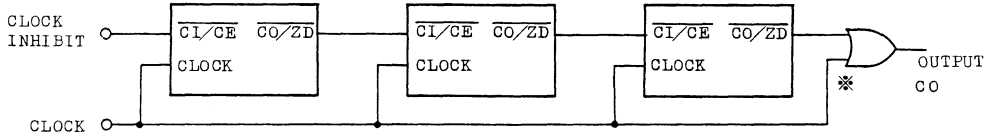


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (J0, J1=V_{CC}, J2 ∿ J7=GND)



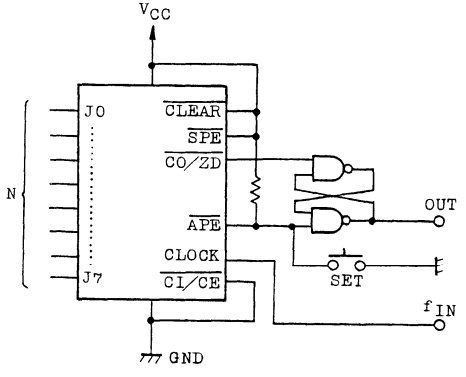
- TC74HC40102P .... 1/2 to 1/100 are dividable.
- TC74HC40103P .... 1/2 to 1/256 are dividable.

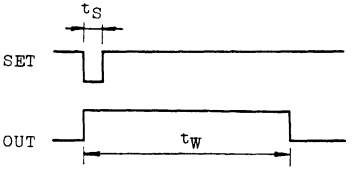
PARALLEL CARRY CASCADING



※ At synchronous cascade connection, huzzerd occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC74HC32 or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ∿ the above formula.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4511P/F

TC74HC4511P/F BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

The TC74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fablicated with silicon gate C²MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

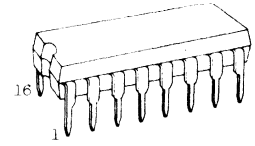
The segment output driver, which is CMOS construction, has large I_{OH} capability which enables to drive cathode common LED directly.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L". These functions are regardless of other inputs and used to test display.

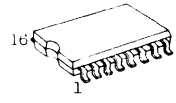
BI input is used to pulse-modulate the brightness of the display.

When error input code (over 10) is applied to BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

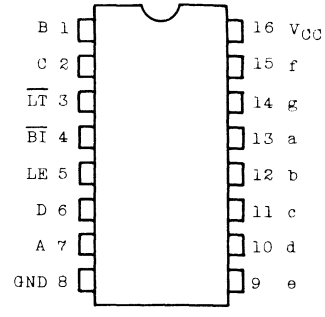


MFP16(F16GC-P)

FEATURES:

- High Speed.....t_w=15ns(Max.) at V_{CC}=4.5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTTL Loads
- High Output Current.....$|I_{OH}|$=20mA
- Wide Operating Voltage Range.$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with standard CMOS 4511B.

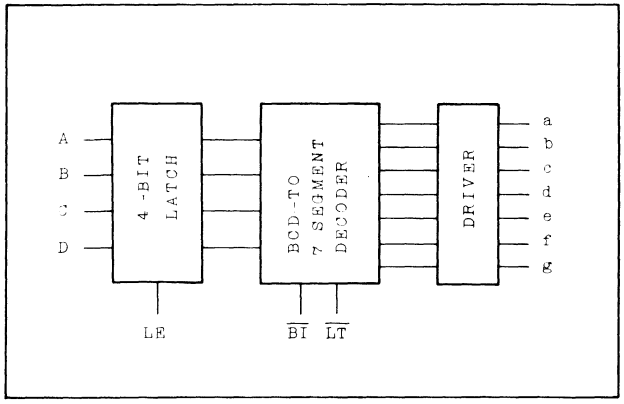
PIN ASSIGNMENT



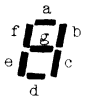
(Top View)

TC74HC4511P/F

BLOCK DIAGRAM

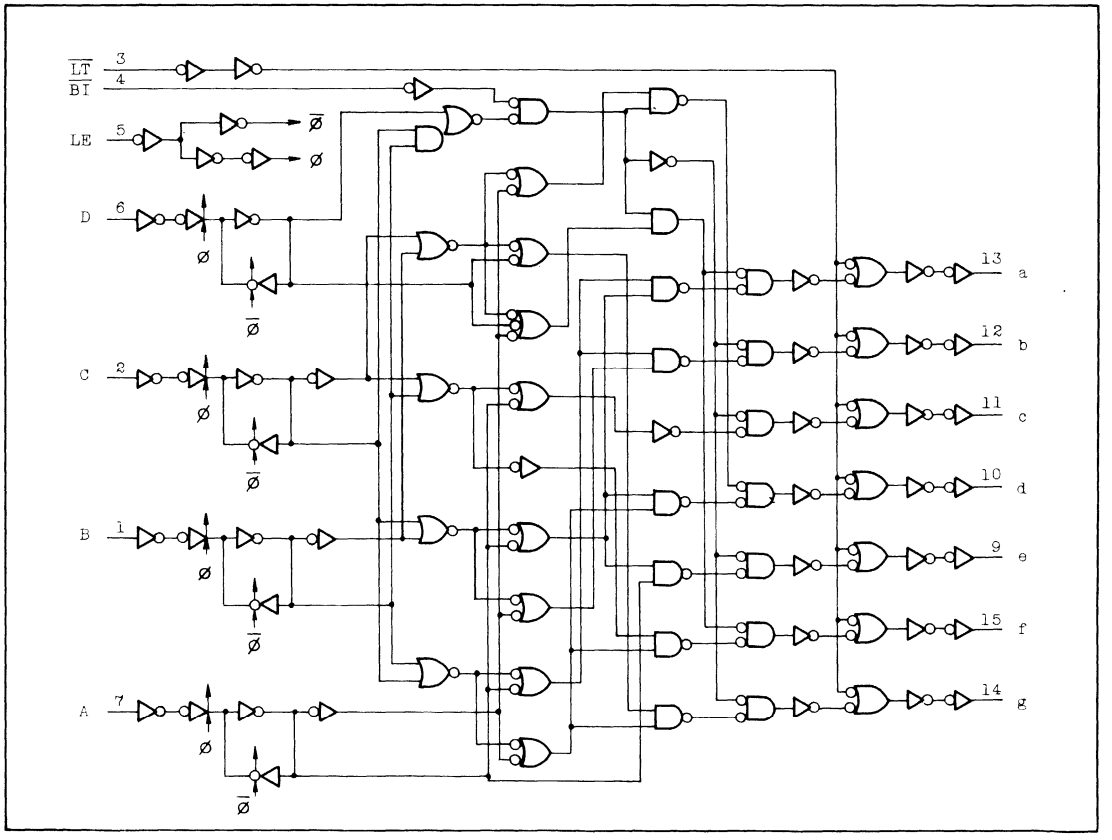


DISPLAY MODE



INPUT CODE										
A	L	H	L	H	L	H	L	H	L	H
B	L	L	H	H	L	L	H	H	L	L
C	L	L	L	L	H	H	H	H	L	L
D	L	L	L	L	L	L	L	L	H	H
DISPLAY	0	1	2	3	4	5	6	7	8	9

LOGIC DIAGRAM



TC74HC4511P/F

TRUTH TABLE

INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

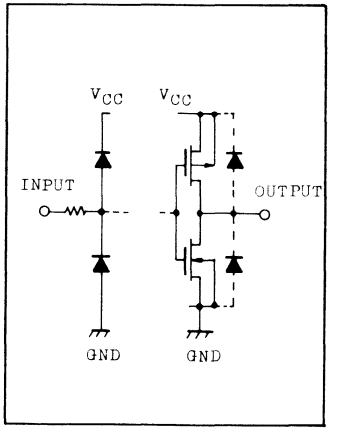
X: Don't care.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25/-35	mA
DC V_{CC}/Ground Current	I_{CC}	+150/-50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C
shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4511P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-20mA	4.5	3.20	3.80	-	2.90	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

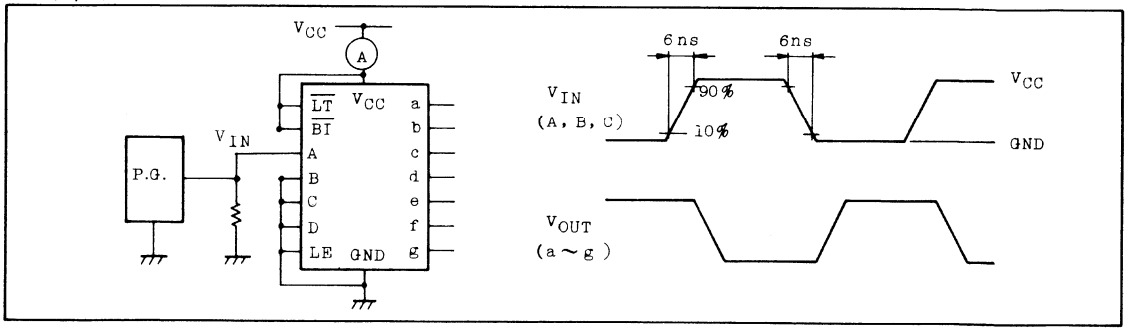
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time Low to High	t_{TLH}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Output Transition Time High to Low	t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (BCD-Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Propagation Delay Time ($\overline{BI}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	116	250	-	315	
			4.5	-	29	50	-	63	
			6.0	-	25	43	-	54	
Propagation Delay Time ($\overline{LT}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Propagation Delay Time (LE - Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	ns
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Minimum Pulse Width (LE)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Data Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	136	-	-	-	

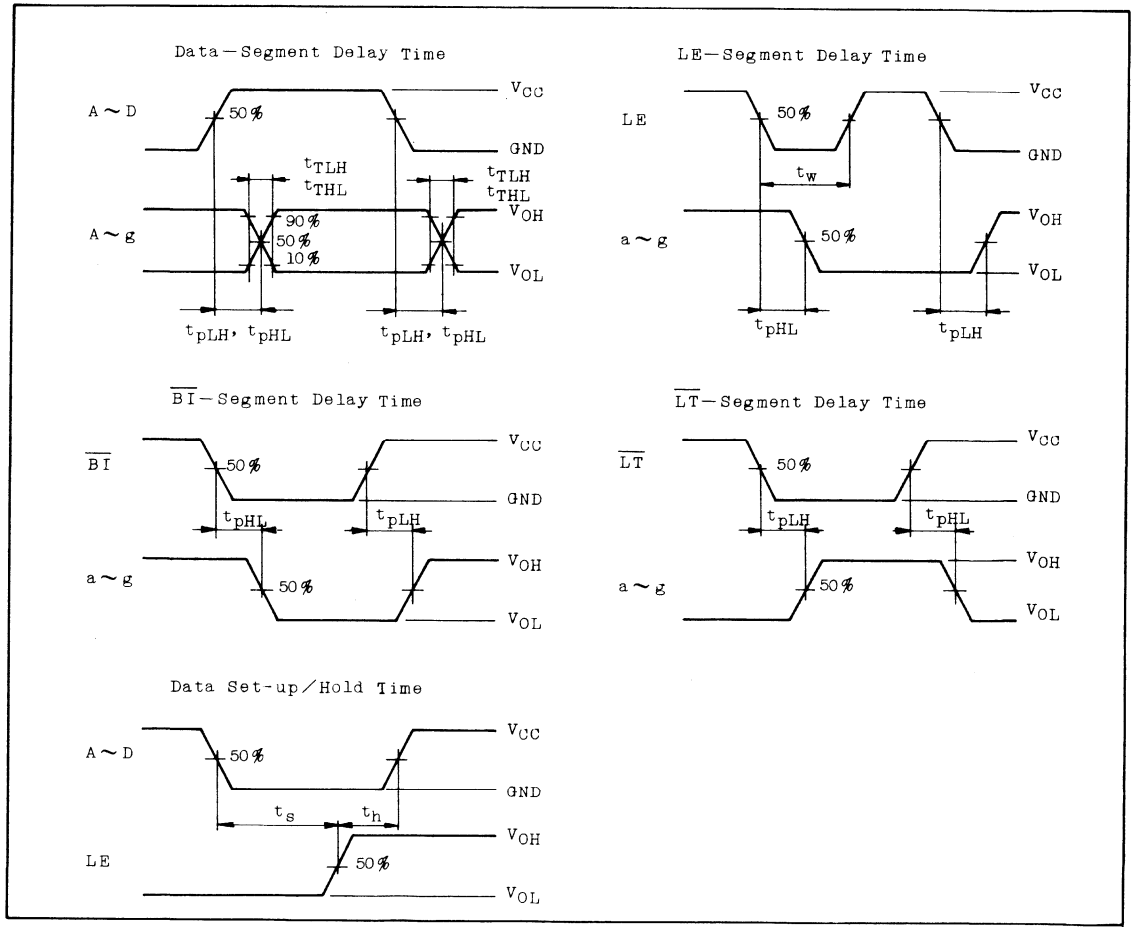
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

TC74HC4511P/F

$I_{CC(opr)}$ TEST CIRCUIT

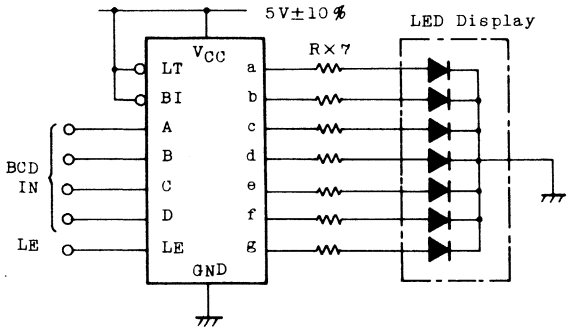


SWITCHING CHARACTERISTICS TEST WAVEFORM



APPLICATION CIRCUIT

Static Display Circuit



Recommended Resistance R

DISPLAY	COLOR	LETTER HIGHT	R
TLR358	Red	13.4mm	390Ω
TLR362	"	14.2	"
TLR332	"	7.6	"
TLR342	"	10.9	"
TLG358	Green	13.4mm	160Ω
TLG362	"	14.2	"
TLG332	"	7.6	"
TLG342	"	10.9	"

TC74HC4514P
TC74HC4515P

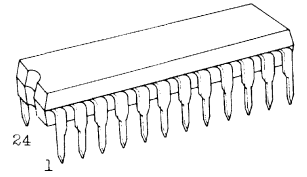
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4514P 4-TO-16 LINE DECODER/LATCH
TC74HC4515P 4-TO-16 LINE DECODER/LATCH (INV.)

The TC74HC4514 and TC74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTS fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. A binary code stored in the four input latches (A thru D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of latches. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at 25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V ∿ 6V
- Pin and Function Compatible with 4514B/4515B



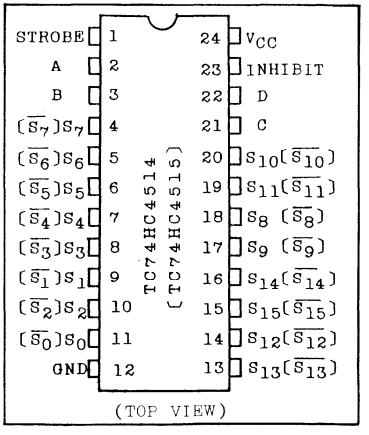
DIP24(3D24A-P)
0.300 INCH(7.62mm) ROW SPACING

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

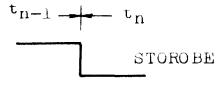
TC74HC4514P
TC74HC4515P

TRUTH TABLE

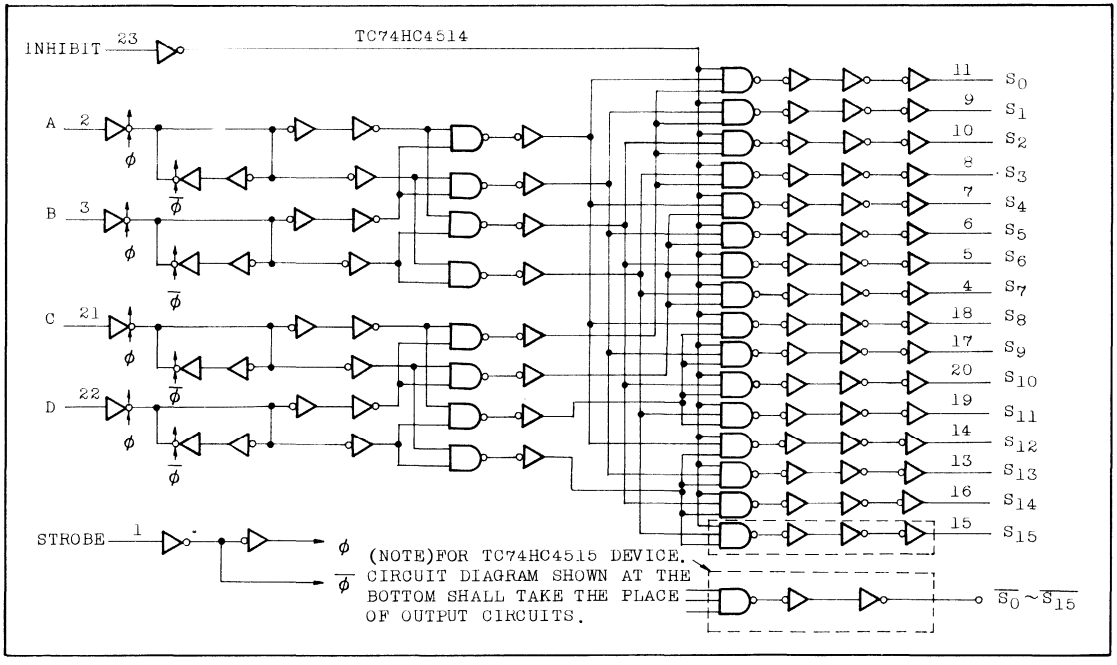
INPUTS					SELECTED OUTPUT TC74HC4514P — "H" (TC74HC4515P — "L")
INHIBIT	A	B	C	D	
L	L	L	L	L	S_0 ($\overline{S_0}$)
L	H	L	L	L	S_1 ($\overline{S_1}$)
L	L	H	L	L	S_2 ($\overline{S_2}$)
L	H	H	L	L	S_3 ($\overline{S_3}$)
L	L	L	H	L	S_4 ($\overline{S_4}$)
L	H	L	H	L	S_5 ($\overline{S_5}$)
L	L	H	H	L	S_6 ($\overline{S_6}$)
L	H	H	H	L	S_7 ($\overline{S_7}$)
L	L	L	L	H	S_8 ($\overline{S_8}$)
L	H	L	L	H	S_9 ($\overline{S_9}$)
L	L	H	L	H	S_{10} ($\overline{S_{10}}$)
L	H	H	L	H	S_{11} ($\overline{S_{11}}$)
L	L	L	H	H	S_{12} ($\overline{S_{12}}$)
L	H	L	H	H	S_{13} ($\overline{S_{13}}$)
L	L	H	H	H	S_{14} ($\overline{S_{14}}$)
L	H	H	H	H	S_{15} ($\overline{S_{15}}$)
H	X	X	X	X	TC74HC4514 — ALL OUTPUTS "L" (TC74HC4515 — ALL OUTPUTS "H")

- X : DON'T CARE
- STROBE = "H" ; REFER TO TRUTH TABLE
- STROBE = "L"

  DATA AT THE NEGATIVE GOING TRANSITION OF STROBE SHALL BE PROVIDED ON THE EACH OUTPUT WHILE STROBE IS HELD LOW.



LOGIC DIAGRAM

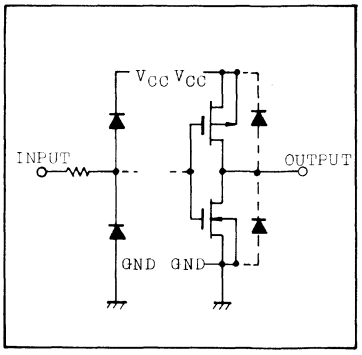


TC74HC4514P
TC74HC4515P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

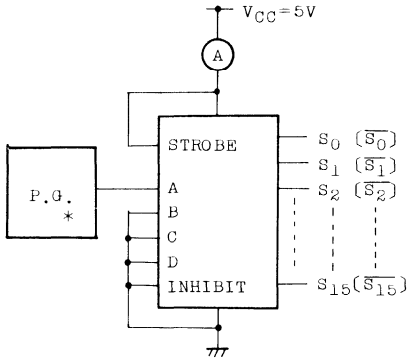
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Rise, Fall Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	nS
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time DATA - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	108	215	-	270	
			4.5	-	27	43	-	54	
			6.0	-	23	37	-	46	
STROBE - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	124	245	-	305	
			4.5	-	31	49	-	61	
			6.0	-	26	42	-	52	
INHIBIT - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Mininum Pulse Width STROBE	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time DATA	t_s		2.0	-	10	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time DATA	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4514P		-	69	-	-	-	
		[TC74HC4515P]		-	[72]	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

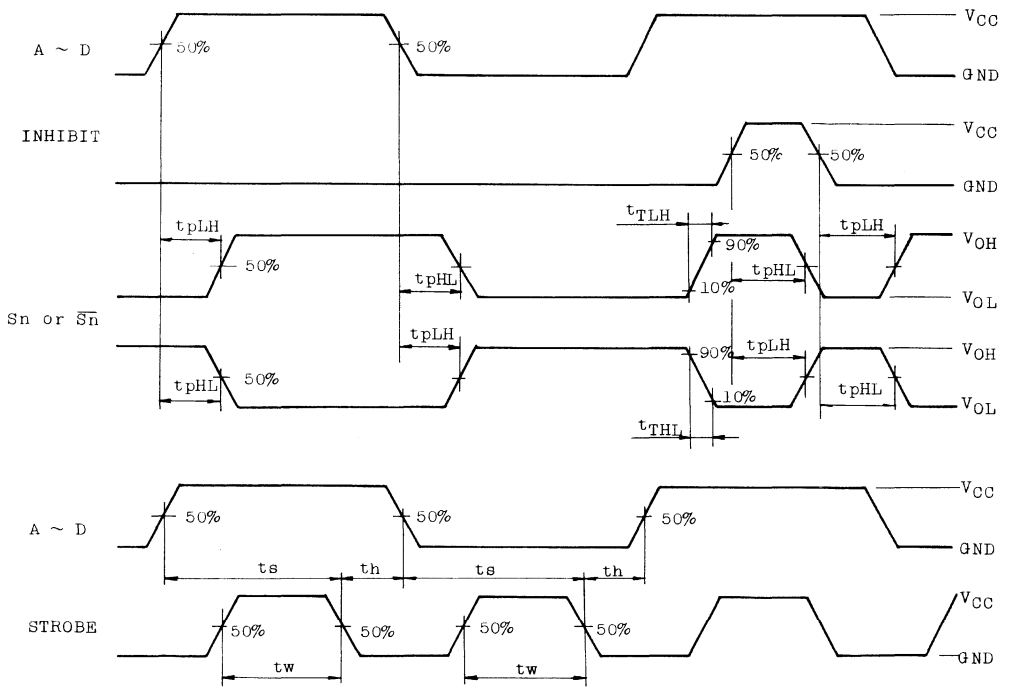
TC74HC4514P
TC74HC4515P

$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISITCS TEST WAVEFORM



TC74HC4518P/F
TC74HC4520P/F

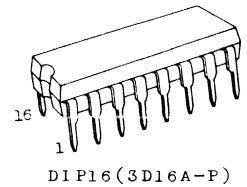
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4518P/F DUAL BCD COUNTER
TC74HC4520P/F DUAL 4-BIT BINARY COUNTER

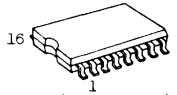
The TC74HC4518 and TC74HC4520 are high speed CMOS DUAL BCD/4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.
It operates ten times as fast as that of metal-gate C^2MOS IC (4518B/4520B) with the same power dissipation.
Since both of TC74HC4518 and TC74HC4520 contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" ($Q_0 \sim Q_3$="L") by giving "H" level signal to CLEAR input regardless of other inputs. The counting condition is changed by the positive going transition of CLOCK input if CE="H" or by the negative going transition of CE if CLOCK="L".
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4518B/4520B



DIP16(3D16A-P)



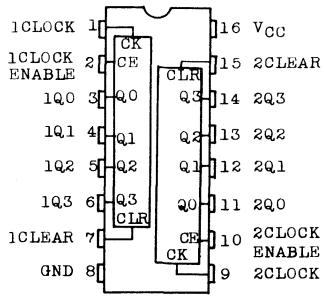
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC4518P/F
TC74HC4520P/F

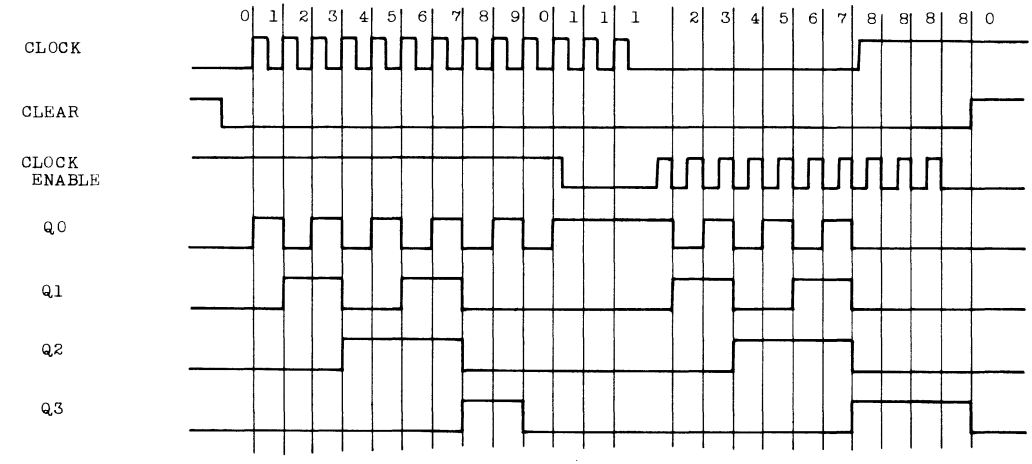
TRUTH TABLE

INPUTS			FUNCTION
CLOCK	CLOCK ENABLE	CLEAR	
↑	H	L	INCLEMENT COUNTER
L	↓	L	INCLEMENT COUNTER
↓	X	L	NO CHANGE
X	↑	L	NO CHANGE
↑	L	L	NO CHANGE
H	↓	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

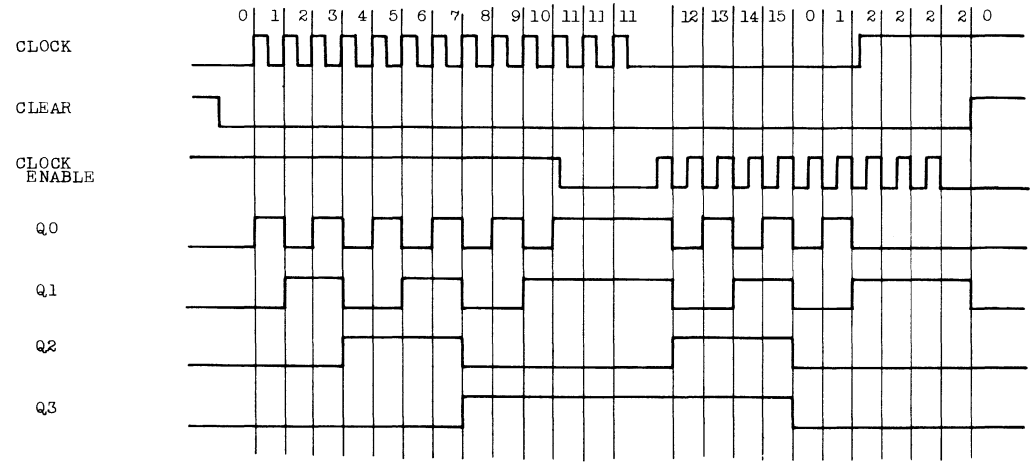
X : DON'T CARE

TIMING CHART

TC74HC4518



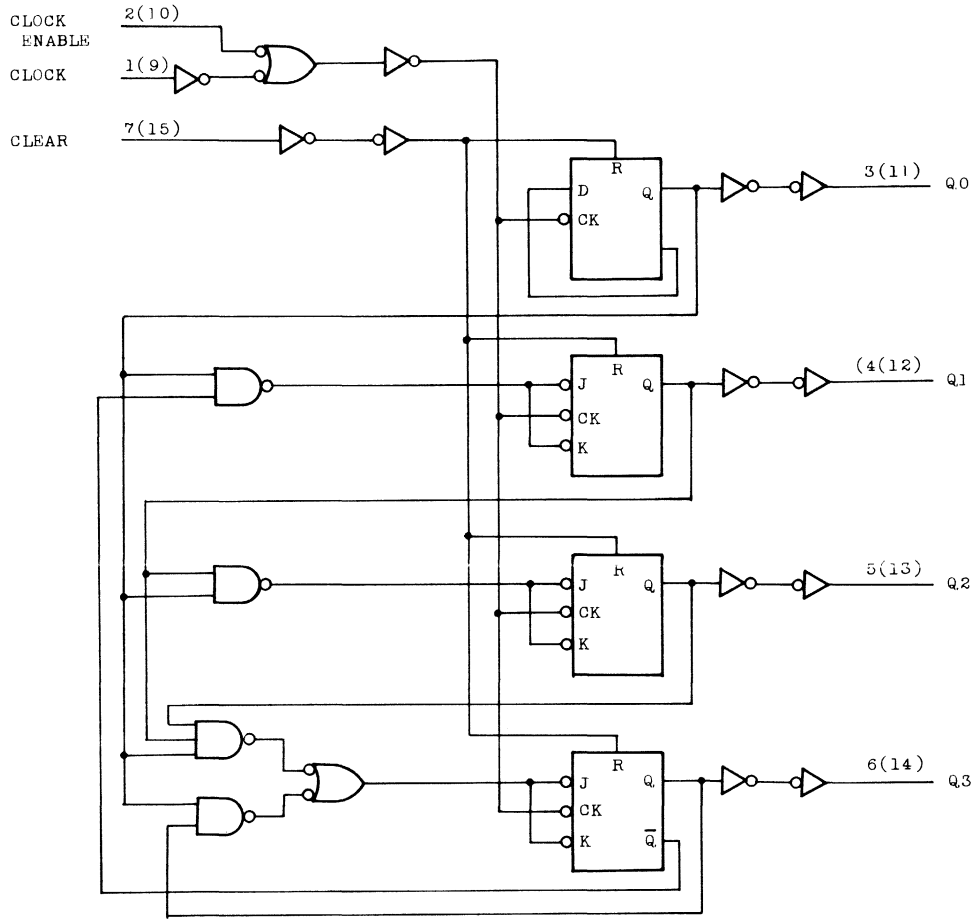
TC74HC4520



TC74HC4518P/F
TC74HC4520P/F

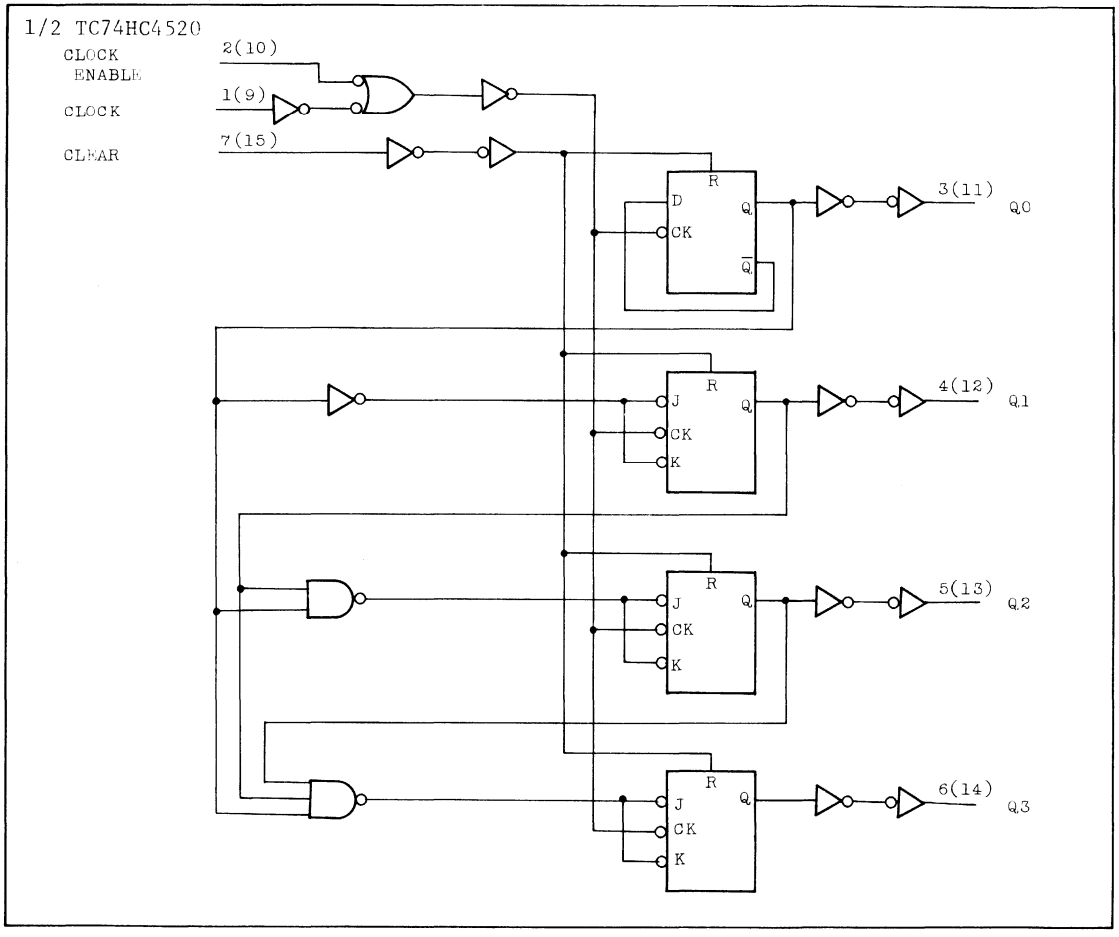
LOGIC DIAGRAM

1/2 TC74HC4518



TC74HC4518P/F
TC74HC4520P/F

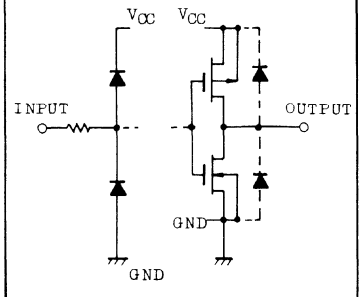
LOGIC DIAGRAM (Continued)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4518P/F
TC74HC4520P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CK, CE - Qn)	t_{pLH} t_{pHL}		2.0	-	100	190	-	240	
			4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time (CLR - Qn)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	25	48	-	20	-	
			6.0	29	56	-	24	-	

TC74HC4518P/F
TC74HC4520P/F

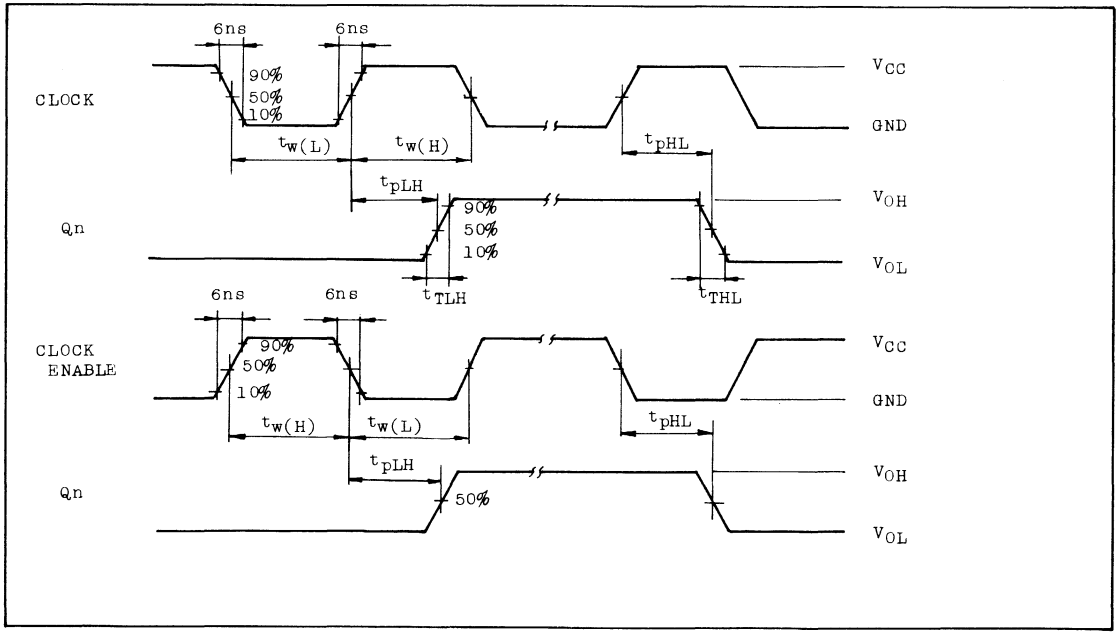
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CK, CE)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum PUlse Width (CLR)	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Removal Time (CLR)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4518		-	145	-	-	-	
		TC74HC4520		-	145	-	-	-	

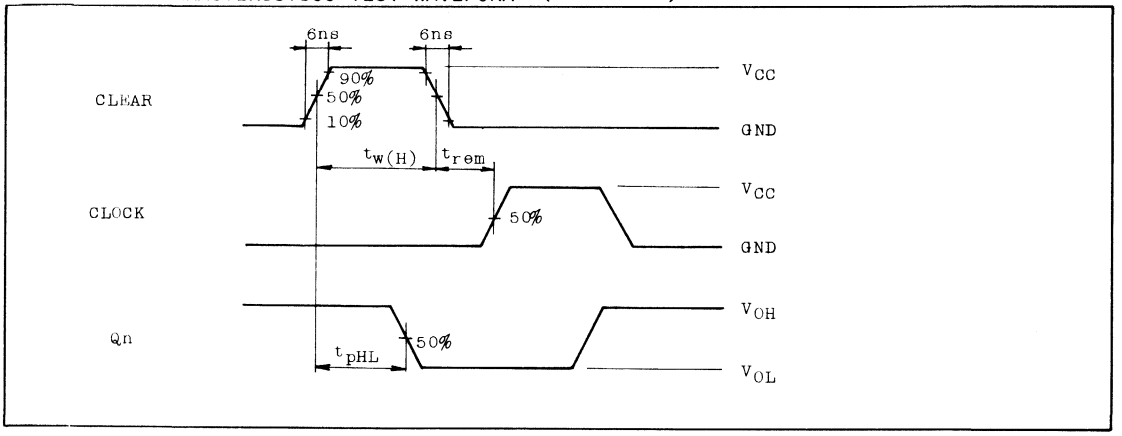
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

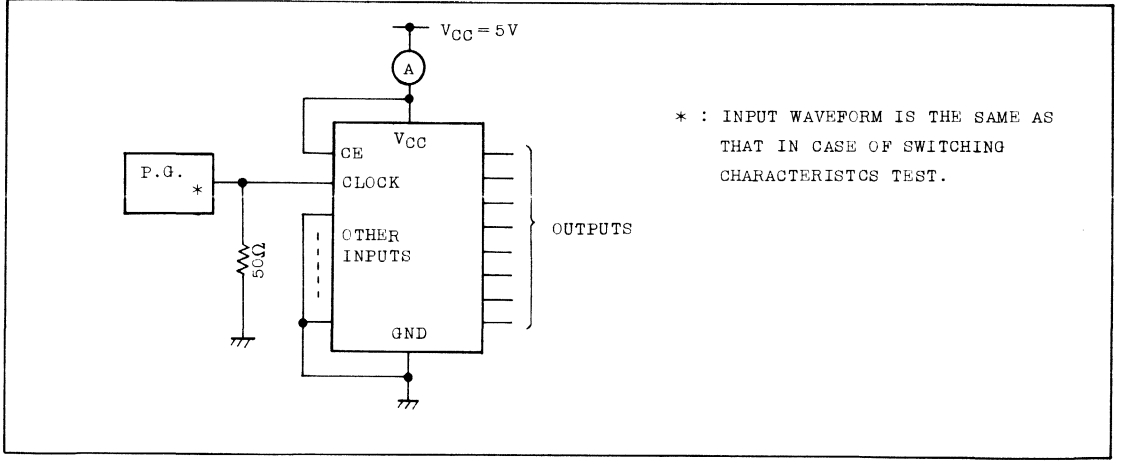
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTCS TEST.

TC74HC4538P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4538P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC4538 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Positive-edge input), another is $\overline{B}$ INPUT (Negative-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CD}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation

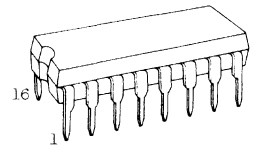
External resistor Rx ..... V_{CC} = 2.0V from 5kΩ to 1MΩ

$V_{CC} \geqq$ 3.0V from 1kΩ to 1MΩ

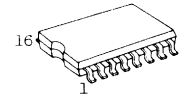
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=27nS(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  - Standby State I_{CC}=4μA(Max.) at Ta=25°C
  - Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Wide Output Pulse Width Range ..... t_w(OUT)=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



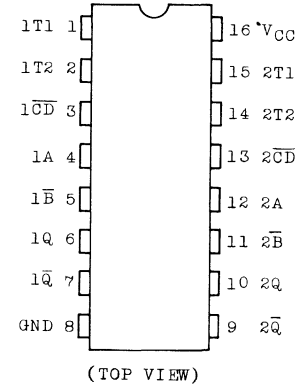
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

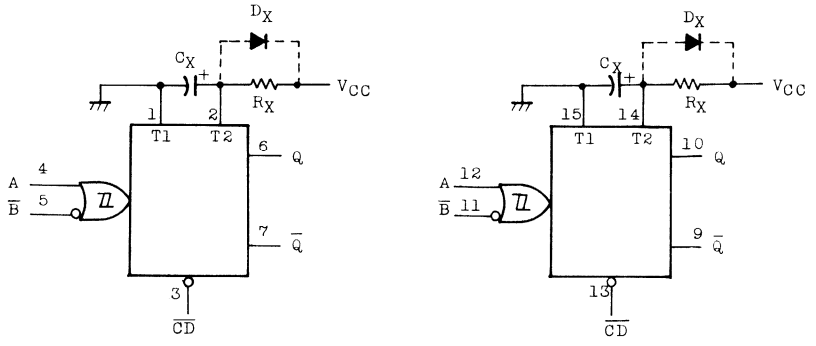
TC74HC4538P/F

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎏	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⎍	⎏	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA.
In the case of large Cx, limitation of falling down time of voltage supply is as follows

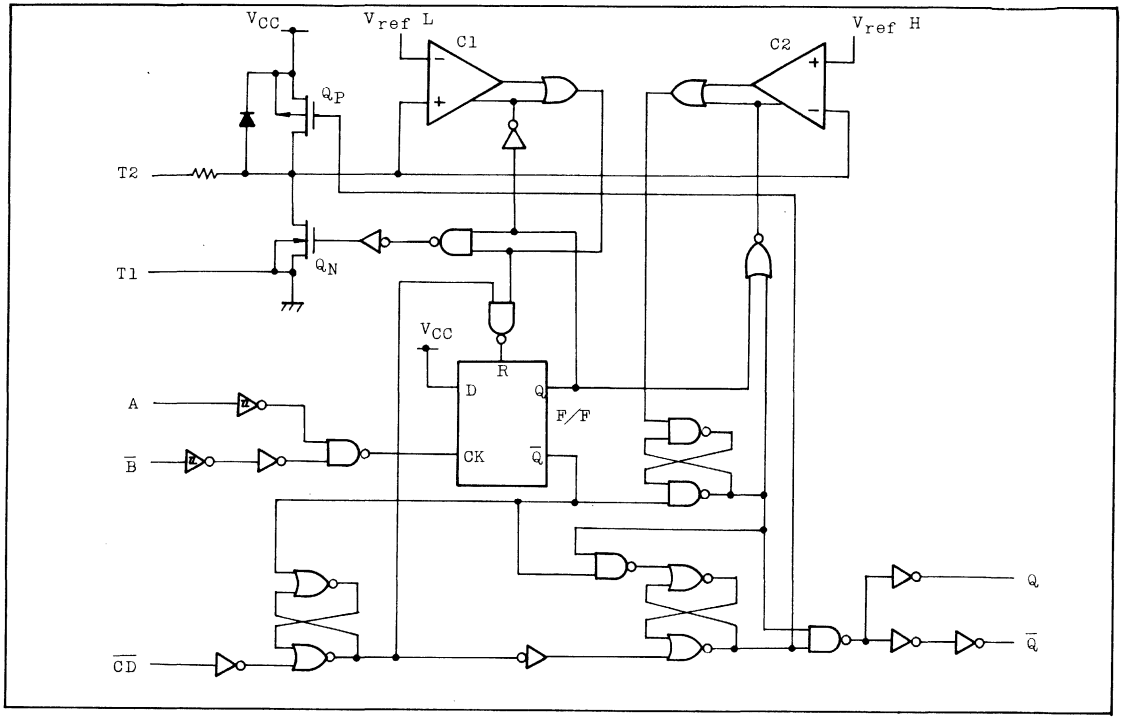
$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC}.)

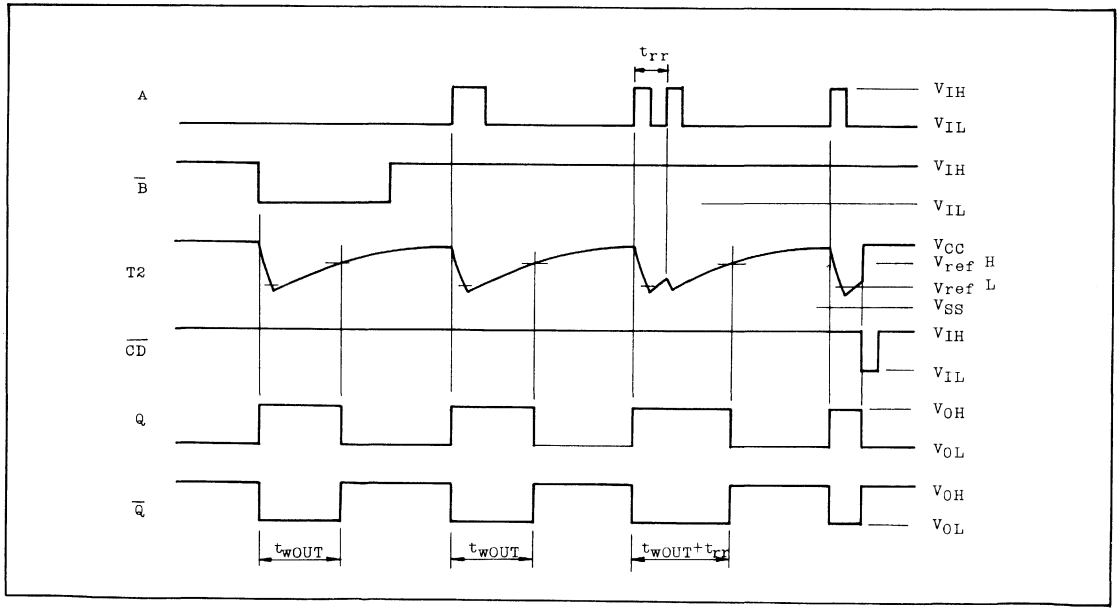
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

TC74HC4538P/F

SYSTEM DIAGRAM



TIMING CHART



FUCNTIONAL DESCRIPTION

(1) Stand-by State

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to T2 node) are in off state.
Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition A INPUT is "L" level and $\overline{B}$ INPUT have falling down signal. Under the condition $\overline{B}$ INPUT is "H" level and A INPUT has rising up signal.
After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of T2 node becomes lower. If voltage level of T2 falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of T2 starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of T2 changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations.
That means, after triggering the voltage level of T2 becomes VrefH, IC keeps its MONO STABLE STATE.
In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.72\ Cx\ Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of T2 falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(Min.) depends on V_{CC} and Cx.

(4) Reset operation

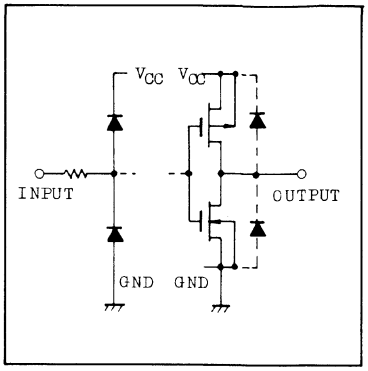
$\overline{CD}$ is normally "H". If $\overline{CD}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level.
This means if $\overline{CD}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC4538P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CD}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/Cext=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per circuit

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (A, $\overline{B}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
	t_{pHL}		6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{CD}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Output Pulse Width	t_{wOUT}	Cx=12pF Rx=1kΩ	3.0	-	210	-	-	-	
			5.0	-	140	-	-	-	
		Cx=100pF Rx=10kΩ	3.0	-	1.45	-	-	-	μs
			5.0	-	1.40	-	-	-	
		Cx=1000pF Rx=10kΩ	3.0	-	10.5	-	-	-	
			5.0	-	10.0	-	-	-	
Output Pulse Width Error Between Circuits (In same Package)	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Trigger Pulse Width	$t_{w(H)}$	A_{IN}	2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(L)}$	$\overline{B}_{IN}$	6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	
			6.0	-	63	-	-	-	
		Cx=0.01μF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{OUT}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	90	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

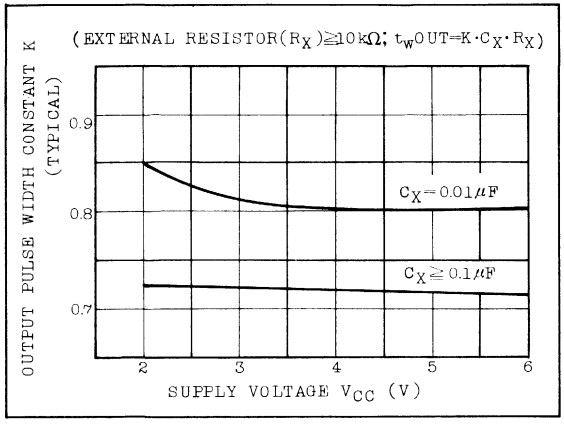
$$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2 \text{ (per monostable)}$$

(I_{CC}': Active Supply Current)

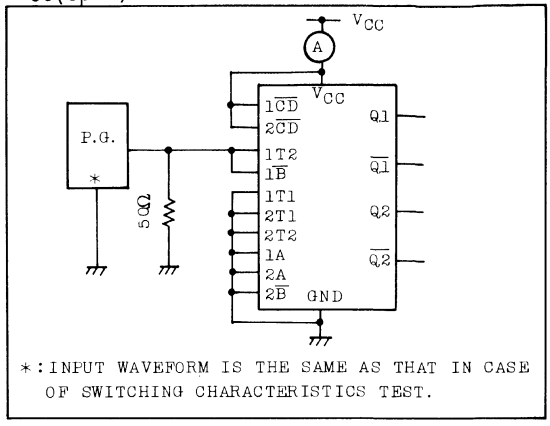
(Duty: %)

TC74HC4538P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

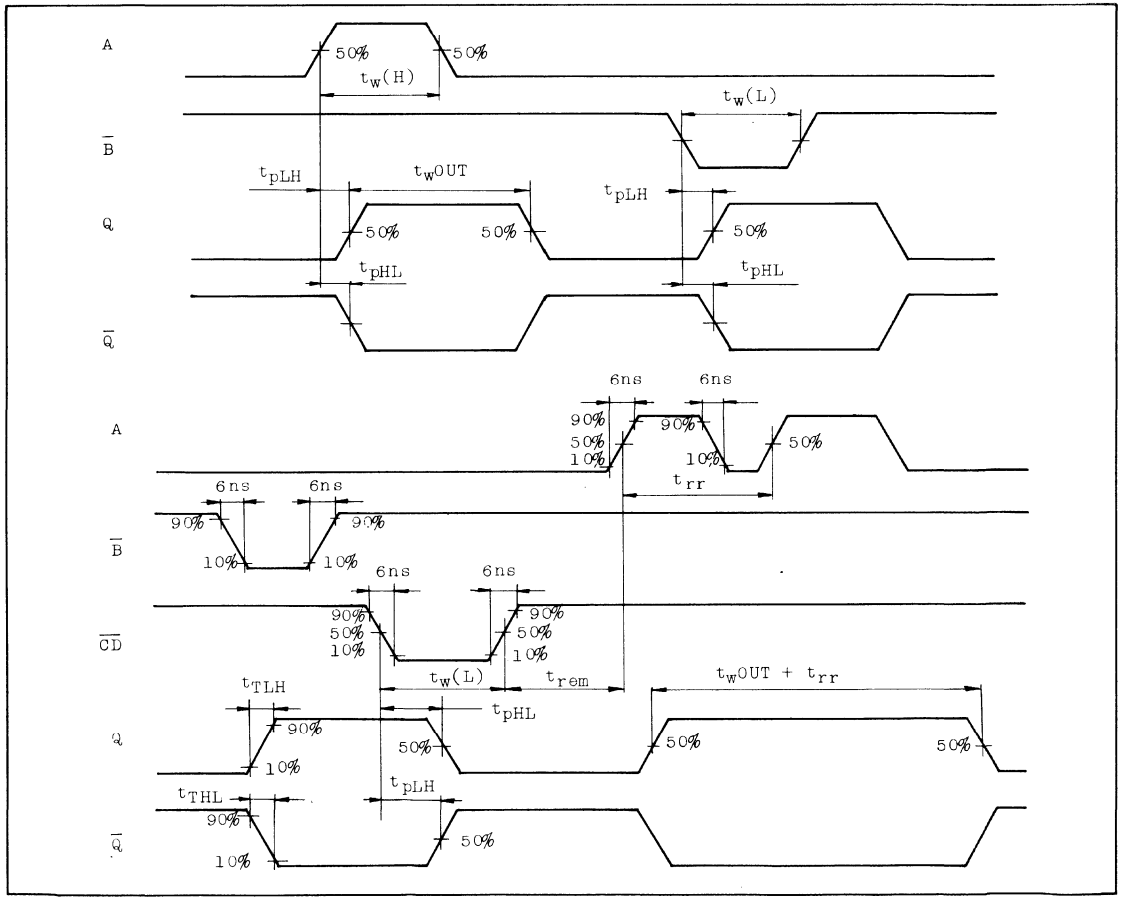


$I_{CC(opr.)}$ TEST WAVEFORM



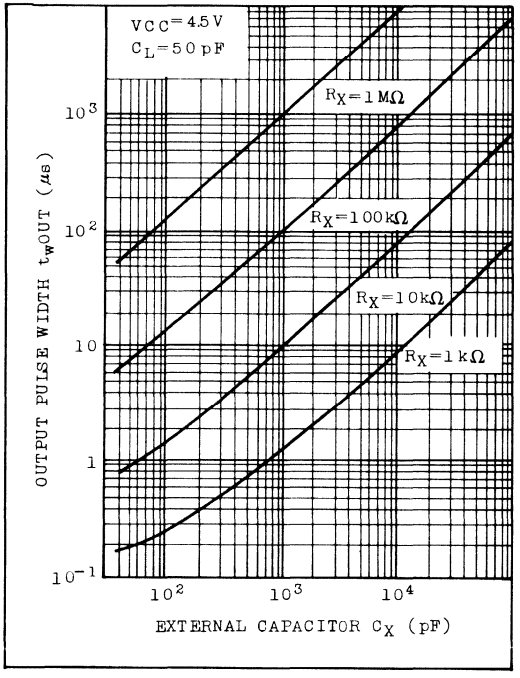
*: INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM

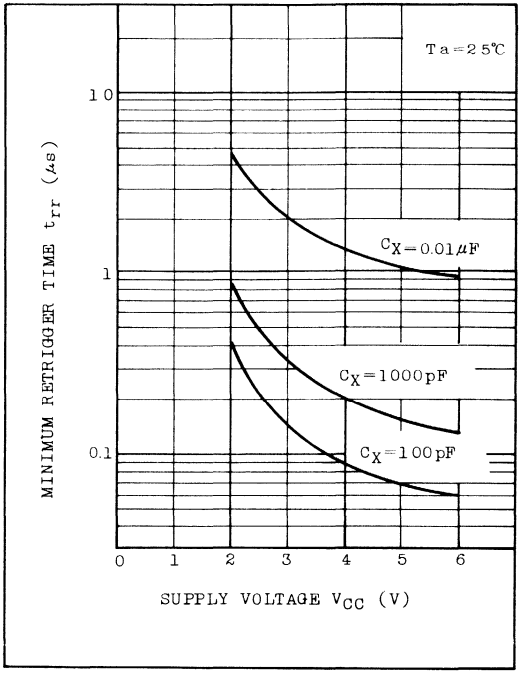


TC74HC4538P/F

t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



TC74HC4543P/F

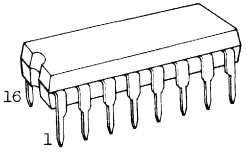
C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4543P/F BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

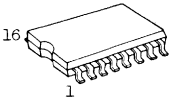
The TC74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated with silicon gate C^2MOS technology. It achieves the high speed latch and decode operation twenty times as fast as the standard CMOS 4511B while maintaining the CMOS low power dissipation. This device consists of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for the liquid crystal display (LCD). When any illegal BCD input signal is applied or BI input is held high, the display is blanked. In case of driving LCD, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as transistor array is required. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_w=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 4543B



DIP16(3D16A-P)



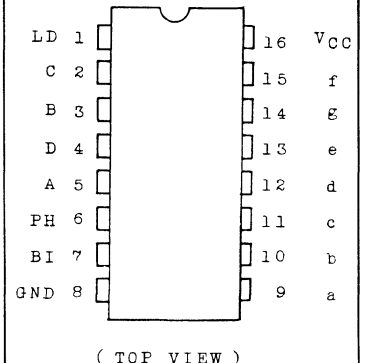
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

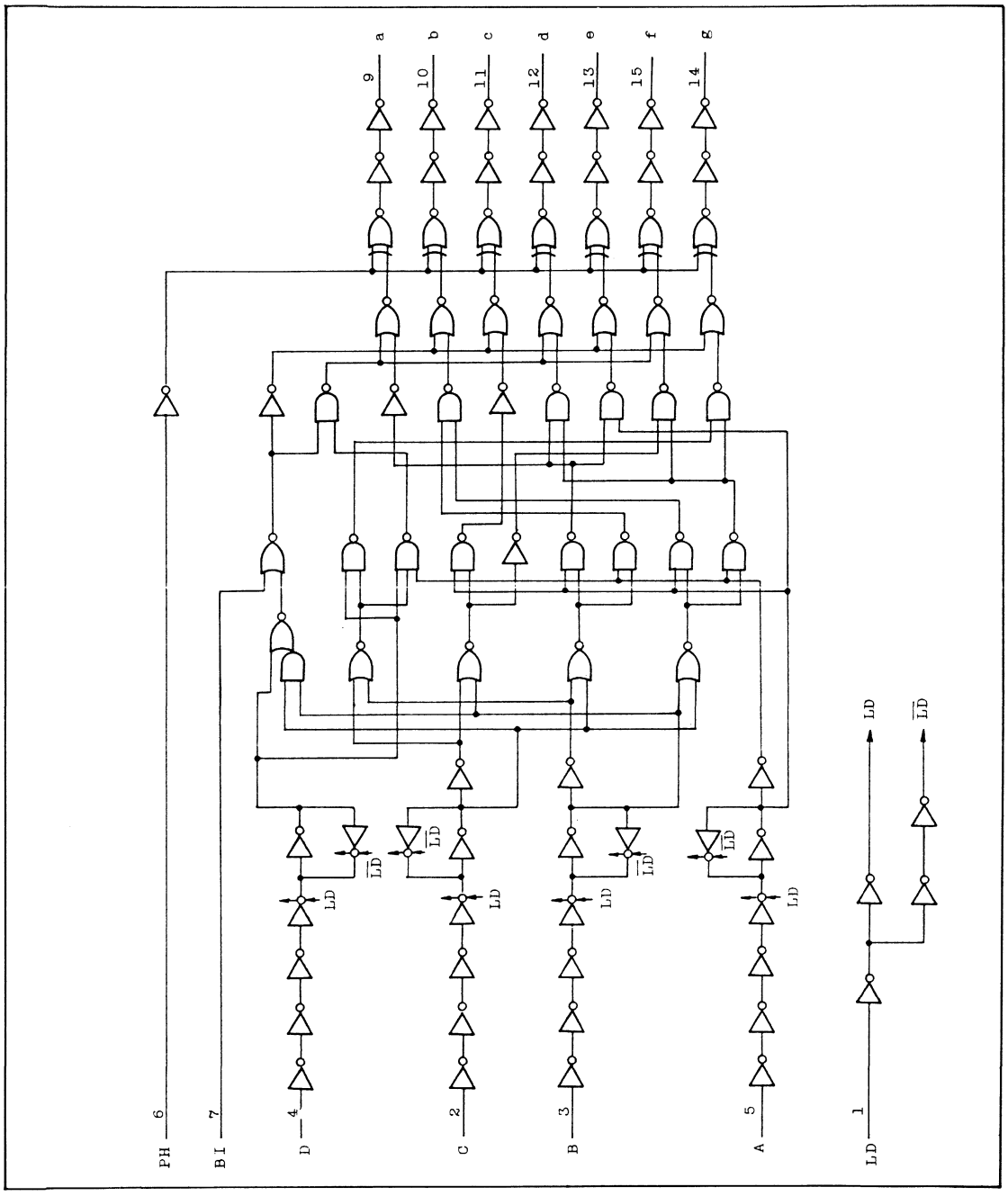
* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TC74HC4543P/F

TRUTH TABLE

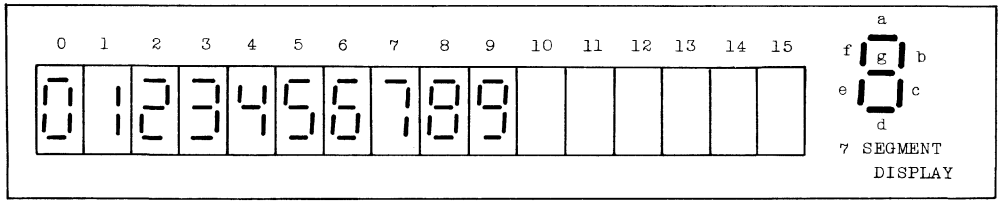
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	###							###
↑	↑	H		↑			INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X : DON'T CARE

↑ : SAME AS ABOVE COMBINATIONS

: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD="H"

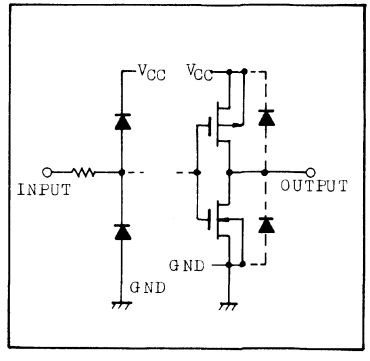
DISPLAY MODE



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4543P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40∿85°C MIN.	-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time BCD - OUT	t_{pLH}		2.0	-	200	385	-	480	
			4.5	-	50	77	-	96	
	t_{pHL}		6.0	-	43	65	-	82	
BI - OUT	t_{pLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{pHL}		6.0	-	26	41	-	51	
PH - OUT	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	

TC74HC4543P/F

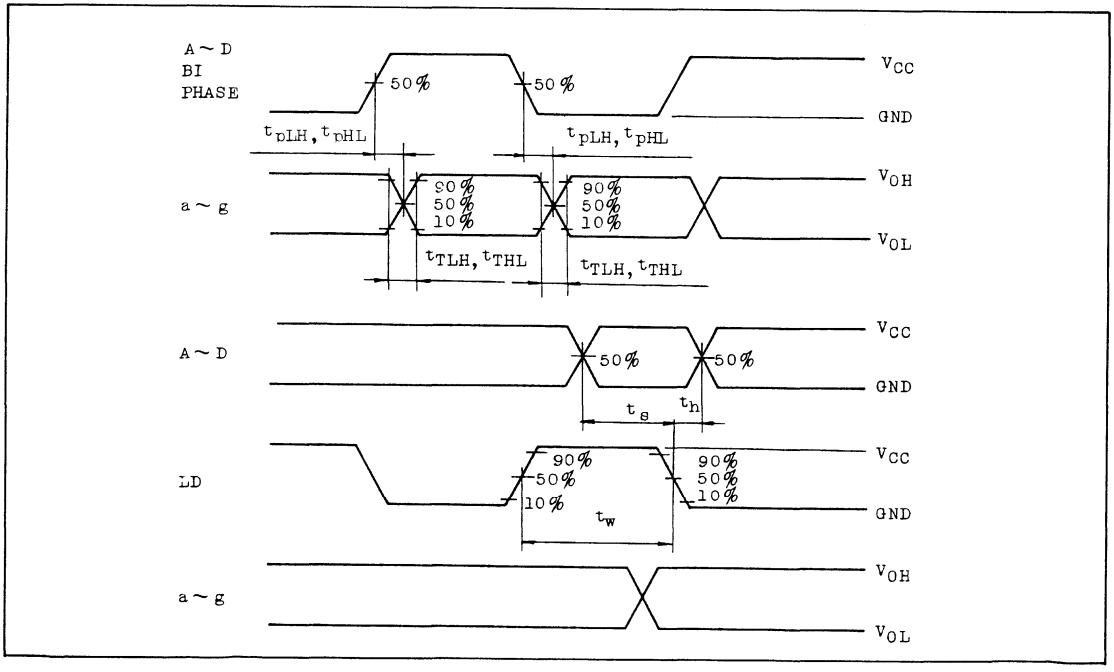
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Minimum Pulse Width (LD)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	30	-	-	-	

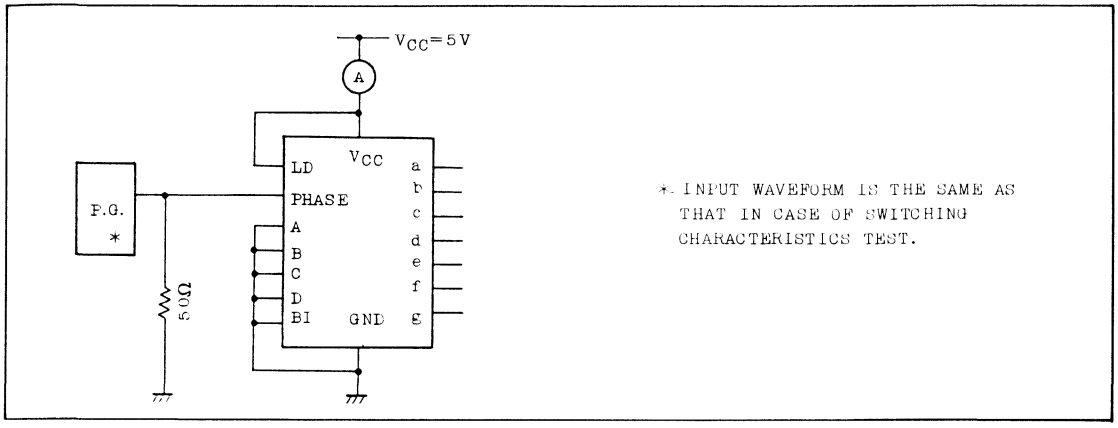
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HCT7007P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT7007P/F HEX BUFFER (TTL INPUT LEVEL)

The TC74HCT07 is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

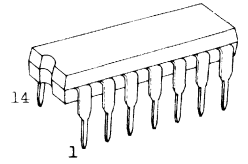
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

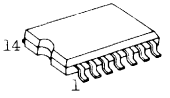
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS07



DIP14(3D14A-P)



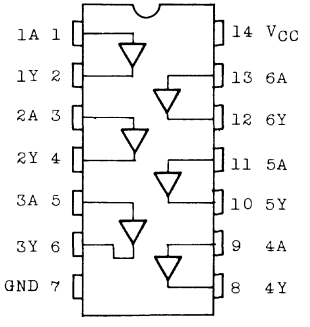
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

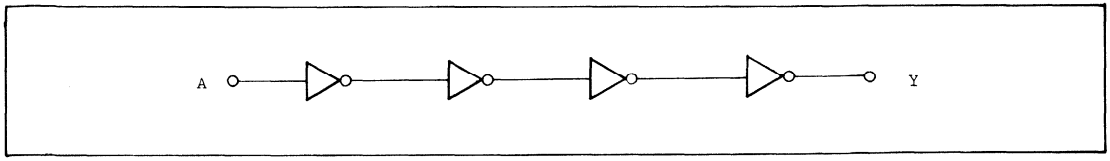
* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

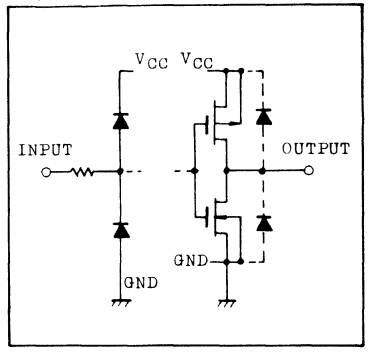
CIRCUIT DIAGRAM (per Circuit)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	V
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	1.0	-	10.0	μA
	I_C	per V_{IN}=0.5V or 2.4V other inputs V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

TC74HCT7007P/F

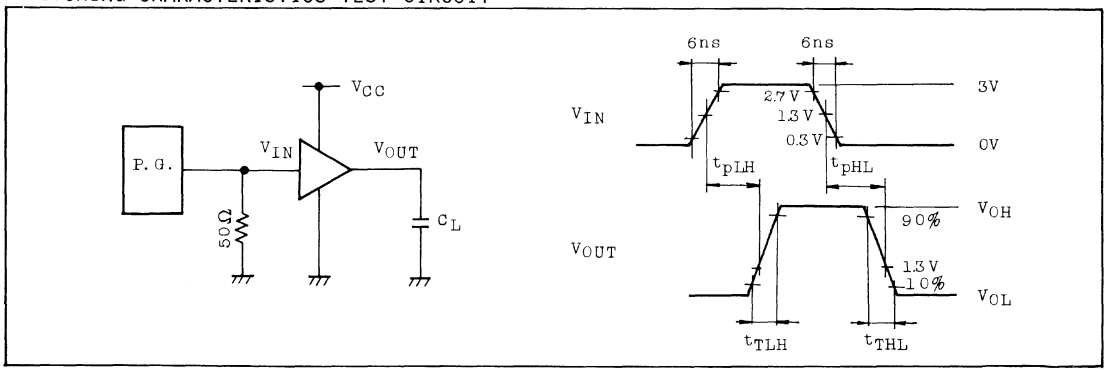
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	16	26	-	33	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	pF

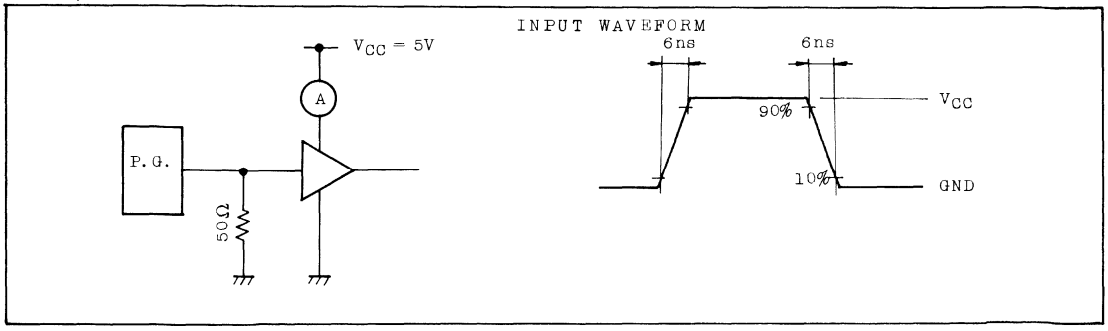
Note 1: C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

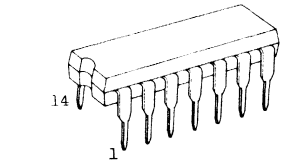
TC74HC7266P/F

TC74HC7266P/F QUAD EXCLUSIVE NOR GATE

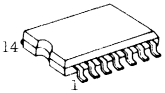
The TC74HC266 is a high speed CMOS QUAD EXCLUSIVE NOR GATE fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Input and output buffer are installed, which enables high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range .....$V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS266



DIP14(3D14A-1)



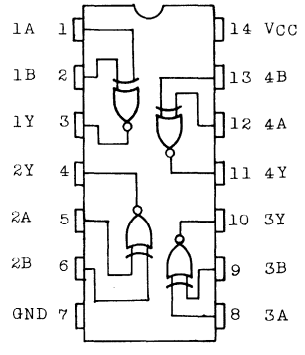
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

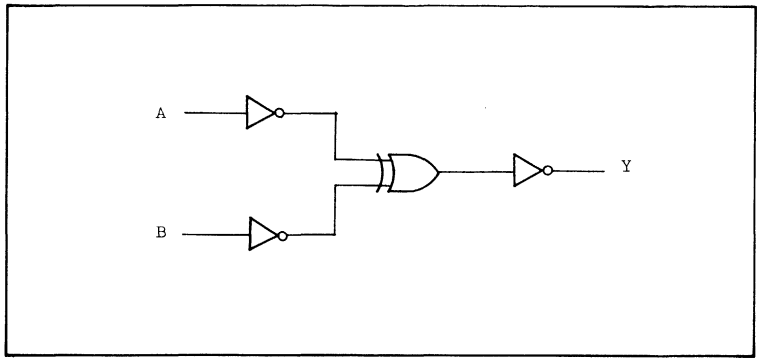
PIN ASSIGNMENT



(TOP VIEW)

TC74HC7266P/F

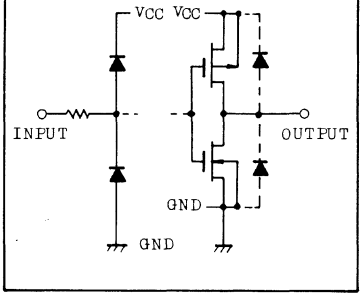
LOGIC DIAGRAM (per Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	52	115	-	145	
			4.5	-	13	23	-	29	
	t_{pHL}		6.0	-	11	20	-	25	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

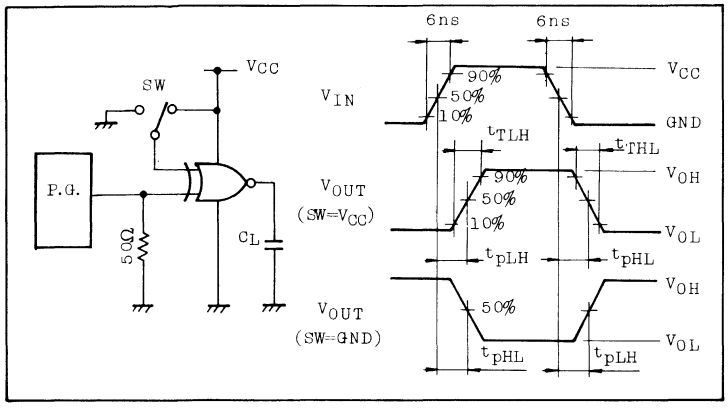
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

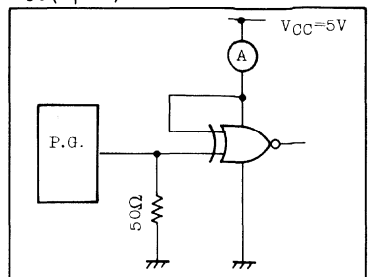
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Gate)}$$

TC74HC7266P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr.) TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC7292P
TC74HC7294P

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC7292P PROGRAMMABLE DIVIDER/TIMER
TC74HC7294P PROGRAMMABLE DIVIDER/TIMER

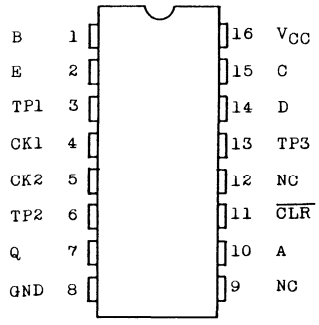
The TC74HC7292 and TC74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table (1)).
The TC74HC7292 can divide from 2^2 to 2^{31}, and the TC74HC7294 can divide from 2^2 to 2^{15}.
Both types feature an active-low clear input to initialize the state of all flip-flops.
To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the 74HC7292 and TP on the 74HC7294).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX} = 50MHz [7292], 60MHz [7294] (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Summetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS292/294

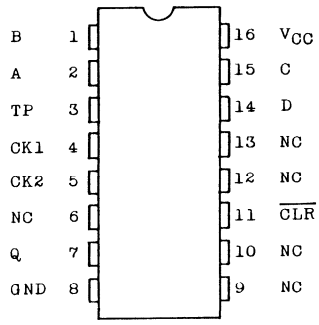
PIN ASSIGNMENT

TC74HC7292



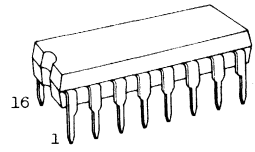
(TOP VIEW)

TC74HC7294



(TOP VIEW)

NC : NO CONNECTION



DIP16(3D16A-P)

TC74HC7292P
TC74HC7294P

TRUTH TABLE

$\overline{\text{CLEAR}}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↓	L	UP Count
H	L	↓	
H	H	X	NO Change
H	X	H	

TC74HC7292

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP2	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

TC74HC7292P
TC74HC7294P

TRUTH TABLE

TC74HC7294

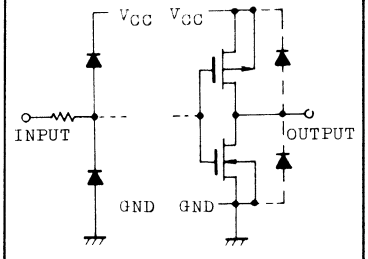
PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC7292P
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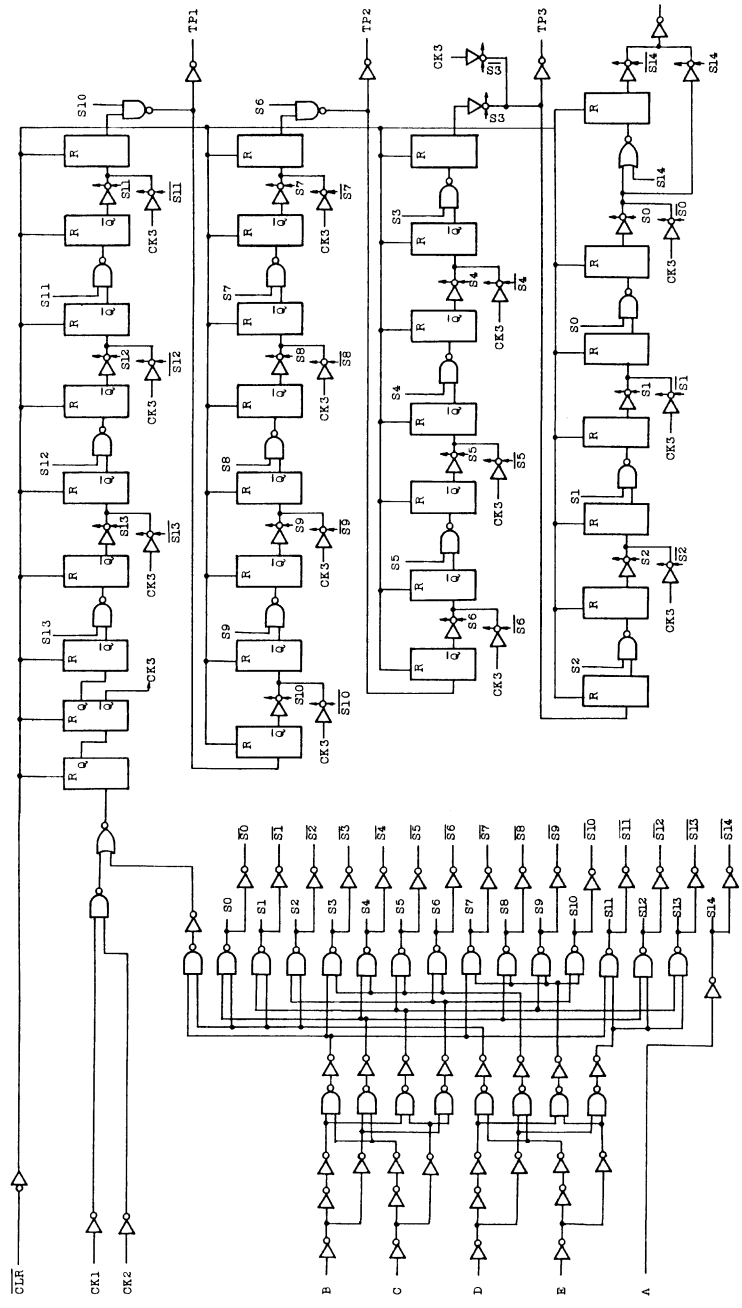
LOGIC DIAGRAM

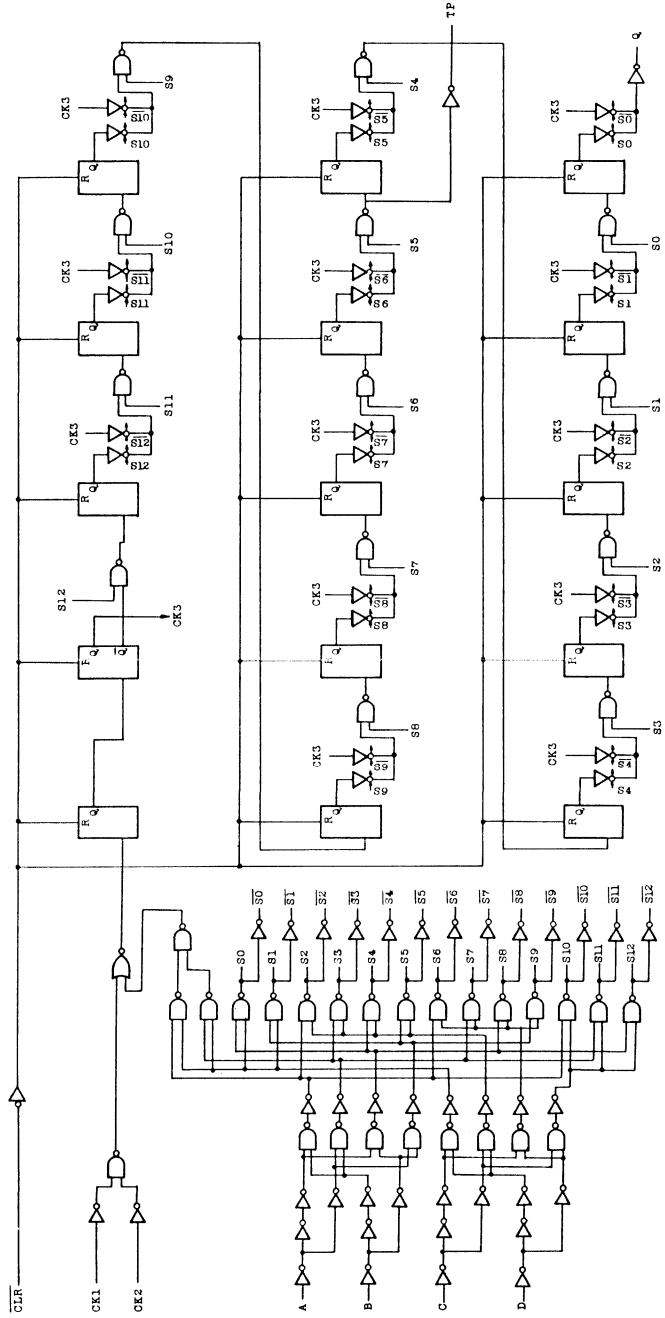
TC74HC7292



TC74HC7292P
TC74HC7294P

LOGIC DIAGRAM

TC74HC7294



TC74HC7292P
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RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

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AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Transition Time (TP)	t_{TLH} t_{THL}		2.0	-	132	255	-	320	
			4.5	-	33	51	-	64	
			6.0	-	28	43	-	54	
Propagation Delay Time (CLOCK - Q) *	t_{pLH} t_{pHL}	B="H" A=C=D=E="L"	2.0	-	264	500	-	625	
			4.5	-	66	100	-	125	
			6.0	-	56	85	-	106	
Propagation Delay Time (CLOCK - Q) **	t_{pLH} t_{pHL}	B="H" A=C=D="L"	2.0	-	236	455	-	570	
			4.5	-	59	91	-	114	
			6.0	-	50	77	-	97	
Propagation Delay Time ($\overline{CLEAR}$ - Q) *	t_{pHL}		2.0	-	224	425	-	530	
			4.5	-	56	85	-	106	
			6.0	-	48	72	-	90	
Propagation Delay Time ($\overline{CLEAR}$ - Q) **	t_{pHL}		2.0	-	204	390	-	490	
			4.5	-	51	78	-	98	
			6.0	-	43	66	-	83	
Maximum Clock Frequency *	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	32	48	-	26	-	
			6.0	38	56	-	31	-	
Maximum Clock Frequency **	f_{MAX}		2.0	7	14	-	6	-	ns
			4.5	32	55	-	30	-	
			6.0	44	65	-	35	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	36	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Pulse Width ($\overline{CLEAR}$) *	$t_{w(L)}$		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Pulse Width ($\overline{CLEAR}$) **	$t_{w(L)}$		2.0	-	72	175	-	220	
			4.5	-	18	35	-	44	
			6.0	-	15	30	-	37	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	74HC7292		-	22	-	-	-	
		74HC7294		-	23	-	-	-	

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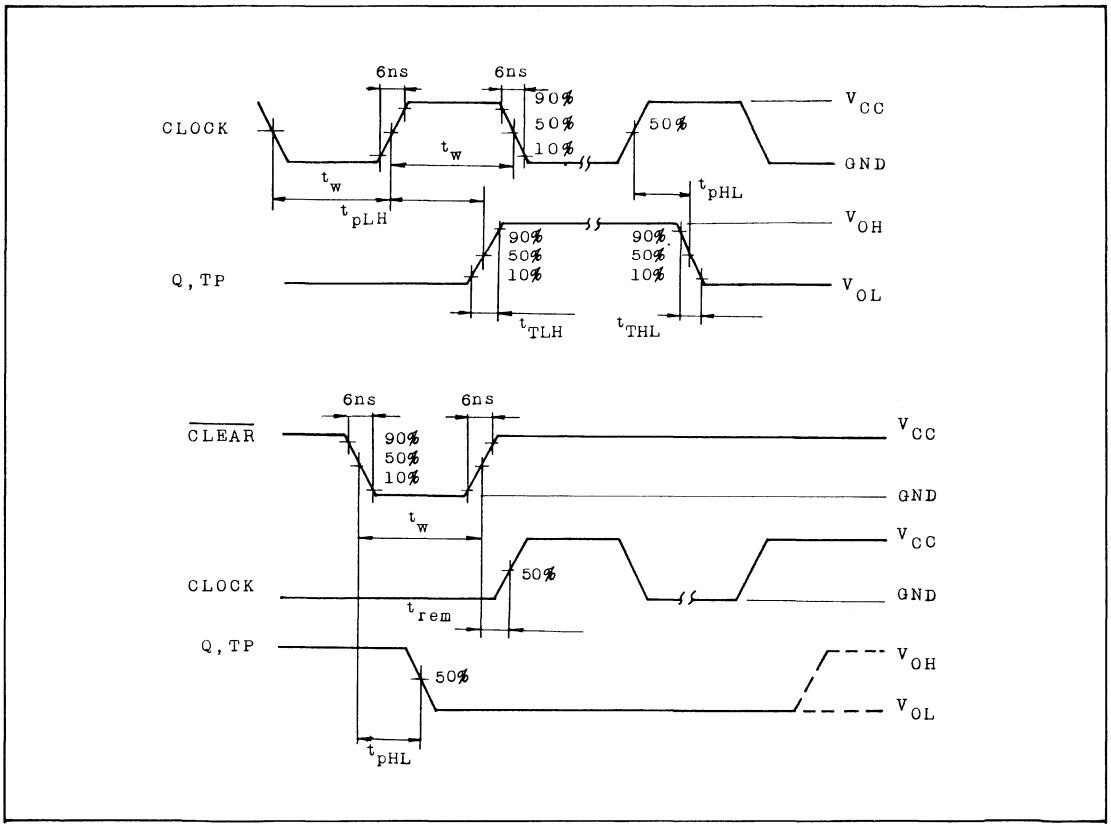
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

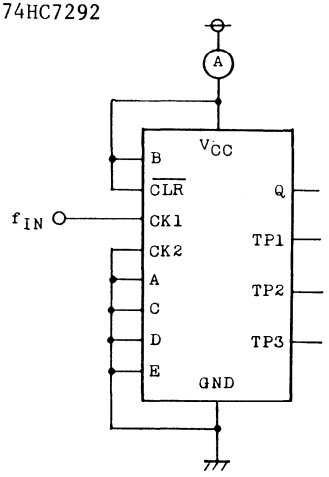
(2): * ; for TC74HC7292
**; for TC74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM

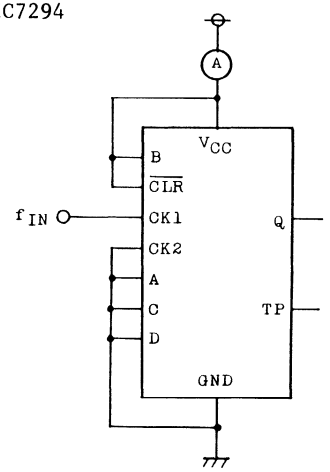


I_{CC}(Opr.) TEST CIRCUIT

TC74HC7292



TC74HC7294

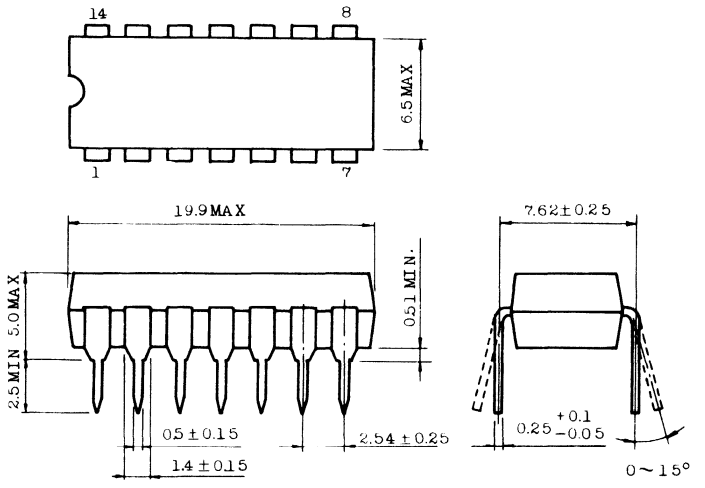


* Input transition time is the same as that in case of switching characteristics test.

11. OUTLINE DRAWINGS

DIP 14 PIN OUTLINE DRAWING (3D14A-P)

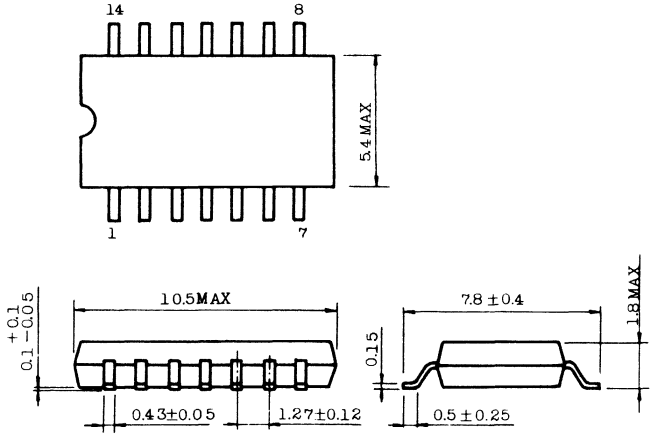
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

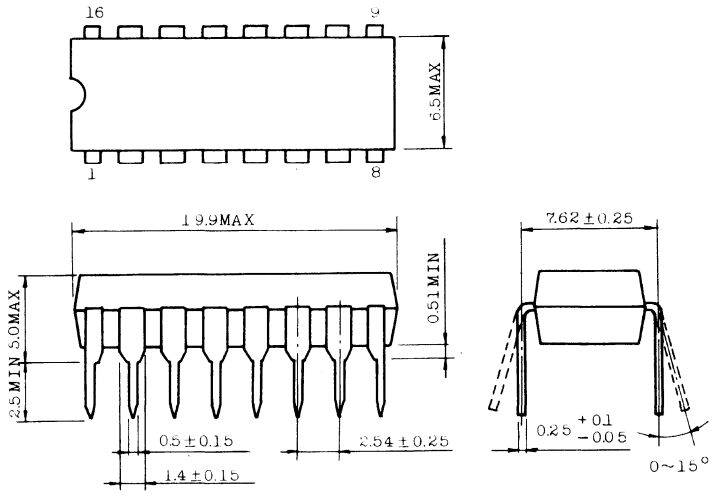
MFP 14 PIN OUTLINE DRAWING (F14GB-P)

Unit in mm



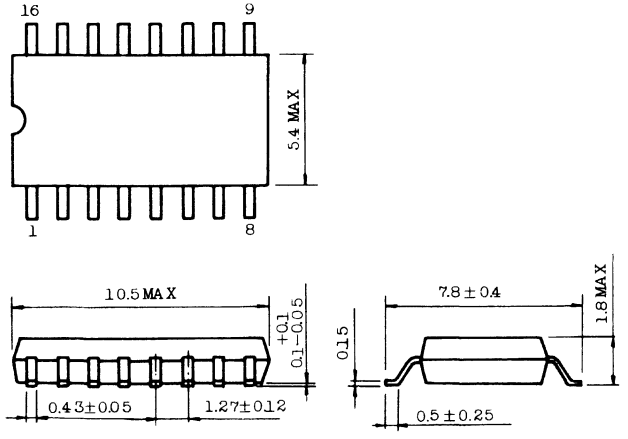
Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

DIP 16 PIN OUTLINE DRAWING (3D16A-P) Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

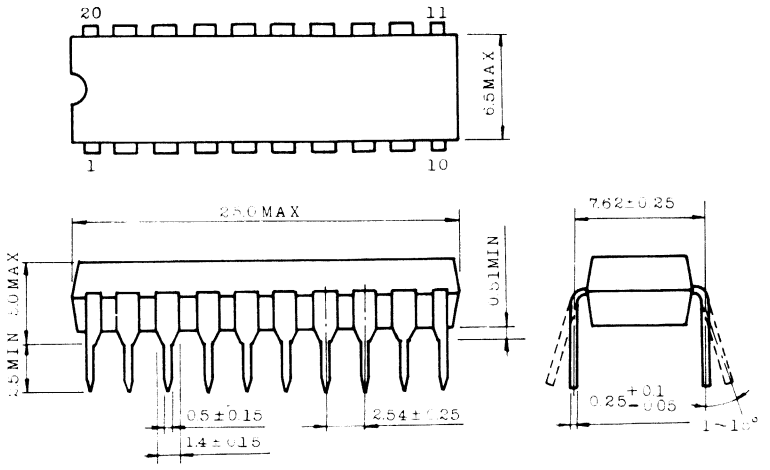
MFP 16 PIN OUTLINE DRAWING (F16GC-P) Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

DIP 20 PIN OUTLINE DRAWING (3D20A-P)

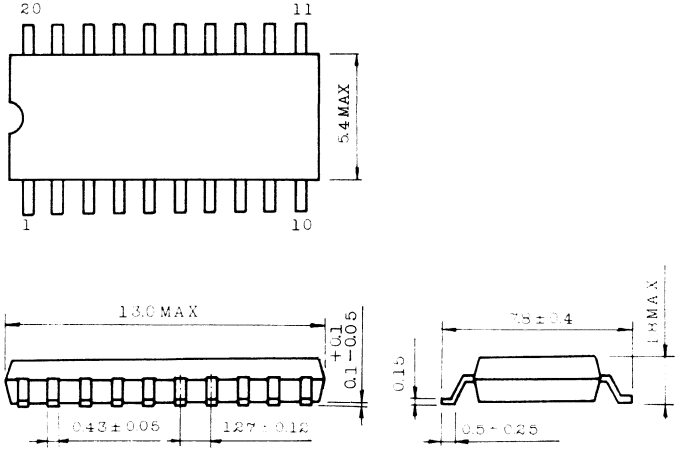
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.20 leads.

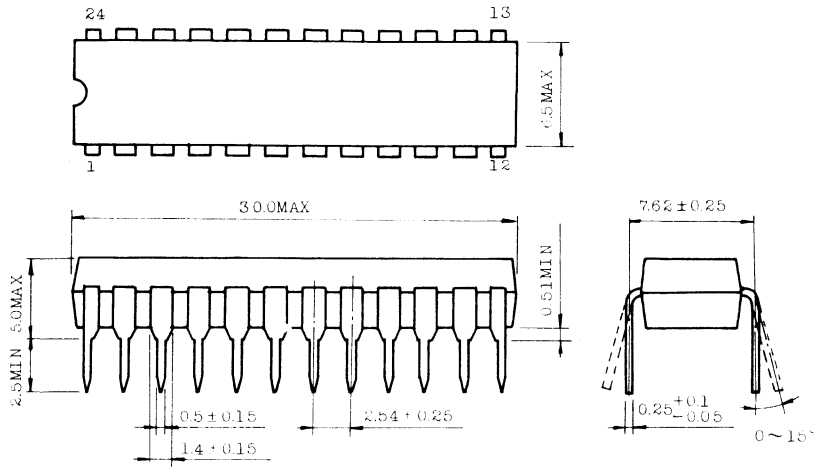
MFP 20 PIN OUTLINE DRAWING (F20GA-P)

Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.20 leads.

DIP 24 PIN OUTLINE DRAWING (3D24A-P) Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.

12. CROSS REFERENCE TABLE

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
QUAD 2-INPUT NAND GATE	00	00	00	00	00	00
QUAD 2-INPUT NOR GATE	02	02	02	02	02	–
QUAD 2-INPUT NAND GATE (OPEN DRAIN)	03	03	03	03	03	–
HEX INVERTER	04	04	04	04	04	04
HEX INVERTER	T04	T04	–	T04	T04	T04
HEX INVERTER (SINGLE STAGE)	U04	U04	U04	U04	U04	U04
QUAD 2-INPUT AND GATE	08	08	08	08	08	08
TRIPLE 3-INPUT NAND GATE	10	10	10	10	10	10
TRIPLE 3-INPUT AND GATE	11	11	11	11	11	11
HEX SCHMITT INVERTER	14	14	14	14	14	14
DUAL 4-INPUT NAND GATE	20	20	20	20	20	20
DUAL 4 INPUT AND GATE	21	–	21	21	–	–
TRIPLE 3-INPUT NOR GATE	27	27	27	27	27	27
8-INPUT NAND GATE	30	30	30	30	30	–
QUAD 2-INPUT OR GATE	32	32	32	32	32	32
BCD TO DECIMAL DECODER	42	42	42	42	42	42
DUAL 2W-2I AND/OR INVERT GATE	51	51	51	–	51	–
DUAL J-K FLIP-FLOP WITH CLEAR	73	73	73	73	73	73
DUAL D FLIP-FLOP WITH PRESET AND CLEAR	74	74	74	74	74	74
4-BIT D-TYPE LATCH	75	75	75	75	75	75
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	76	76	76	–	76	–
4-BIT D-TYPE LATCH	77	–	77	–	–	–
4-BIT MAGNITUDE COMPARATOR	85	85	85	85	85	85

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
QUAD EXCLUSIVE OR GATE	86	86	86	86	86	86
DUAL J-K FLIP-FLOP WITH CLEAR	107	107	107	107	107	107
DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR	109	109	109	109	109	109
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	112	112	112	112	112	112
DUAL J-K FLIP-FLOP WITH PRESET	113	113	113	–	113	–
DUAL MONOSTABLE MULTIVIBRATOR	123	123A	–	123	123A	123
QUAD BUS BUFFER (3-STATE)	125	125	125	125	125	–
QUAD BUS BUFFER (3-STATE)	126	126	126	126	126	–
3-TO-8 LINE DECODER/LATCH	131	–	–	–	–	–
QUAD 2-INPUT SCHMITT NAND	132	132	–	132	132	132
13-INPUT NAND GATE	133	133	133	–	133	133
3-TO-8 LINE DECODER/LATCH	137	137	137	137	137	137
3-TO-8 LINE DECODER/LATCH	T137	–	T137	T137	–	–
3-TO-8 LINE DECODER	138	138	138	138	138	138
3-TO-8 LINE DECODER	T138	T138	T138	T138	T138	T138
DUAL 2-TO-4 LINE DECODER	139	139	139	139	139	139
10-TO-4 LINE PRIORITY ENCODER	147	147	147	147	147	147
8-TO-3 LINE PRIORITY ENCODER	148	148	148	–	148	–
8-CHANNEL MULTIPLEXER	151	151	151	151	151	151
DUAL 4-CHANNEL MULTIPLEXER	153	153	153	153	153	153
4-TO-16 LINE DECODER	154	154	154	154	154	154
DUAL 2-TO-4 LINE DECODER	155	–	–	–	–	–
QUAD 2-CHANNEL MULTIPLEXER	157	157	157	157	157	157

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
QUAD 2-CHANNEL MULTIPLEXER (INV.)	158	158	158	158	158	158
SYNC. DECADE COUNTER WITH ASYNC. CLEAR	160	160	160	160	160	160
SYNC. BINARY COUNTER WITH ASYNC. CLEAR	161	161	161	161	161	161
SYNC. DECADE COUNTER WITH SYNC. CLEAR	162	162	162	162	162	162
SYNC. BINARY COUNTER WITH SYNC. CLEAR	163	163	163	163	163	163
8-BIT SIPO SHIFT REGISTER	164	164	164	164	164	164
8-BIT PISO SHIFT REGISTER	165	165	165	165	165	165
8-BIT PISO SHIFT REGISTER	166	166	166	166	166	166
QUAD D-TYPE REGISTER (3-STATE)	173	173	173	173	173	173
HEX D FLIP-FLOP WITH CLEAR	174	174	174	174	174	174
QUAD D FLIP-FLOP WITH CLEAR	175	175	175	175	175	175
ALITHMETIC LOGIC UNIT	181	181	–	181	181	–
LOOK AHEAD CARRY LOGIC	182	182	–	182	182	–
BCD UP/DOWN COUNTER	190	190	190	190	190	190
4-BIT BINARY UP/ DOWN COUNTER	191	191	191	191	191	191
SYNC. UP/DOWN DECADE COUNTER	192	192	192	192	192	192
SYNC. UP/DOWN BINARY COUNTER	193	193	193	193	193	193
4-BIT PIPO SHIFT REGISTER	194	194	194	194	194	194
4-BIT PIPO SHIFT REGISTER	195	195	195	195	195	–
DUAL MONOSTABLE MULTIVIBRATOR	221	221A	–	221	221A	221
3-TO-8 LINE DECODER/LATCH	237	237	237	237	237	–
3-TO-8 LINE DECODER	238	–	238	238	–	238
OCTAL BUS BUFFER (3-STATE/INV.)	240	240	240	240	240	240

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF74HC
OCTAL BUS BUFFER (3-STATE/INV.)	T240	T240	T240	T240	T240	T240
OCTAL BUS BUFFER (3-STATE)	241	241	241	241	241	241
OCTAL BUS BUFFER (3-STATE)	T241	T241	T241	T241	T241	T241
QUAD BUS TRANS-CEIVER (3-STATE/INV.)	242	242	242	242	242	242
QUAD BUS TRANS-CEIVER (3-STATE)	243	243	243	243	243	243
OCTAL BUS BUFFER (3-STATE)	244	244	244	244	244	244
OCTAL BUS BUFFER (3-STATE)	T244	T244	T244	T244	T244	T244
OCTAL BUS TRANS-CEIVER (3-STATE)	245	245	245	245	245	245
OCTAL BUS TRANS-CEIVER (3-STATE)	T245	T245	T245	T245	T245	T245
8-CHANNEL MULTI-PLEXER (3-STATE)	251	251	251	251	251	251
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	253	253	253	253	253	253
QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	257	257	257	257	257	257
QUAD 2-CHANNEL MULTIPLEXER (3-STATE/INV.)	258	–	258	258	–	–
8-BIT ADDRESSABLE LATCH	259	259	259	259	259	259
OCTAL D FLIP-FLOP WITH CLEAR	273	273	273	273	273	273
QUAD $\overline{S}$-$\overline{R}$ LATCH	279	–	–	–	–	–
9-BIT PARITY GENERATOR/CHECKER	280	280	280	280	280	280
4-BIT BINARY FULL ADDER	283	283	–	283	283	–
QUAD 2-CHANNEL MULTIPLEXER/ REGISTER	298	298	298	–	298	–
8-BIT PIPO SHIFT REGISTER	299	299	–	299	299	299
8-BIT PIPO SHIFT REGISTER	323	–	–	–	–	–
8-CHANNEL MULTI-PLEXER/REGISTER	354	354	354	354	354	354
8-CHANNEL MULTI-PLEXER/REGISTER	356	356	356	356	356	356

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
HEX BUS BUFFER (3-STATE)	365	365	365	365	365	365
HEX BUS BUFFER (3-STATE/INV.)	366	366	366	366	366	366
HEX BUS BUFFER (3-STATE)	367	367	367	367	367	367
HEX BUS BUFFER (3-STATE/INV.)	368	368	368	368	368	368
OCTAL D-TYPE LATCH (3-STATE)	373	373	373	373	373	373
OCTAL D-TYPE LATCH (3-STATE)	T373	T373	T373	T373	T373	T373
OCTAL D-TYPE FLIP-FLOP (3-STATE)	374	374	374	374	374	374
OCTAL D-TYPE FLIP-FLOP (3-STATE)	T374	T374	T374	T374	T374	T374
QUAD D-TYPE LATCH	375	–	375	–	–	–
OCTAL D-TYPE FLIP-FLOP	377	–	377	377	–	377
QUAD EXCLUSIVE OR GATE	386	–	386	–	–	–
DUAL DECADE COUNTER	390	390	390	390	390	390
DUAL BINARY COUNTER	393	393	393	393	393	393
DUAL MONOSTABLE MULTIVIBRATOR	423	423A	–	423	423A	423
OCTAL D-TYPE LATCH (3-STATE/INV.)	533	533	533	533	533	533
OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	534	534	534	534	534	534
OCTAL BUS BUFFER (3-STATE/INV.)	540	540	540	540	540	540
OCTAL BUS BUFFER (3-STATE/INV.)	T540	–	T540	T540	T540	T540
OCTAL BUS BUFFER (3-STATE)	541	541	541	541	541	541
OCTAL BUS BUFFER (3-STATE)	T541	–	T541	T541	T541	T541
OCTAL D-TYPE LATCH (3-STATE/INV.)	563	563	563	563	563	563
OCTAL D-TYPE LATCH (3-STATE/INV.)	T563	–	T563	T563	T563	T563
OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	564	564	564	564	564	564

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF74HC
OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	T564	–	T564	T564	T564	T564
OCTAL D-TYPE LATCH (3-STATE)	573	573	573	573	573	573
OCTAL D-TYPE LATCH (3-STATE)	T573	–	T573	T573	T573	T573
OCTAL D-TYPE FLIP-FLOP (3-STATE)	574	574	574	574	574	574
OCTAL D-TYPE FLIP-FLOP (3-STATE)	T574	–	T574	T574	T574	T574
8-BIT BINARY COUNTER/REGISTER (3-STATE)	590	–	–	–	590	–
8-BIT REGISTER/ BINARY COUNTER	592	–	–	–	592	–
8-BIT REGISTER/ BINARY COUNTER (3-STATE)	593	–	–	–	593	–
8-BIT SHIFT REGISTER/LATCH (3-STATE)	595	595	–	–	595	–
8-BIT LATCH/SHIFT REGISTER	597	597	–	–	597	–
OCTAL BUS TRANS-CEIVER (3-STATE/INV.)	620	–	620	–	–	–
OCTAL BUS TRANS-CEIVER (3-STATE)	623	–	623	–	–	–
OCTAL BUS TRANS-CEIVER (3-STATE/INV.)	640	640	640	640	640	640
OCTAL BUS TRANS-CEIVER (3-STATE/INV.)	T640	T640	T640	T640	T640	T640
OCTAL BUS TRANS-CEIVER (3-STATE)	643	643	643	643	643	643
OCTAL BUS TRANS-CEIVER (3-STATE)	T643	T643	T643	T643	T643	T643
OCTAL BUS TRANSCEIVER/ REGISTER (3-STATE)	646	646	646	646	646	646
OCTAL BUS TRANSCEIVER/ REGISTER (3-STATE)	T646	–	T646	T646	–	T646
OCTAL BUS TRANS-CEIVER/REGISTER (3-STATE/INV.)	648	648	648	648	648	648
OCTAL BUS TRANS-CEIVER/REGISTER (3-STATE/INV.)	T648	–	T648	T648	–	T648
OCTAL BUS TRANS-CEIVER/REGISTER (3-STATE/INV.)	651	–	651	–	–	–
OCTAL BUS TRANS-CEIVER/REGISTER (3-STATE/INV.)	T651	–	T651	–	–	–
OCTAL BUS TRANS-CEIVER/REGISTER (3-STATE)	652	–	652	–	–	–

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
OCTAL BUS TRANSCEIVER/ REGISTER (3-STATE)	T652	–	T652	–	–	–
4-WORD 4-BIT REGISTER FILE (3-STATE)	670	–	–	670	–	670
8-BIT EQUALITY COMPARATOR	688	688	688	688	688	688
DECADE COUNTER REGISTER (3-STATE)	690	–	–	–	–	–
4-BIT BINARY COUNTER REGISTER (3-STATE)	691	–	–	–	–	–
DECADE COUNTER REGISTER (3-STATE)	692	–	–	–	–	–
4-BIT BINARY COUNTER REGISTER (3-STATE)	693	–	–	–	–	–
U/D DECADE COUNTER/REGISTER (3-STATE)	696	–	–	–	–	–
U/D 4-BIT BINARY CTR./REGISTER (3-STATE)	697	–	–	–	–	–
U/D DECADE COUNTER/REGISTER (3-STATE)	698	–	–	–	–	–
U/D 4-BIT BINARY CTR./REGISTER (3-STATE)	699	–	–	–	–	–
DUAL 4-INPUT NOR GATE	4002	4002	4002	4002	4002	4002
DECADE COUNTER/ DIVIDER	4017	4017	4017	4017	4017	4017
14-STAGE BINARY COUNTER	4020	4020	4020	4020	4020	4020
OCTAL COUNTER/ DIVIDER	4022	–	4022	–	–	–
7-STAGE BINARY COUNTER	4024	4024	4024	4024	4024	4024
BCD-TO-DECIMAL DECODER	4028	–	–	–	–	4028
12-STAGE BINARY COUNTER	4040	4040	4040	4040	4040	4040
HEX BUFFER (INV.)	4049	4049	–	–	–	4049
HEX BUFFER	4050	4050	–	–	–	4050
8-CHANNEL ANALOG MULTIPLEXER	4051	4051	–	4051	4051	4051
DUAL 4-CHANNEL ANALOG MULTIPLEXER	4052	4052	–	4052	4052	4052
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	4053	4053	–	4053	4053	4053

CROSS REFERENCE TABLE

FUNCTION	TOSHIBA TC74HC	MOTOROLA MC74HC	TI SN74HC	RCA CD74HC	N.S. MM74HC	SIGNETICS PCF 74HC
14-STAGE BINARY COUNTER/ OSCILLATOR	4060	4060	4060	4060	4060	4060
QUAD BILATERAL SWITCH	4066	4066	–	4066	4066	4066
DUAL 4-INPUT OR GATE	4072	–	–	–	–	–
TRIPLE 3-INPUT OR GATE	4075	4075	4075	4075	4075	4075
8-INPUT OR/NOR GATE	4078	4078	4078A	–	4078	–
8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)	4094	–	–	4094	–	4094
DUAL BCD PROGRAMMABLE DOWN COUNTER	40102	–	–	40102	–	–
8-BIT BINARY PROGRAMMABLE DOWN COUNTER	40103	–	–	40103	–	–
BCD TO 7 SEGMENT L/D/D (LED)	4511	4511	–	4511	4511	4511
4-TO-16 LINE DECODER/LATCH	4514	4514	4514	4514	4514	4514
4-TO-16 LINE DECODER/ LATCH (INV.)	4515	–	4515	4515	4515	4515
DUAL DECADE COUNTER	4518	–	–	4518	4518	4518
DUAL 4-BIT BINARY COUNTER	4520	–	–	4520	4520	4520
DUAL MONOSTABLE MULTIVIBRATOR	4538	4538	–	4538	4538	4538
BCD TO 7 SEGMENT L/D/D (LCD)	4543	4543	–	4543	4543	4543
HEX BUFFER	T7007	–	–	–	–	–
QUAD EXCLUSIVE NOR GATE	7266	266	7266	7266	266	–
PROGRAMMABLE DIVIDER/TIMER	7292	292	–	–	292	–
PROGRAMMABLE DIVIDER/TIMER	7294	294	–	–	294	–